

CDCVF857

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

- **Recommended Applications:**
 - DDR Memory Modules (DDR400/333/266/200)
 - Zero Delay Fan-Out Buffer
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 220 MHz**
- **Low Jitter (Cycle-Cycle): ± 35 ps**
- **Low Static Phase Offset: ± 50 ps**
- **Low Jitter (Period): ± 30 ps**
- **1-To-10 Differential Clock Distribution (SSTL2)**
- **Best in Class for $V_{OX} = V_{DD}/2 \pm 0.1$ V**
- **Operates From Dual 2.6-V or 2.5-V Supplies**
- **Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, 56-Ball MicroStar Junior™ BGA Package**
- **Consumes < 100 - μ A Quiescent Current**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**
- **Meets/Exceeds JEDEC Standard (JESD82–1) For DDRI-200/266/333 Specification**
- **Meets/Exceeds Proposed DDRI-400 Specification (JESD82–1A)**
- **Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low**

description

The CDCVF857 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and one differential pair of feedback clock outputs (FBOU, $\overline{\text{FBOU}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When PWRDWN is high, the outputs switch in phase and frequency with CLK. When PWRDWN is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a >20-MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Because the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T _A	TSSOP (DGG)	40-Pin MLF	56-Ball BGA †
–40°C to 85°C	CDCVF857DGG (Pb-Free)	CDCVF857RTB	CDCVF857GQL
–40°C to 85°C		CDCVF857RHA (Pb-Free, Green)	

† Maximum load recommended is 12 pf for 200 MHz. At 12-pf load, maximum T_A allowed is 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

CDCVF857

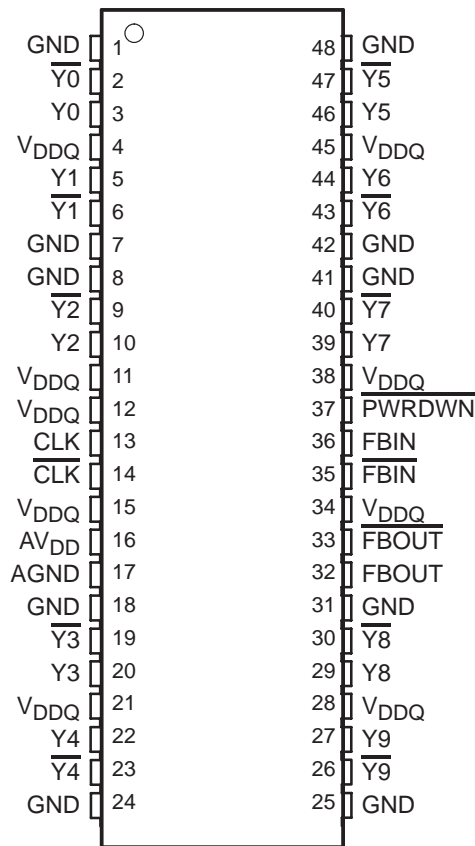
2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

FUNCTION TABLE
(Select Functions)

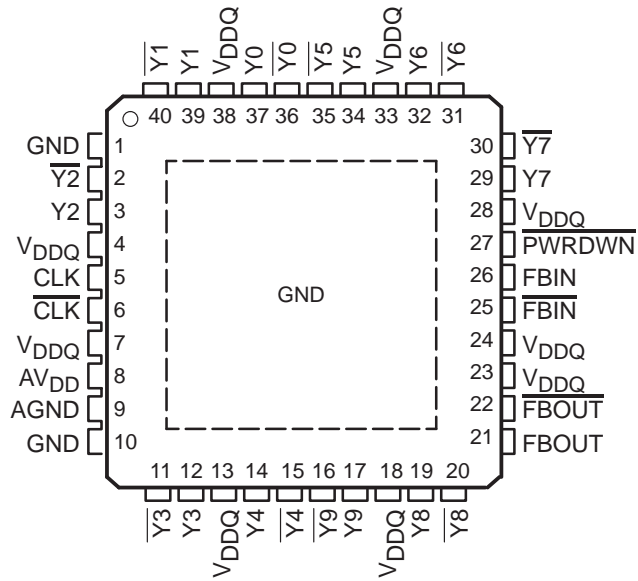
INPUTS				OUTPUTS				PLL
AVDD	PWRDWN	CLK	CLK	Y[0:9]	Y[0:9]	FBOUT	FBOUT	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

DGG PACKAGE (TSSOP)
(TOP VIEW)



48-pin TSSOP (MO-153-ED)

RHA/RTB PACKAGE (MLF)
(TOP VIEW)



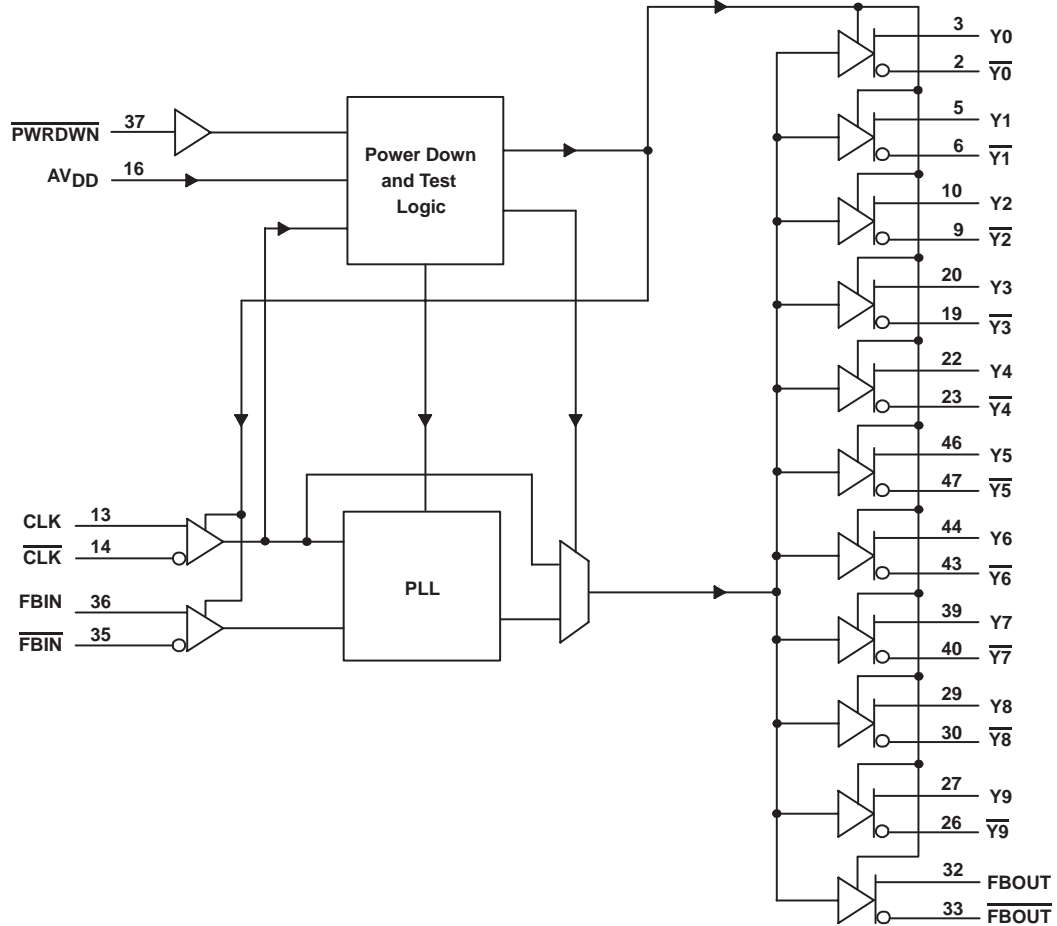
40-pin HP-VFQFP-N (6,0 x 6,0-mm Body Size, 0,5-mm Pitch, M0#220, Variation VJJD-2, E2 = D2 = 2,9 mm ± 0,15 mm) Package Pinouts

CDCVF857

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

functional block diagram



Terminal Functions

NAME	TERMINAL			I/O	DESCRIPTION
	DGG	RHA/RTB	GQL		
AGND	17	9	H1		Ground for 2.5-V analog supply
AV _{DD}	16	8	G2		2.5-V analog supply
CLK, $\overline{\text{CLK}}$	13, 14	5, 6	F1, F2	I	Differential clock input
$\overline{\text{FBIN}}$, FBIN	35, 36	25, 26	F5, F6	I	Feedback differential clock input
FBO _{UT} , $\overline{\text{FBOU}}$	32, 33	21, 22	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	1, 10	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{\text{PWRDWN}}$	37	27	E6	I	Output enable for Y and $\overline{\text{Y}}$
V _{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	4, 7, 13, 18, 23, 24, 28, 33, 38	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V supply
Y0, $\overline{\text{Y0}}$	3, 2	37, 36	A1, A2	O	Buffered output copies of input clock, CLK, $\overline{\text{CLK}}$
Y1, $\overline{\text{Y1}}$	5, 6	39, 40	B2, B1	O	
Y2, $\overline{\text{Y2}}$	10, 9	3, 2	D1, D2	O	
Y3, $\overline{\text{Y3}}$	20, 19	12, 11	J2, J1	O	
Y4, $\overline{\text{Y4}}$	22, 23	14, 15	K1, K2	O	
Y5, $\overline{\text{Y5}}$	46, 47	34, 35	A6, A5	O	
Y6, $\overline{\text{Y6}}$	44, 43	32, 31	B5, B6	O	
Y7, $\overline{\text{Y7}}$	39, 40	29, 30	D6, D5	O	
Y8, $\overline{\text{Y8}}$	29, 30	19, 20	J5, J6	O	
Y9, $\overline{\text{Y9}}$	27, 26	17, 16	K6, K5	O	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{DDQ} , AV _{DD}	0.5 V to 3.6 V
Input voltage range, V _I (see Notes 1 and 2)	-0.5 V to V _{DDQ} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	-0.5 V to V _{DDQ} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DDQ})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DDQ})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{DDQ})	±50 mA
Continuous current to GND or V _{DDQ}	±100 mA
Storage temperature range T _{stg}	-65°C to 150°C

θ_{JA} For TSSOP (DGG) Package (see Note 3)

θ_{JA} For MLF (RHA/RTB) Package

θ_{JA} For BGA(GQL) Package (see Note 4)

Airflow	Low K	High K	Airflow	With 4 Thermal Vias	Airflow	High K
0 ft/min	89.1°C/W	70°C/W	0 ft/min	44.7°C/W	0 ft/min	132.2°C/W
150 ft/min	78.5°C/W	65.3°C/W	150 ft/min		150 ft/min	126.4°C/W

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 - This value is limited to 3.6 V maximum.
 - The package thermal impedance is calculated in accordance with JESD 51.
 - Connecting the NC-balls (C3, C4, D3, D4, G3, G4, H3, H4) to a ground plane improves the θ_{JA} to 114.8°C/W (0 airflow).

CDCVF857

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

recommended operating conditions (see Note 5)

			MIN	TYP	MAX	UNIT
Supply voltage	V _{DDQ}	PC1600 – PC3200	2.3		2.7	V
	AV _{DD}		V _{DDQ} – 0.12		2.7	
Low-level input voltage, V _{IL}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$				V _{DDQ} /2 – 0.18	V
	PWRDWN		–0.3		0.7	
High-level input voltage, V _{IH}	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$		V _{DDQ} /2 + 0.18			V
	PWRDWN		1.7		V _{DDQ} + 0.3	
DC input signal voltage (see Note 5)			–0.3		V _{DDQ} + 0.3	V
Differential input signal voltage, V _{ID} (see Note 6)	dc	CLK, FBIN	0.36		V _{DDQ} + 0.6	V
	ac	CLK, FBIN	0.7		V _{DDQ} + 0.6	
Input differential pair cross voltage, V _{IX} (see Notes 7 and 8)			V _{DDQ} /2 – 0.2		V _{DDQ} /2 + 0.2	V
High-level output current, I _{OH}					–12	mA
Low-level output current, I _{OL}					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T _A			–40		85	°C

- NOTES: 5. The unused inputs must be held high or low to prevent them from floating.
6. The dc input signal voltage specifies the allowable dc execution of the differential input.
7. The differential input signal voltage specifies the differential voltage |V_TR – V_CP| required for switching, where V_TR is the true input level and V_CP is the complementary input level.
8. The differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input voltage	All inputs	V _{DDQ} = 2.3 V, I _I = –18 mA				–1.2	V
V _{OH}	High-level output voltage		V _{DDQ} = min to max, I _{OH} = –1 mA		V _{DDQ} – 0.1			V
			V _{DDQ} = 2.3 V, I _{OH} = –12 mA		1.7			
V _{OL}	Low-level output voltage		V _{DDQ} = min to max, I _{OL} = 1 mA				0.1	V
			V _{DDQ} = 2.3 V, I _{OL} = 12 mA				0.6	
V _{OD}	Output voltage swing‡		Differential outputs are terminated with 120 Ω /C _L = 14 pF (See Figure 3)		1.1		V _{DDQ} – 0.4	V
V _{OX}	Output differential cross-voltage§				V _{DDQ} /2 – 0.1	V _{DDQ} /2	V _{DDQ} /2 + 0.1	
I _I	Input current		V _{DDQ} = 2.7 V, V _I = 0 V to 2.7 V				±10	μA
I _{OZ}	High-impedance state output current		V _{DDQ} = 2.7 V, V _O = V _{DDQ} or GND				±10	μA
I _{DDPD}	Power-down current on V _{DDQ} + AV _{DD}		CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I _{DD} and A _I DD			20	100	μA
A _I DD	Supply current on AV _{DD}		f _O = 170 MHz			6	8	mA
			f _O = 200 MHz			8	10	
C _I	Input capacitance		V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND		2	2.5	3.5	pF

† All typical values are at a respective nominal V_{DDQ}.

‡ The differential output signal voltage specifies the differential voltage |V_TR – V_CP|, where V_TR is the true output level and V_CP is the complementary output level.

§ The differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I _{DD}	Dynamic current on V _{DDQ}	Without load	f _O = 170 MHz	120	140	mA
			f _O = 200 MHz	125	150	
		Differential outputs terminated with 120 Ω/C _L = 0 pF	f _O = 170 MHz	220	270	
			f _O = 200 MHz	230	280	
		Differential outputs terminated with 120 Ω/C _L = 14 pF	f _O = 170 MHz	280	330	
			f _O = 200 MHz	300	350	
ΔC	Part-to-part input capacitance variation	V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND			1	pF
C _{I(Δ)}	Input capacitance difference between CLK and CKB, FBIN, and FBINB	V _{DDQ} = 2.5 V, V _I = V _{DDQ} or GND			0.25	pF

† All typical values are at a respective nominal V_{DDQ}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f _{CLK}	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	
Input clock duty cycle		40%	60%	
Stabilization time† (PLL mode)			10	μs
Stabilization time‡ (bypass mode)			30	ns

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} §	Low-to-high level propagation delay time	Test mode/CLK to any output		3.5		ns
t _{PHL} §	High-to-low level propagation delay time	Test mode/CLK to any output		3.5		ns
t _{jit(per)} ¶	Jitter (period), See Figure 7	100 MHz (PC1600)	-65		65	ps
		133/167/200 MHz (PC2100/2700/3200)	-30		30	
t _{jit(cc)} ¶	Jitter (cycle-to-cycle), See Figure 4	100 MHz (PC1600)	-50		50	ps
		133/167/200 MHz (PC2100/2700/3200)	-35		35	
t _{jit(hper)} ¶	Half-period jitter, See Figure 8	100 MHz (PC1600)	-100		100	ps
		133/167/200 MHz (PC2100/2700/3200)	-75		75	
t _{slr(o)}	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF		1	2	V/ns
t(∅)	Static phase offset, See Figure 5	100/133/167/200 MHz		-50	50	ps
t _{sk(o)}	Output skew, See Figure 6	Load: 120 Ω/14 pF 100/133/167/200 MHz			40	ps

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.

CDCVF857 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

PARAMETER MEASUREMENT INFORMATION

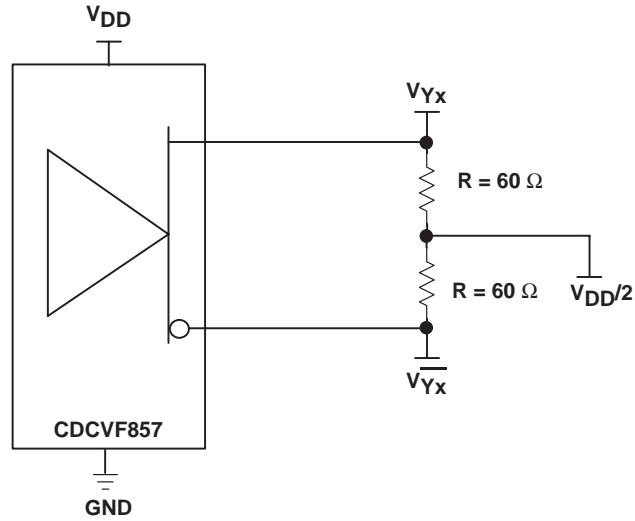


Figure 1. IBIS Model Output Load

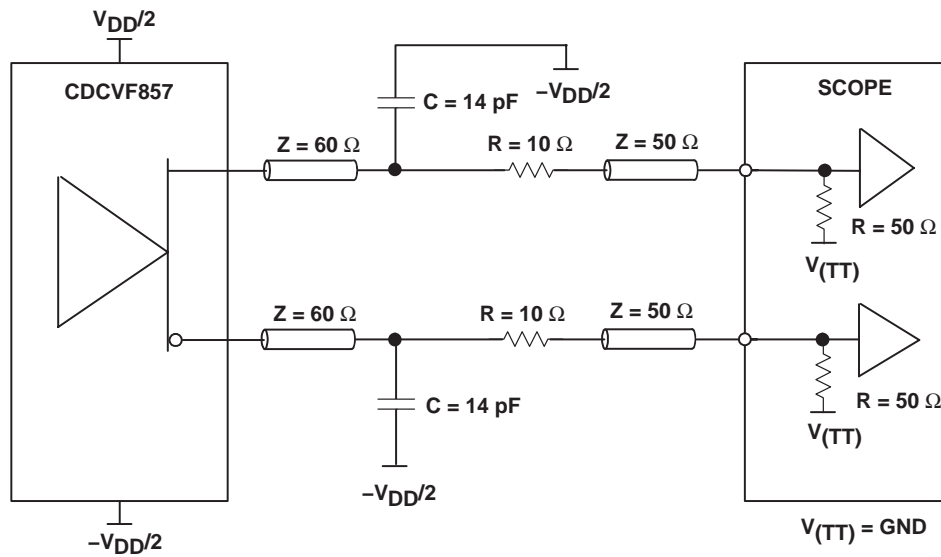


Figure 2. Output Load Test Circuit

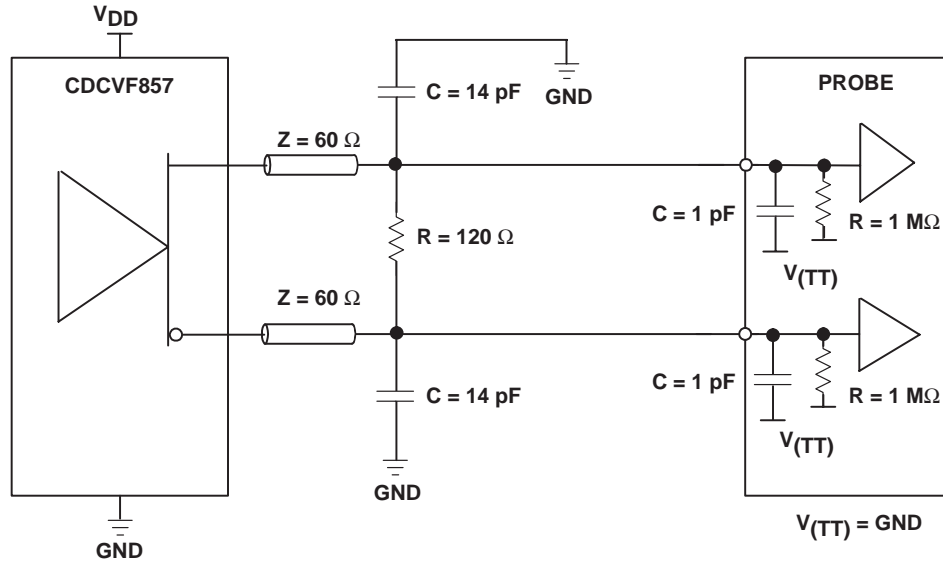


Figure 3. Output Load Test Circuit for Crossing Point

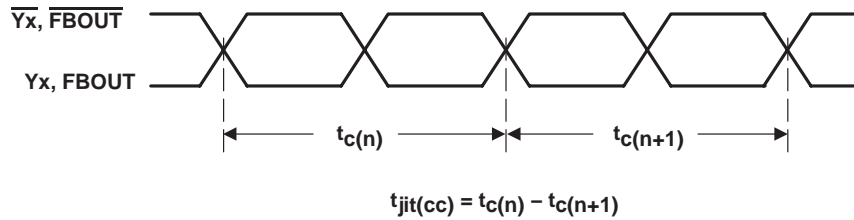


Figure 4. Cycle-to-Cycle Jitter

CDCVF857

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005

PARAMETER MEASUREMENT INFORMATION

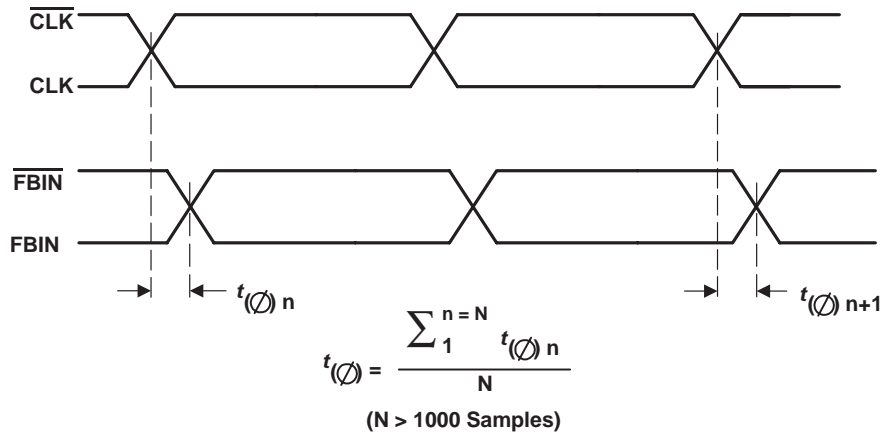


Figure 5. Phase Offset

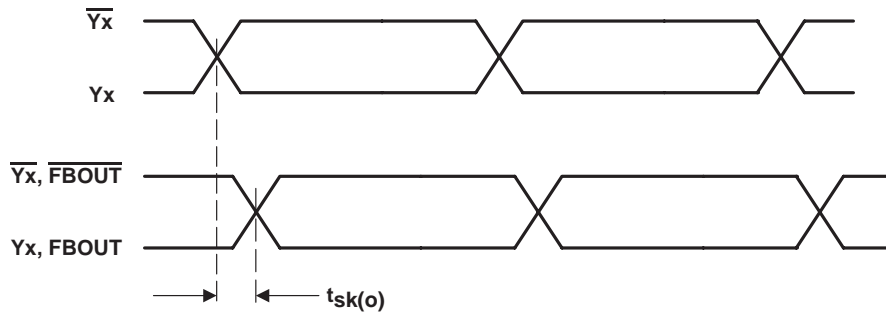


Figure 6. Output Skew

PARAMETER MEASUREMENT INFORMATION

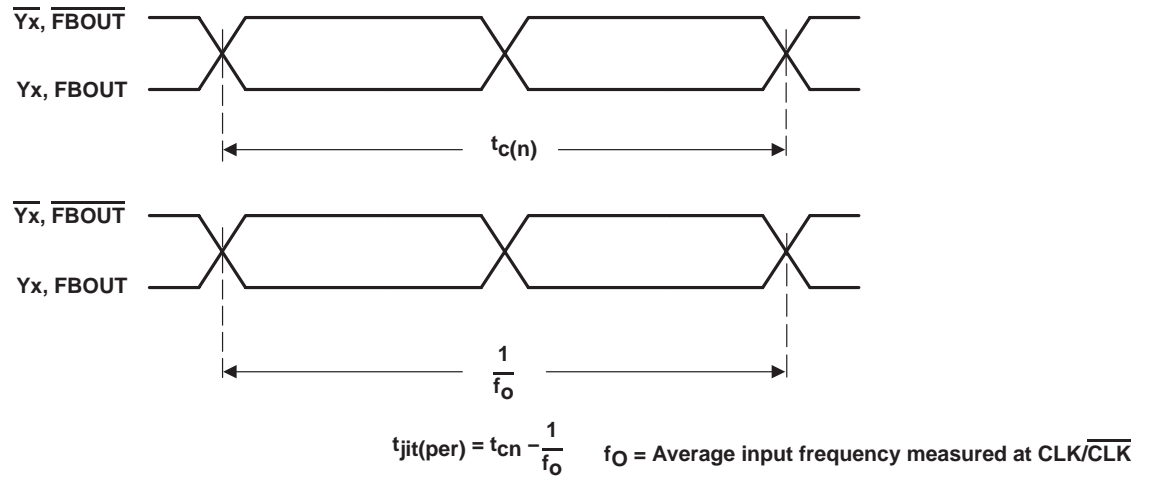


Figure 7. Period Jitter

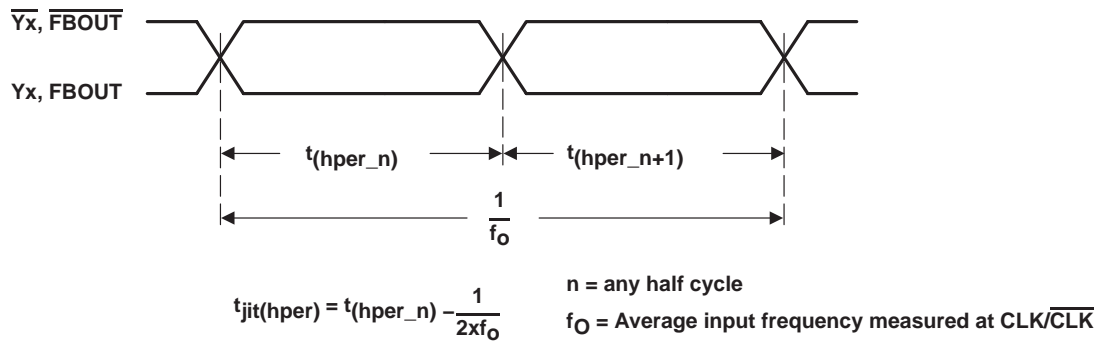


Figure 8. Half-Period Jitter

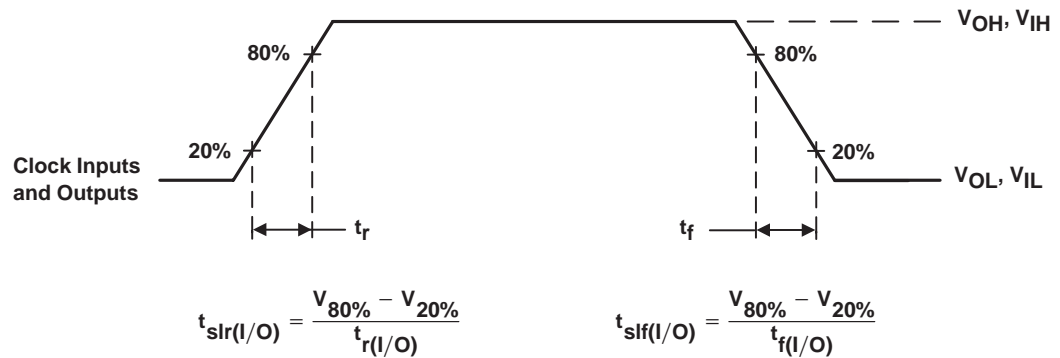
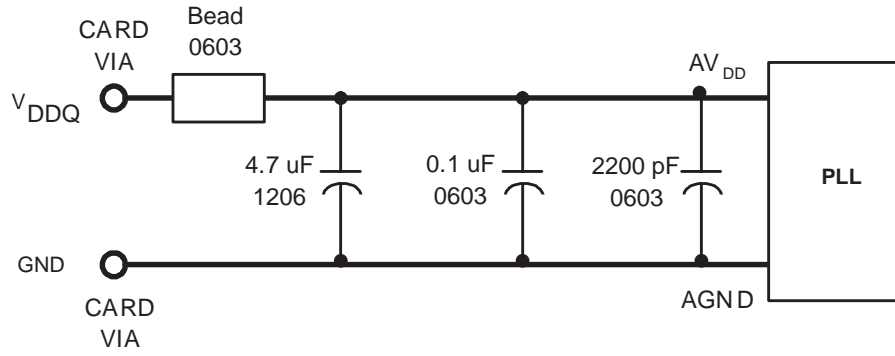


Figure 9. Input and Output Slew Rates

CDCVF857

2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS047D – MARCH 2003 – REVISED JUNE 2005



See Notes 9, 10, and 11

Figure 10. Recommended AV_{DD} Filtering

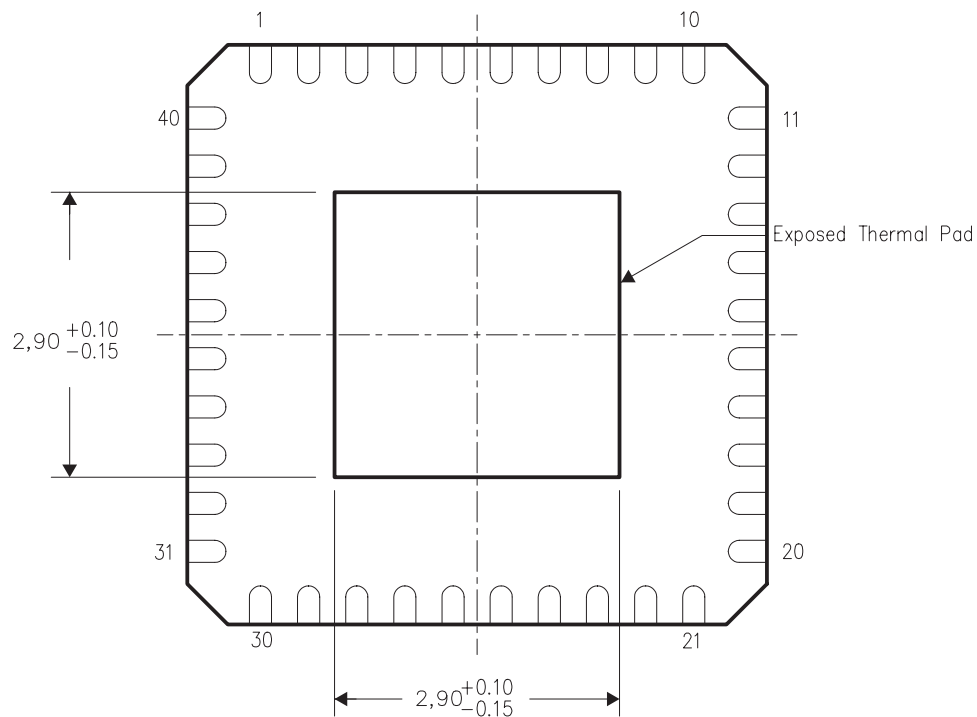
- NOTES:
9. Place the 2200-pF capacitor close to the PLL.
 10. Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
 11. Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDCVF857DGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCVF857DGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCVF857DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCVF857DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCVF857GQLR	ACTIVE	VFBGA	GQL	56	1000	TBD	Call TI	Level-2A-220C-4 WKS
CDCVF857RHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCVF857RHARG4	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCVF857RHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCVF857RHATG4	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCVF857RTBR	ACTIVE	QFN	RTB	40	2500	TBD	CU SNPB	Level-3-235C-168 HR
CDCVF857RTBT	ACTIVE	QFN	RTB	40	250	TBD	CU SNPB	Level-3-235C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

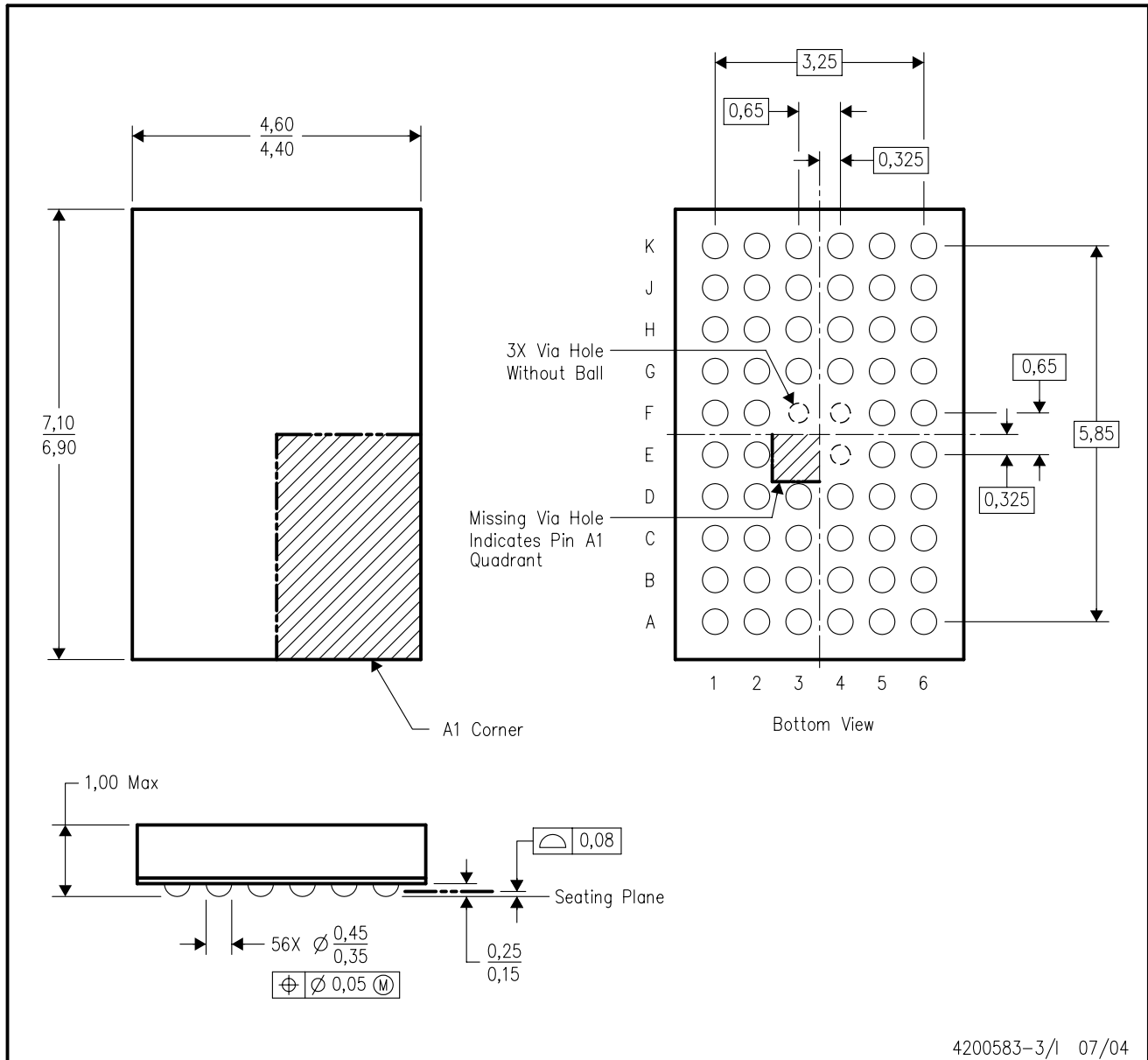
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GQL (R-PBGA-N56)

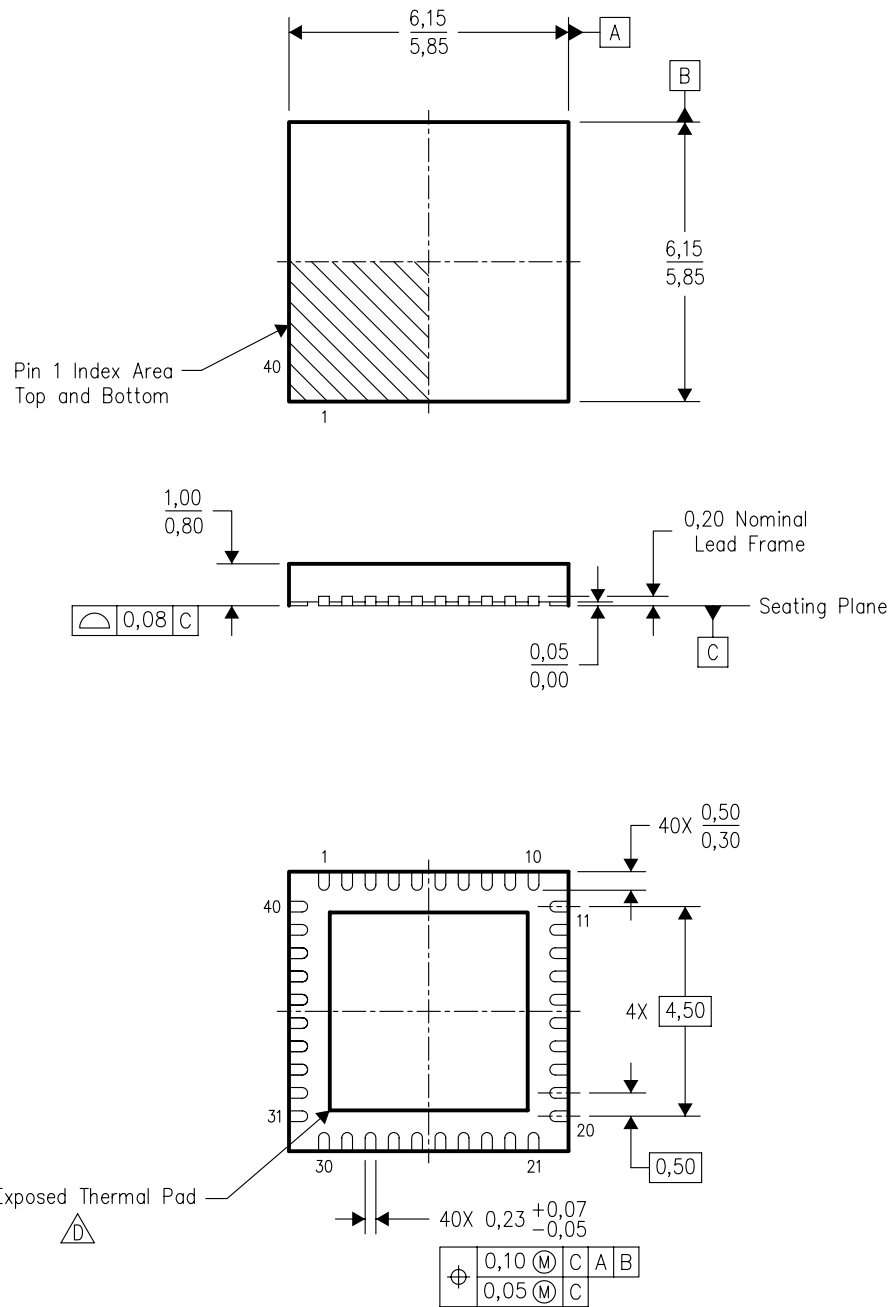
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.


RHA (S-PQFP-N40)

PLASTIC QUAD FLATPACK



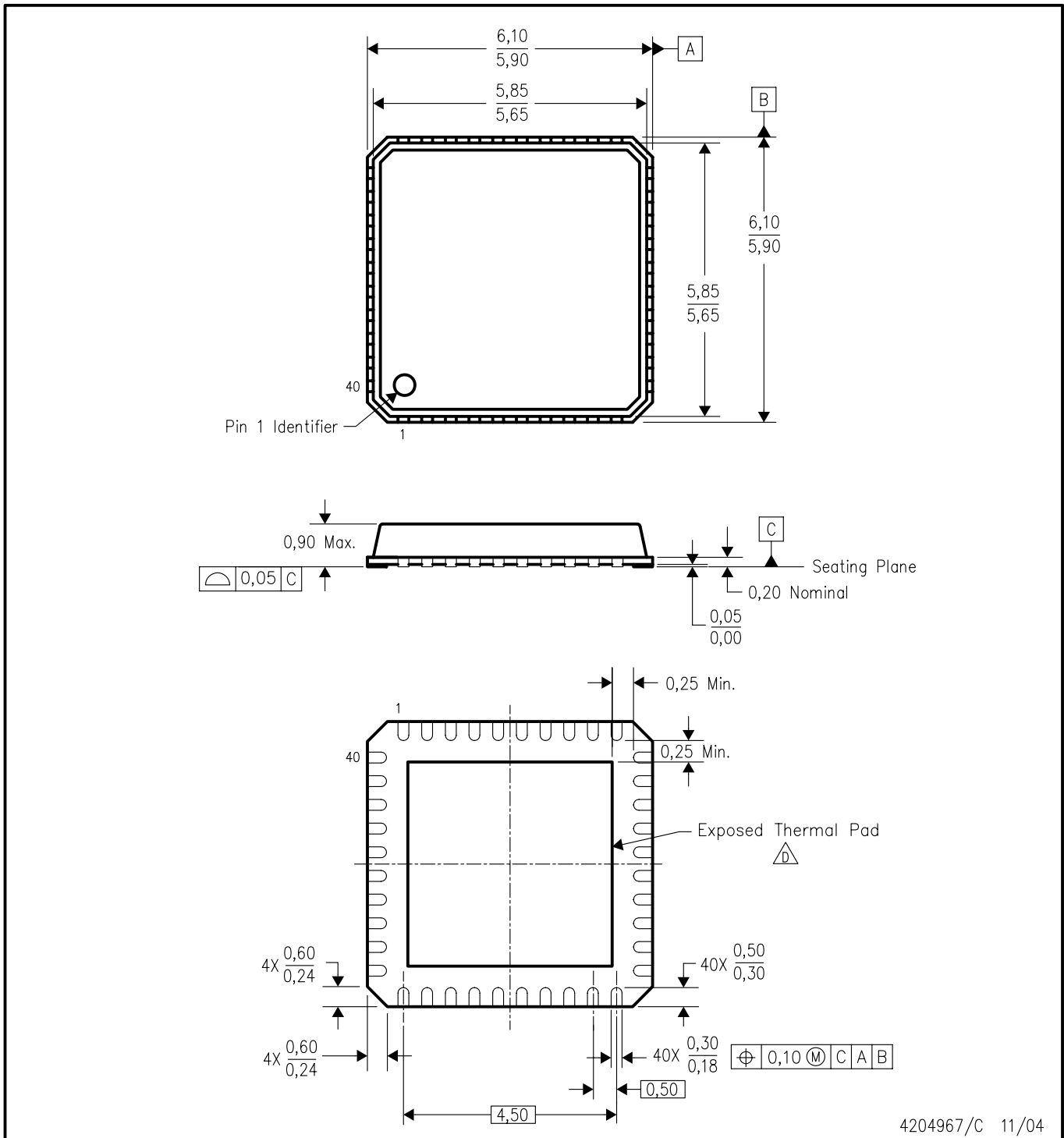
Bottom View

4204276/C 12/2004


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-220 variation VJJD-2.

RTB (S-PQFP-N40)

PLASTIC QUAD FLATPACK



4204967/C 11/04

- NOTES: A. All linear dimensions are in millimeters.
 Dimensioning and tolerancing per ASME Y14.5M-1994.  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 B. This drawing is subject to change without notice.
 C. QFN (Quad Flatpack No-Lead) Package configuration.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265