

# CEP7030L/CEB7030L

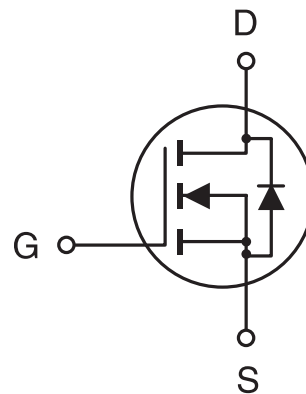
JUN 1998

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

4

### FEATURES

- 30V , 65A ,  $R_{DS(ON)} = 8m\Omega$  @  $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 12m\Omega$  @  $V_{GS} = 4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS ( $T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Drain Current-Continuous @ $T_J = 125^\circ\text{C}$ -Pulsed	$I_D$	65	A
	$I_{DM}$	180	A
Drain-Source Diode Forward Current	$I_S$	65	A
Maximum Power Dissipation @ $T_c = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50	W
		0.4	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-65 to 175	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case <sup>a</sup>	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

# CEP7030L/CEB7030L

4

## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	35		V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			10	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.5	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =35A		7.4	8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =28A		10.6	12	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V	60			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =35A		50		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		2000	2200	pF
Output Capacitance	C <sub>OSS</sub>			1011	1250	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			131	400	pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =60A, V <sub>GEN</sub> =10V R <sub>G</sub> =1.8 Ω R <sub>L</sub> =0.25 Ω		15		ns
Rise Time	t <sub>r</sub>			210		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			30		ns
Fall Time	t <sub>f</sub>			55		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =24V, I <sub>D</sub> =60A, V <sub>GS</sub> =10V		60	110	nC
Gate-Source Charge	Q <sub>gs</sub>			9	31	nC
Gate-Drain Charge	Q <sub>gd</sub>			20	57	nC

# CEP7030L/CEB7030L

## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 35A		0.93	1.3	V

Notes

- a. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

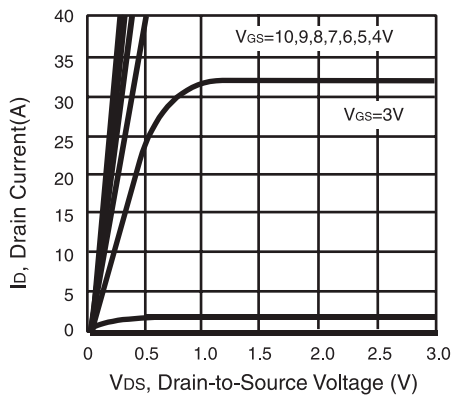


Figure 1. Output Characteristics

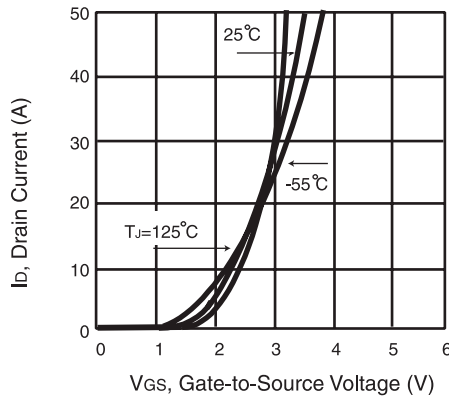


Figure 2. Transfer Characteristics

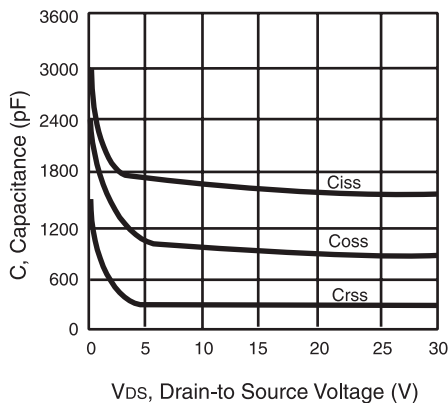


Figure 3. Capacitance

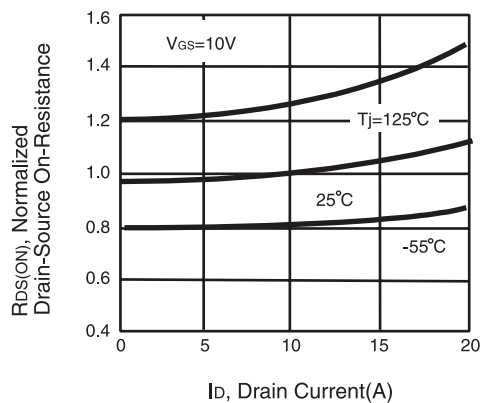
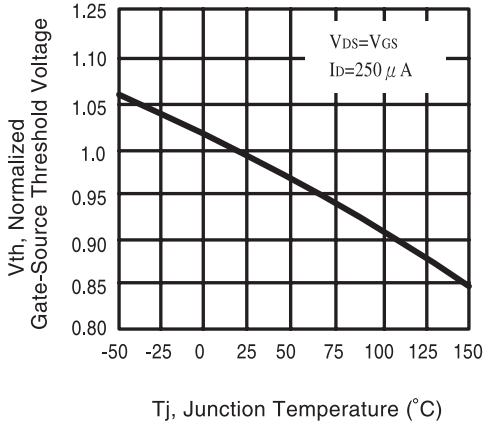


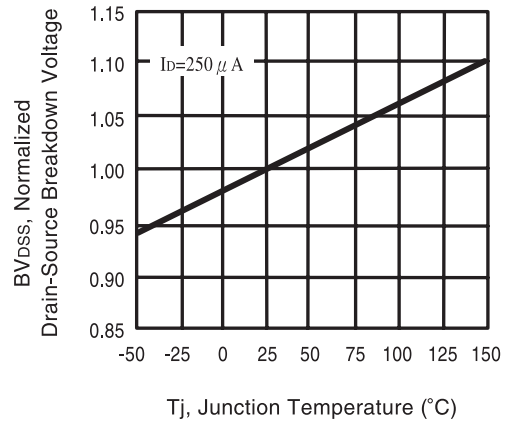
Figure 4. On-Resistance Variation with Drain Current and Temperature

# CEP7030L/CEB7030L

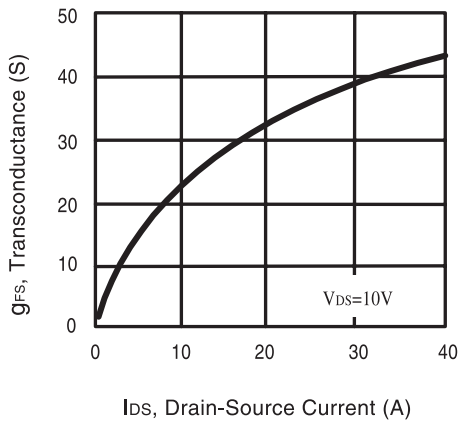
4



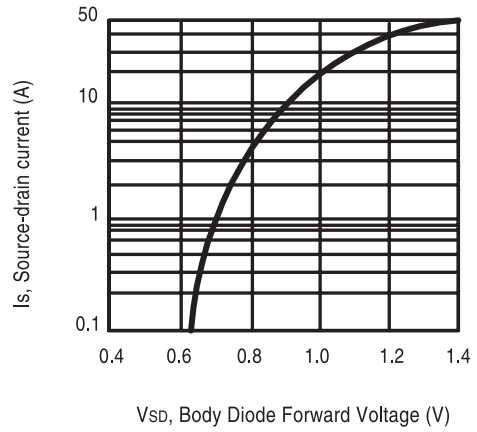
**Figure 5. Gate Threshold Variation with Temperature**



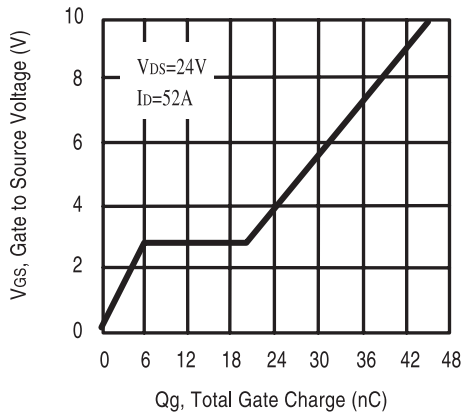
**Figure 6. Breakdown Voltage Variation with Temperature**



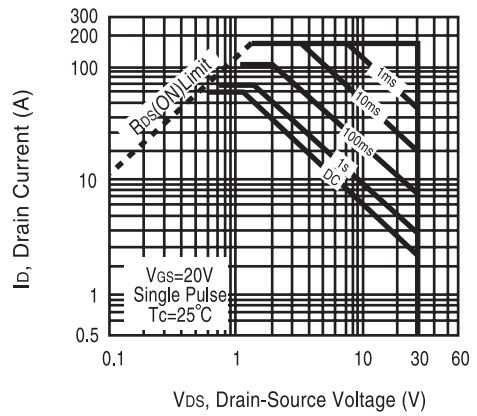
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

# CEP7030L/CEB7030L

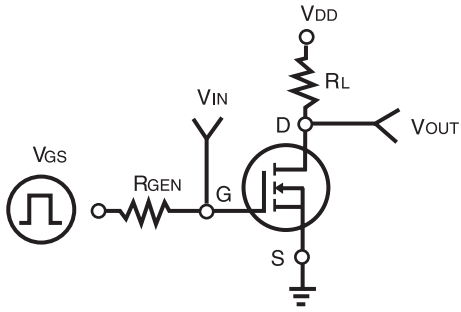


Figure 11. Switching Test Circuit

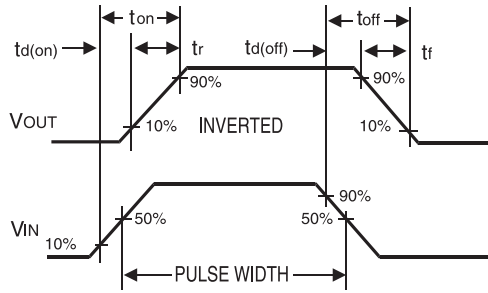


Figure 12. Switching Waveforms

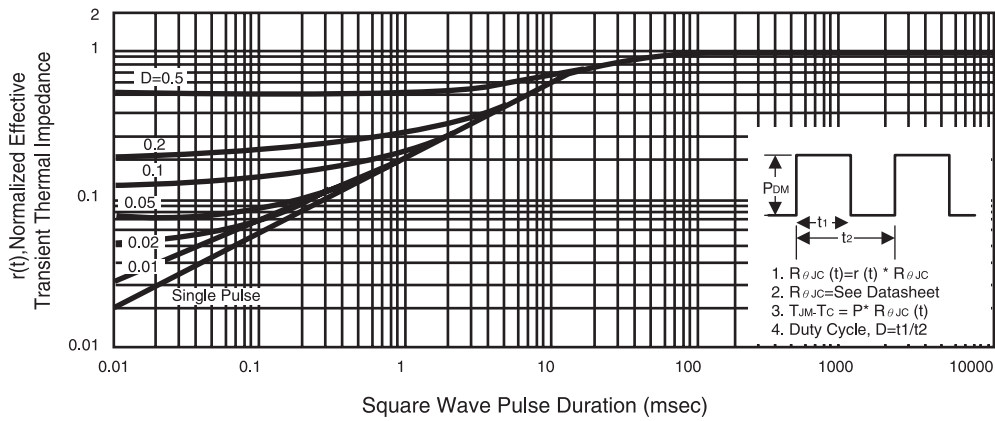


Figure 13. Normalized Thermal Transient Impedance Curve