



CEP655N/CEB655N CEI655N/CEF655N

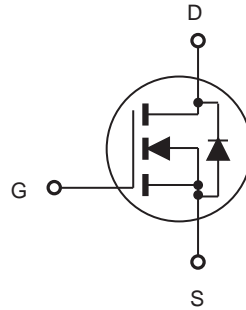
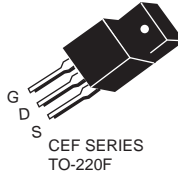
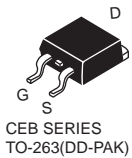
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP655N	150V	0.153Ω	15A	10V
CEB655N	150V	0.153Ω	15A	10V
CEI655N	150V	0.153Ω	15A	10V
CEF655N	150V	0.153Ω	15A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V _{DS}	150		V
Gate-Source Voltage	V _{GS}	±25		V
Drain Current-Continuous	I _D	15	15 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	60	60 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	83	39	W
		0.56	0.26	W/°C
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 175		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	1.8	3.8	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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<http://www.cetsemi.com>



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	150			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 25V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -25V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 8.2A$		118	153	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 40V, I_D = 8.2A$		5		S
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		750		pF
Output Capacitance	C_{oss}			175		pF
Reverse Transfer Capacitance	C_{riss}			70		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75V, I_D = 15A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		17	35	ns
Turn-On Rise Time	t_r			48	100	ns
Turn-Off Delay Time	$t_{d(off)}$			40	80	ns
Turn-Off Fall Time	t_f			46	90	ns
Total Gate Charge	Q_g	$V_{DS} = 120V, I_D = 15A,$ $V_{GS} = 10V$		26	34	nC
Gate-Source Charge	Q_{gs}			6		nC
Gate-Drain Charge	Q_{gd}			12.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				15	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 15A^g$			1.5	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e .Pulse width limited by safe operating area . f .Full package $I_{S(max)} = 10A$. g.Full package V_{SD} test condition $I_S = 10A$.						



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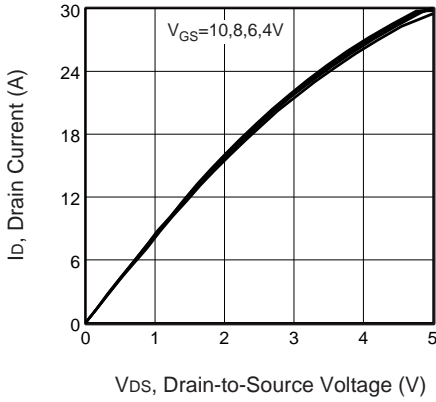


Figure 1. Output Characteristics

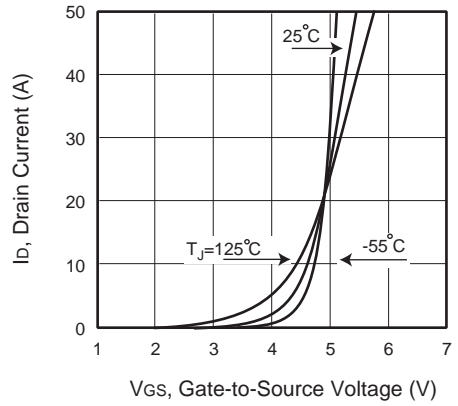


Figure 2. Transfer Characteristics

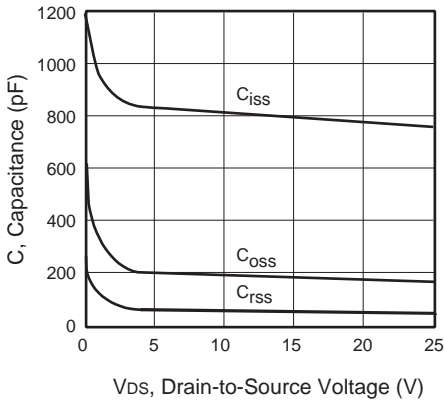


Figure 3. Capacitance

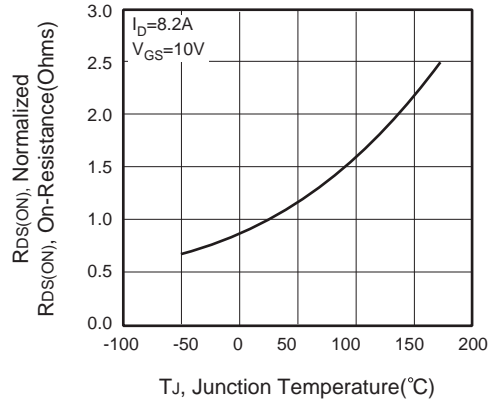


Figure 4. On-Resistance Variation with Temperature

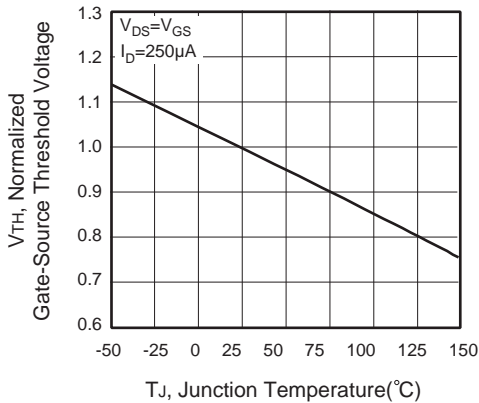


Figure 5. Gate Threshold Variation with Temperature

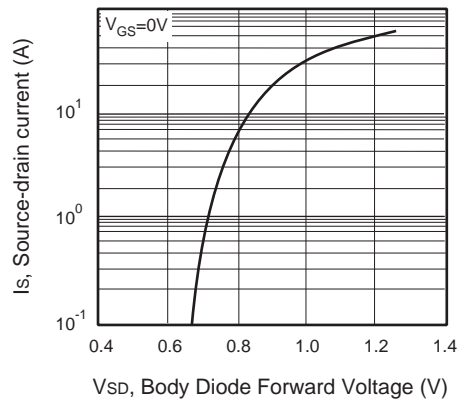


Figure 6. Body Diode Forward Voltage Variation with Source Current



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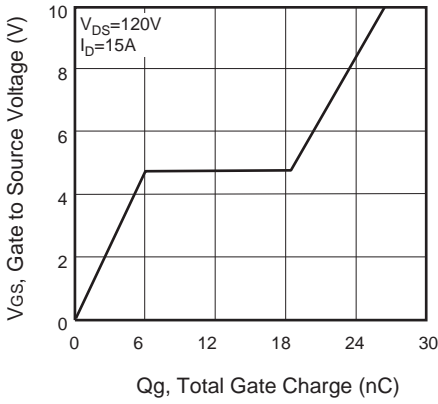


Figure 7. Gate Charge

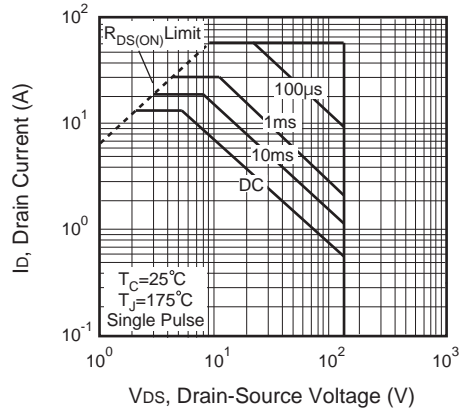


Figure 8. Maximum Safe Operating Area

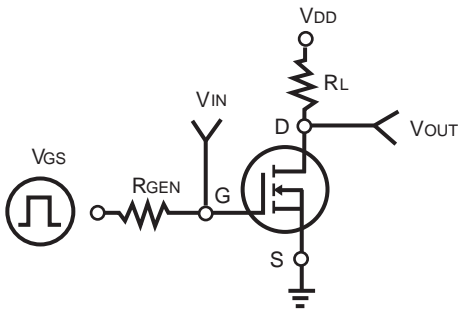


Figure 9. Switching Test Circuit

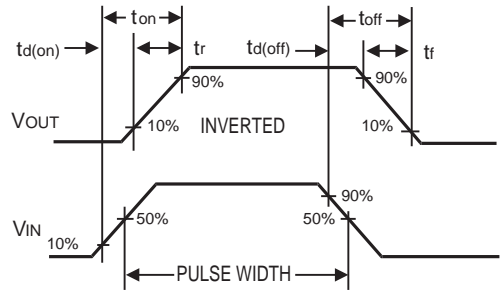


Figure 10. Switching Waveforms

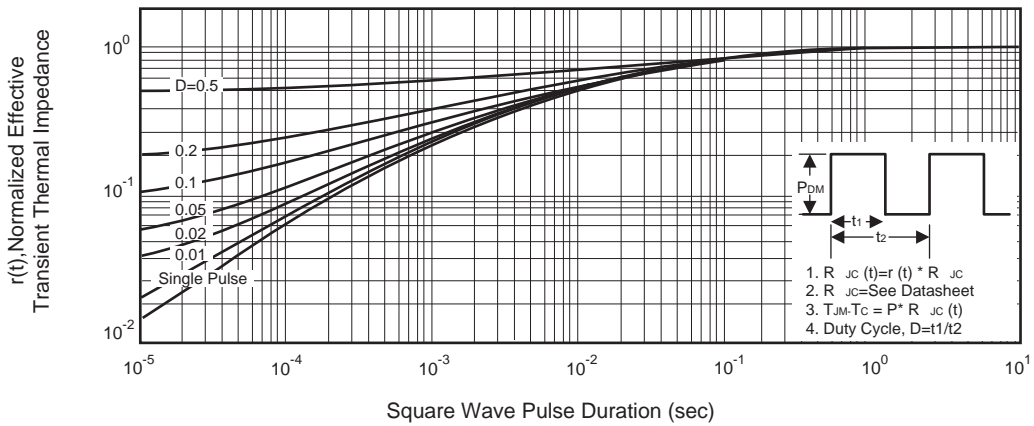


Figure 11. Normalized Thermal Transient Impedance Curve