

CF010 Series

Broadband Power GaAs MESFET Chips

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- ❑ **P_{1dB} Power:**
 - CF003-01: +22 dBm
 - CF005-01: +25 dBm
 - CF010-01: +28 dBm
- ❑ **High Gain (@ 12 GHz):**
 - CF003-01: 9.0 dB
 - CF005-01: 8.5 dB
 - CF010-01: 8.0 dB
- ❑ **Broadband: Usable to 18 GHz**
- ❑ **Wafer Qualification Procedure**
- ❑ **Customer Wafer Selection Available**

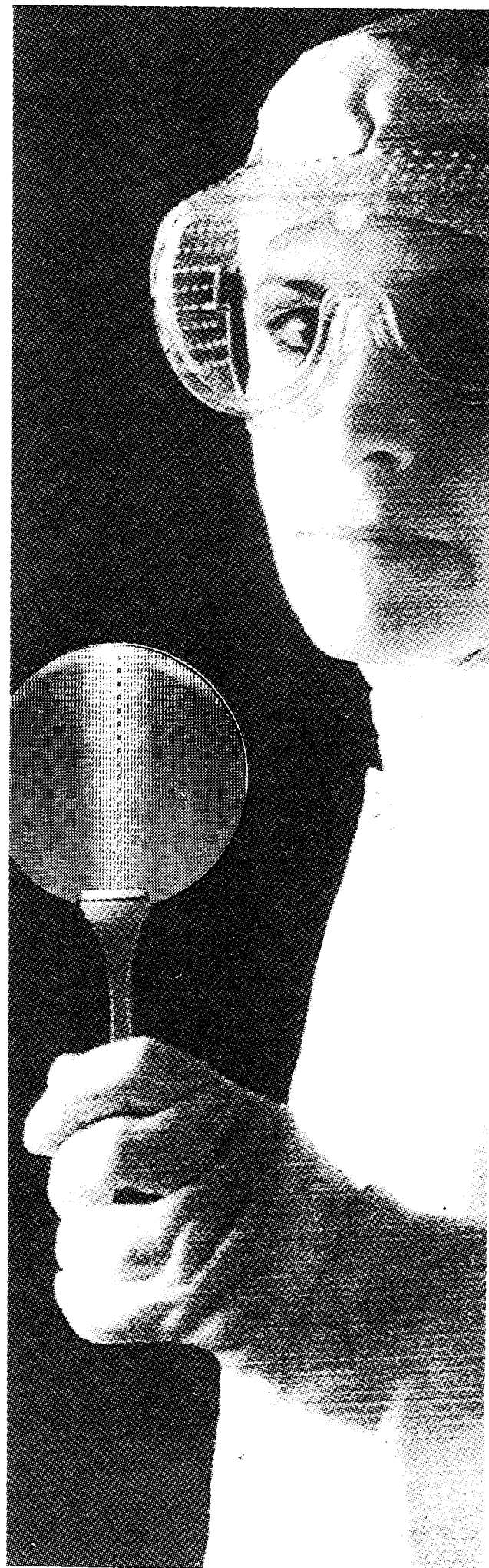
Celeritek Broadband Power Chips

Celeritek Medium Power Chips are GaAs MESFETs which include the CF003-01, CF005-01 and CF010-01 models. They are 600 μm , 1200 μm and 2400 μm gate width, respectively. All have sub-half-micron gate lengths, Celeritek's proprietary Silicon Nitride passivation, and are fabricated on ion implanted wafers.

Celeritek's Wafer Qualification Procedure for these devices consists of DC, RF and reliability testing of both individual die and generic 6 to 18 GHz amplifier modules.

Celeritek's broadband power chips make up a family of GaAs FET devices which have high broadband gain and provide up to 1 watt in balanced 6 to 18 GHz amplifier circuits. These devices are also suitable for high power oscillators. In narrow band applications they offer superior associated gain.

These devices are available in chip form and are suitable for airborne, shipboard and ground-based equipment. Screening includes MIL-STD-750 Class B, Class S and commercial screening. These devices are also available in packaged form. Please consult the Packaged Power GaAs FET data sheets or contact the factory for further information.



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Broadband Power GaAs Chips

Specifications ($T_A = 25^\circ\text{C}$)				CF003-01			CF005-01			CF010-01		
Active Layer				Ion Implanted			Ion Implanted			Ion Implanted		
Symbol	Parameters and Conditions	Frequency (GHz)	Units	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
G_L	Linear Power Gain $V_{DS} = 6.0\text{ V}$, $I_{DS} = 80\text{ mA}$ $V_{DS} = 6.0\text{ V}$, $I_{DS} = 160\text{ mA}$ $V_{DS} = 6.0\text{ V}$, $I_{DS} = 300\text{ mA}$	12.0	dB	8.0	9.0		7.5	8.5		7.0	8.0	
P_{1dB}	Power Output @ 1 dB GC $V_{DS} = 6.0\text{ V}$, $I_{DS} = 80\text{ mA}$ $V_{DS} = 6.0\text{ V}$, $I_{DS} = 160\text{ mA}$ $V_{DS} = 6.0\text{ V}$, $I_{DS} = 300\text{ mA}$	12.0	dBm	21.5	22.0		24.0	25.0		27.0	28.0	
g_m	Transconductance $V_{DS} = 3.0\text{ V}$, $V_{GS} = 0\text{ V}$		mS		120			240			480	
I_{DSS}	Drain Current $V_{DS} = 3.0\text{ V}$, $V_{GS} = 0\text{ V}$		mA	120	180	240	220	350	440	440	700	880
V_P	Pinchoff Voltage $V_{DS} = 3.0\text{ V}$, $I_{DS} = 1\text{ mA}$		Volts	-0.7	-1.3	-2.5	-0.7	-1.3	-2.5	-0.7	-1.3	-2.5
BV_{GD}	Breakdown Voltage, Gate-Drain $I_{GD} = 100\text{ }\mu\text{A}$ $I_{GD} = 200\text{ }\mu\text{A}$ $I_{GD} = 400\text{ }\mu\text{A}$		Volts	-5.5	-8.0		-5.5	-8.0		-5.5	-8.0	
R_{th}	Thermal Resistance		$^\circ\text{C/W}$		80			50			25	

Absolute Maximum Ratings

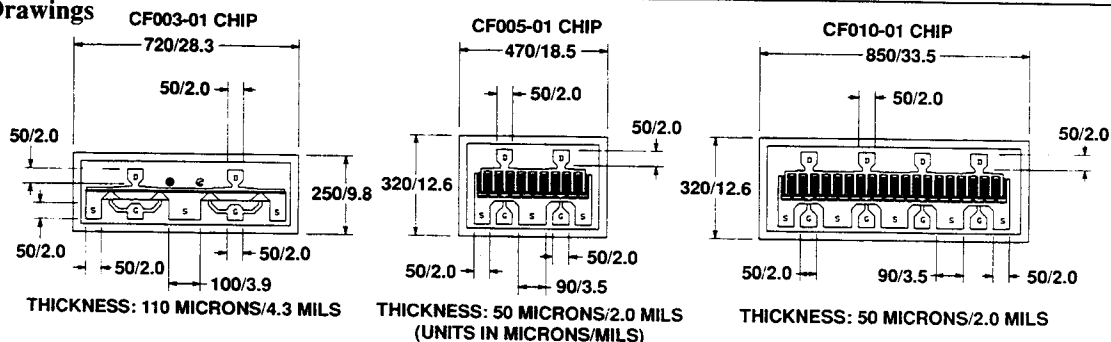
Parameter	Symbol	Ratings
Drain-Source Voltage	V_{DS}	8V
Gate-Source Voltage	V_{GS}	-5V
Drain Current	I_{DS}	I_{DSS}
Continuous Dissipation		
CF003-01	P_T	1.6 W
CF005-01	P_T	3.0 W
CF010-01	P_T	6.0 W
Channel Temperature	T_{CH}	175 $^\circ\text{C}$
Storage Temperature	T_{STG}	-65 $^\circ\text{C}$ to +175 $^\circ\text{C}$

Die Attach and Bonding Procedures

Die Attach: Eutectic die attach is recommended. For eutectic die attach: Preform: AuSn (80% Au, 20% Sn); Stage Temperature: 290 $^\circ\text{C}$, $\pm 5^\circ\text{C}$; Handling Tool: Tweezers; Time: 1 min or less.

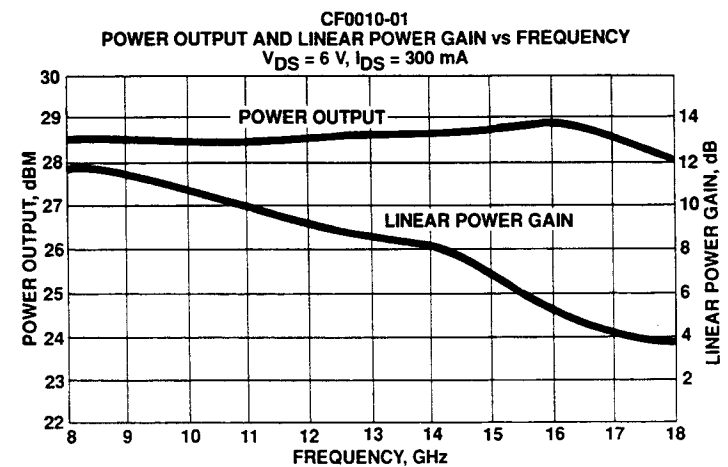
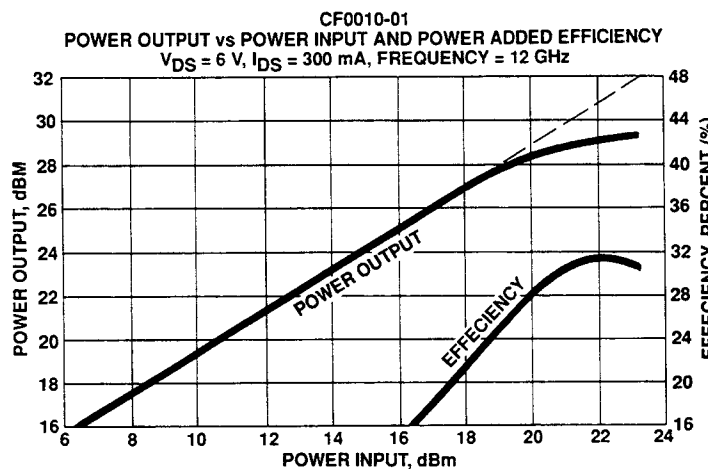
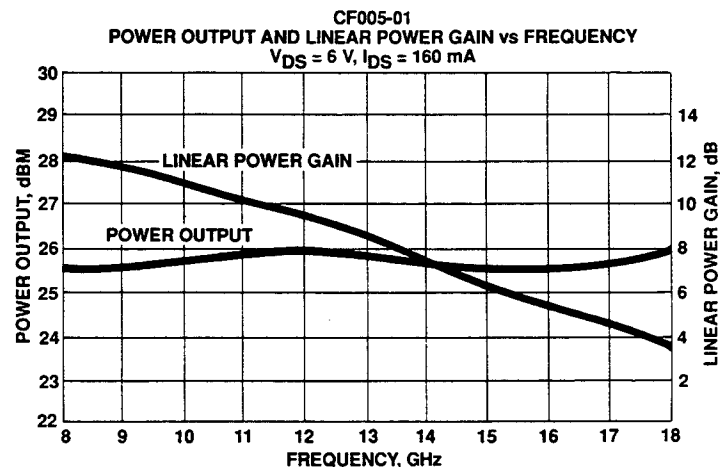
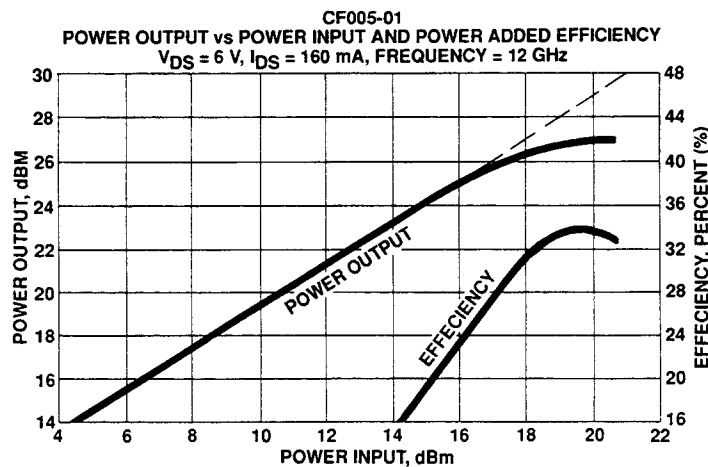
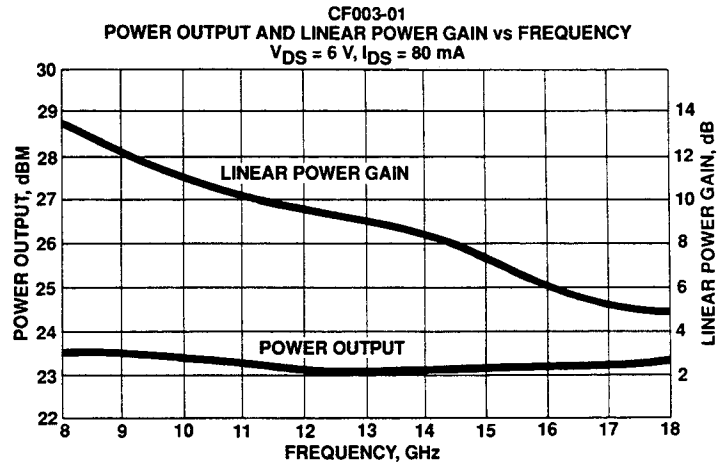
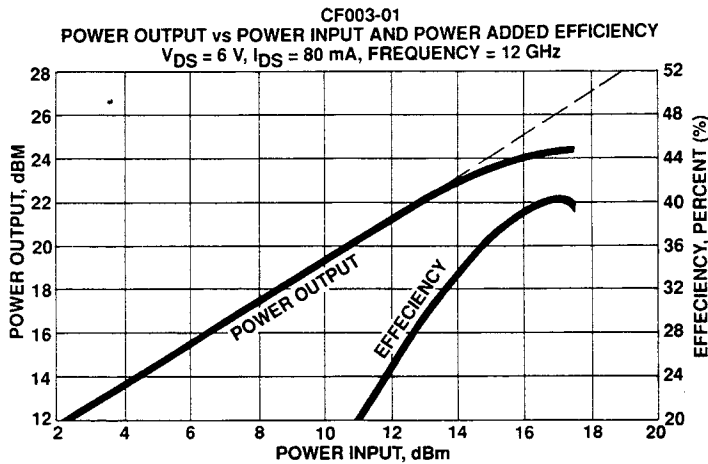
Wire Bonding: Wire Size: 0.7 to 1.0 mil in diameter (pre-stressed); Thermocompression bonding is preferred over thermosonic bonding. For thermocompression bonding: Stage Temperature: 250 $^\circ\text{C}$; Bond Tip Temperature: 150 $^\circ\text{C}$; Bonding Tip Pressure: 18 to 40 gms depending on size of wire.

Chip Outline Drawings

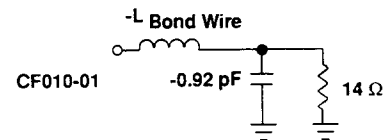
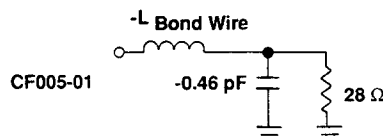
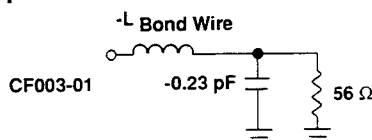


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Typical Performance ($T_A = 25^\circ\text{C}$)



Output Power Match Models



 $V_{DS} = 6 \text{ V}, I_{DS} = 80 \text{ mA}$

CF005-01 at Power Bias

 $V_{DS} = 6 \text{ V}, I_{DS} = 160 \text{ mA}$

CF010-01 at Power Bias

 $V_{DS} = 6 \text{ V}, I_{DS} = 300 \text{ mA}$

Device Model

80% of tested samples must meet specifications for wafer acceptance.

Specifications subject to change.