

9-18GHz Frequency Multiplier

GaAs Monolithic Microwave IC

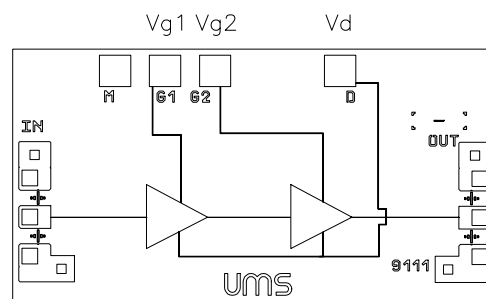
preliminary

Description

The CHX2089 is a cascaded by 2 frequency multiplier monolithic circuit.

It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

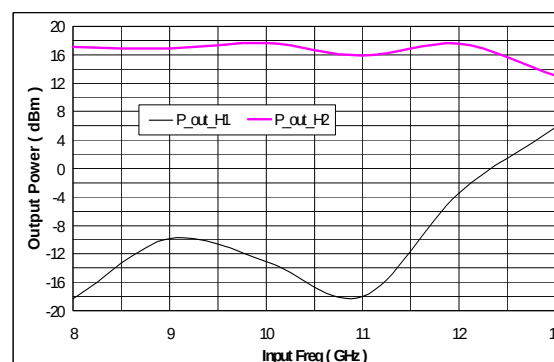
The circuit is manufactured with a PM-HEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.



typical measurement.

Main Features

- Broadband performances : 8-11.5GHz
- 15dBm output power for +12dBm input power
- DC bias : Vd=3.5Volt@Id=60mA
- Chip size : 1.62 x 0.89 x 0.10 mm



Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	8	9	11.5	GHz
Fout	Output frequency range	16	18	23	GHz
Pin	Input power		12	15	dBm
Pout	Output power for +12dBm input power	11	15		dBm

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics

T_{amb} = +25°C, V_d = 3.5V, V_{g1} = -0.9V, V_{g2} adjusted for I_d=50 mA (V_{g2} typ.= -0.3V).

Symbol	Parameter	Min	Typ	Max	Unit
F _{in}	Input frequency range	8	9	11.5	GHz
F _{out}	Output frequency range	16	18	23	GHz
P _{in}	Input power		12	15	dBm
P _{out}	Output power for +12dBm input power	11	15		dBm
I _s /F _o	Fin rejection at the output	15	20		dBc
VSWR _{in}	Input VSWR			2.0:1	
VSWR _{out}	Output VSWR			2.5:1	
I _d	Bias current without RF		40	70	mA
I _d	Bias current with RF (P _{in} =12 dBm)		60	85	mA

Absolute Maximum Ratings

T_{amb.} = 25°C (1)

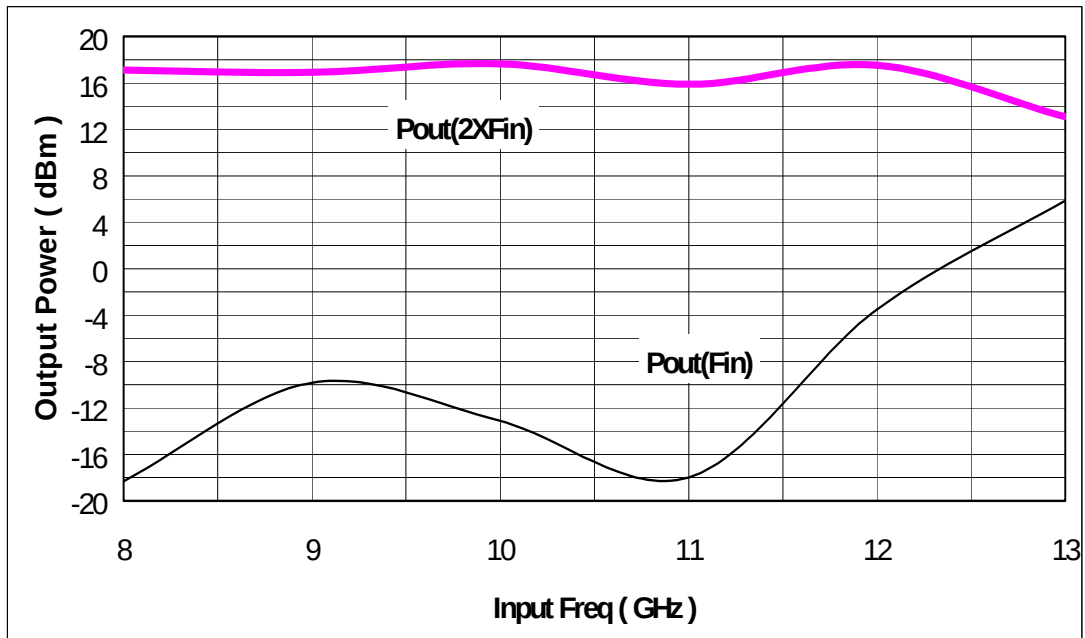
Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4	V
I _d	Drain bias current	90	mA
V _g	Gate bias voltage	-2 to +0.4	V
P _{in}	Input power	20	dBm
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

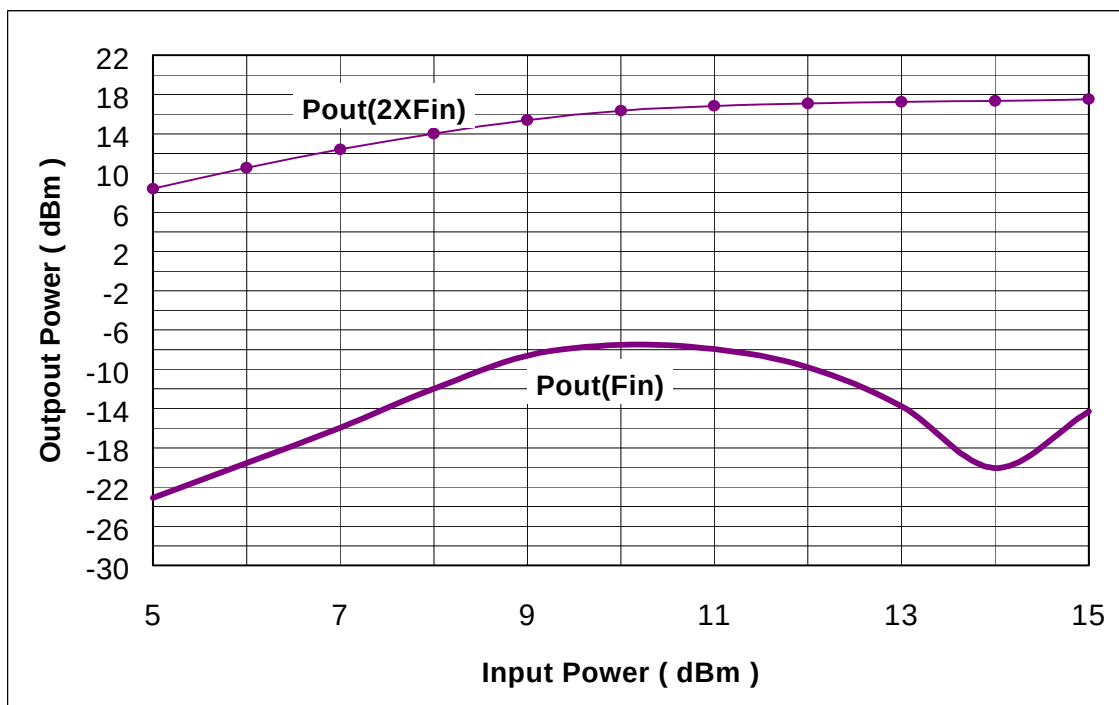
Typical on wafer Measurements.

Bias conditions : $V_d = 3.5V$, $V_{g1} = -0.9V$, $V_{g2} = -0.3V$.

$P_{out} = f(F_{in})$ for $P_{in}=12\text{ dBm}$.

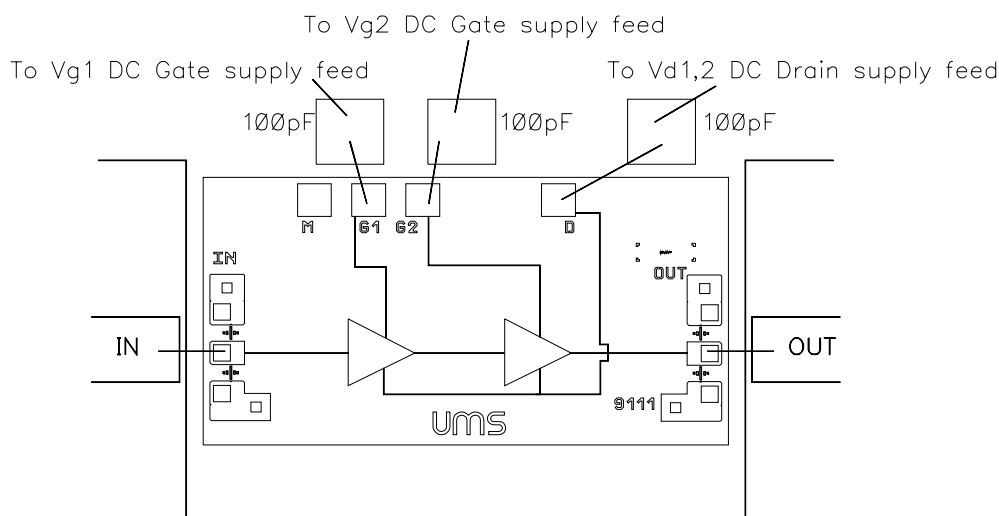


$P_{out} = f(P_{in})$ for $F_{in} = 9\text{ GHz}$.

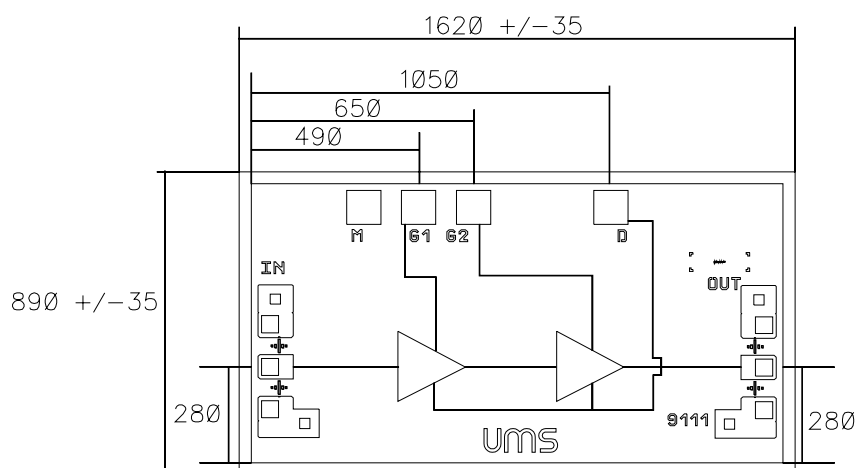


Chip Assembly and Mechanical Data

Vd=3.5V Vg1=-0.9V Vg2=-0.3V.



Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.



Bonding pad positions.

(Chip thickness : 100µm. All dimensions are in micrometers)

Ordering Information

Chip form : CHX2089-99F/00

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Specifications subject to change without notice