Universal Serial Bus Transceiver with Level Translator

Features

- Complies with USB Specification Rev 1.1 & 2.0
- Supports Full Speed Mode (12Mbit/s)
- Integrated 5V to 3.3V regulator
- Bi-directional driver input/output pins
- Two single-ended receivers with hysteresis
- USB detection of V_{BUS} via level translator
- Stable RCV output during SE0 condition
- Low power operation
- Supports 1.65 to 3.6V I/O voltage levels
- Full industrial operating range -40 to 85°C
- Available in tiny HBCC-16 and TQFN-16 packages
- Lead-free versions available

Applications

- Wireless Handsets
- Digital Still Cameras
- PDAs (Personal Digital Assistants)
- IAs (Information Appliances)
- Pin and functionally compatible with Philips ISP1102

Product Description

The CM2400-05 Universal Serial Bus (USB) transceiver is fully compliant with USB specification, revisions 1.1 and 2.0. It supports a speed of 12Mbits/s (Full Speed Mode).

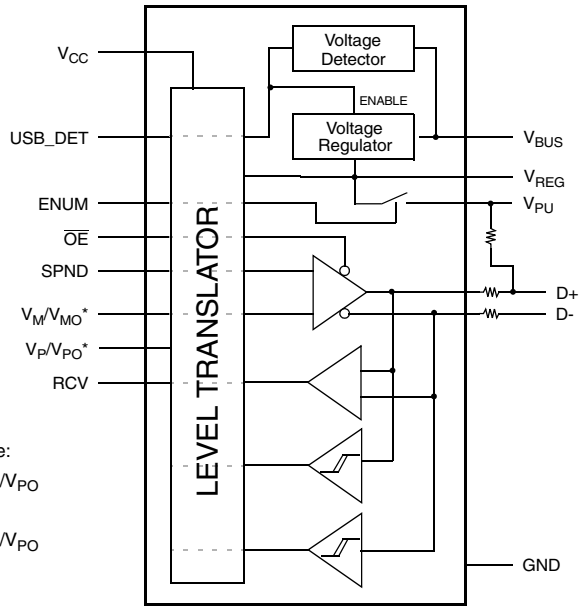
An internal level shifter allows interface to Application Specific Integrated Circuits (ASICs) and Programmable Logic Devices (PLDs) running at core voltages of 1.65V to 3.6V.

An internal 5V to 3.3V regulator is used to power the CM2400-05 USB transceiver via the USB supply V_{BUS}. V_M/V_{MO} and V_P/V_{PO} are bi-directional interface pins. In one mode they function as the differential driver input data. In another mode they function as the output of the single ended receivers. This mode is configured by the $\overline{OE}$ pin.

This device is ideal for portable electronic devices such as mobile phones, digital still cameras, PDAs (Personal Digital Assistants) and IAs (Information Appliances).

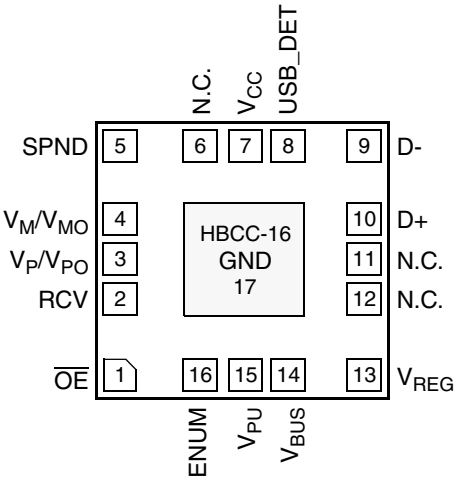
The CM2400-05 is manufactured in small form-factor 16-lead HBCC or TQFN packages to conserve board space and is available with optional lead-free finishing.

Simplified Block Schematic

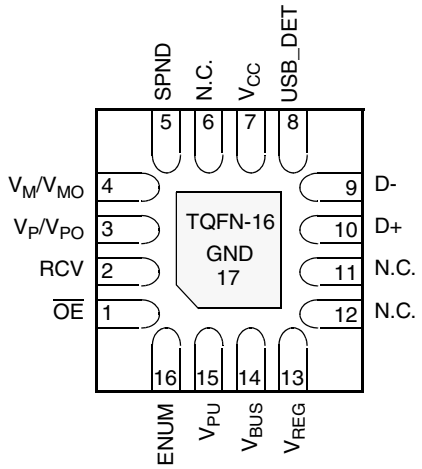


* Pins are bi-directional based on $\overline{OE}$ state:
If $\overline{OE}$ = V_{CC}, then V_M/V_{MO} and V_P/V_{PO} are configured as outputs.
If $\overline{OE}$ = GND, then V_M/V_{MO} and V_P/V_{PO} are configured as inputs.

PACKAGE / PINOUT DIAGRAM



HBCC16 Package
Bottom View



TQFN16 Package
Bottom View

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PINS	NAME	DESCRIPTION
1	$\overline{OE}$	Input for Output Enable (Active low). Enables transceiver driver to transmit data on the USB bus. When $\overline{OE}$ pin = LOW, driver circuitry is enabled.
2	RCV	Differential receiver output of D+ and D- input data lines. The output state of RCV is preserved and stable during an SE0 condition.
3	V_P/V_{PO}	Bi-directional input output of D+. Configured by $\overline{OE}$.
4	V_M/V_{MO}	Bi-directional input output of D-. Configured by $\overline{OE}$.
5	SPND	Suspend input. Allows the device to enter a low power state while the USB is inactive.
6	N.C.	No internal connection to circuitry.
7	V_{CC}	Supply voltage for digital I/O pins. Voltages supported: 1.65 to 3.3V.
8	USB_DET	I/O level USB detect output. Logic High indicates that a USB cable is present.
9	D-	Negative USB data connection.
10	D+	Positive USB data connection. In full-speed connect mode, connect to V_{PU} via a 1.5kΩ resistor. Tolerance of this resistor is defined in the USB specification REV 1.1 & 2.0
11	N.C.	No internal connection to circuitry.
12	N.C.	No internal connection to circuitry.
13	V_{REG}	Regulated supply voltage output during USB operation of V_{BUS}. 1µF decoupling capacitor is required.
14	V_{BUS}	Supply voltage input. Can be directly connected to USB V_{BUS}.
15	V_{PU}	Pull-up supply voltage. Pin function is controlled by input ENUM.
16	ENUM	Enumerate, allows software to control connection of the external pull-up via the level translator. If ENUM = LOW then V_{PU} is floating. If ENUM = HIGH then V_{PU} is internally connected to V_{REG}.
17	GND	The ground terminal is connected to the exposed diepad (heatsink)

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish[3]	
Pads/Pins[1]	Package	Ordering Part Number[2]	Part Marking	Ordering Part Number[2]	Part Marking
16	HBCC-16	CM2400-05HB	CM240 005HB	CM2400-05HA	CM240 005HA
16	TQFN-16	CM2400-05QF	CM240 005QF	CM2400-05QE	CM240 005QE

Note 1: There is one additional GND pad on the bottom of the device not included in this pin count.
Note 2: Parts are shipped in Tape & Reel form unless otherwise specified.
Note 3: Lead-free, 100% tin plated.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD Protection (HBM, All Pins, See Note 1)	±2000	V
V_{BUS}	[GND - 0.5] to +5.5	V
V_{CC}	[GND - 0.5] to +6.0	V
V_I (INPUT)	[GND - 0.5] to [V_{CC} + 0.5]	V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Junction	-40 to +150	°C

Note 1: Equivalent to discharging a 100pF capacitor via a 1.5kΩ resistor (Human Body Model).

STANDARD (RECOMMENDED) OPERATING CONDITIONS					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{BUS}	USB V_{BUS} Supply	4.1	5.0	5.5	V
V_{CC}	DC System Supply	1.65	3.3	3.6	V
V_I	DC Input Voltage	0	-	V_{CC}	V
$V_{I(AI/O)}$	Analog I/O Pins (D+, D-)	0	-	3.6	V
T_A	Ambient Operating Temperature Range	-40	-	85	°C

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

Static Operating Characteristics

Supply Pins (V_{BUS} = 4.1V to 5.5V; V_{CC} = 1.65V to 3.6V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REG}	Regulated supply output	Unloaded	3.0	3.3	3.6	V
I_{BUS}	Operating supply current	Full-speed TX and RX; C_L=50pF on D+/D- outputs			10	mA
$I_{BUS(IDLE)}$	Supply current during full speed idle and SE0	Full-speed idle; Note 2			500	µA
$I_{BUS(SUSP)}$	Supply current during suspend	SPND = logic "1"; Note 2			100	µA
I_{CC}	Operating I/O supply current	Full-speed TX and RX			2.0	mA
$I_{CC(STAT)}$	Static I/O supply current	Full-speed idle, SE0 or suspend			10.0	µA
$I_{CC(SHARE)}$	Supply current during sharing mode	V_{BUS} not connected			10.0	µA
$I_{DX(SHARE)}$	D+/D- load current during sharing mode	V_{BUS} not connected; ENUMERATE = logic "0"			10.0	µA
$V_{TH(VBUS)}$	V_{BUS} supply detection threshold, USB_D output	Supply lost (USB_D low)			3.6	V
		Supply present	4.1			V
		$V_{TH(BUS)}$ Hysteresis		100		mV
$V_{TH(VCC)}$	V_{CC} supply detection threshold.	Supply lost			0.5	V
		Supply present	1.4			V
		$V_{TH(VCC)}$ Hysteresis		200		mV

Digital Pins (V_{BUS} = 4.1V to 5.5V; V_{CC} = 1.65V to 3.6V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Logic LOW input voltage				0.3 X V_{CC}	V
V_{IH}	Logic HIGH input voltage		0.6 X V_{CC}			V
V_{OL}	Logic LOW output voltage	I_{OL} = 100µA I_{OL} = 2mA			0.15 0.40	V V
V_{OH}	Logic HIGH output voltage	I_{OH} = 100µA I_{OH} = 2mA	V_{CC} - 0.15 V_{CC} - 0.40			V V

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Note 2: Excluding any load current and V_{PU}/V_{SW} source current to 1.5kΩ and 15kΩ pull-up and pull-down resistors (200 µA).

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (CONT'D)

Static Operating Characteristics (cont'd)

Analog I/O Pins (V_{BUS} = 4.1V to 5.5V; V_{CC} = 1.65V to 3.6V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DI}	Differential receiver input sensitivity	$\lvert V_I(D+) - V_I(D-) \rvert$	0.2			V
V_{CM}	Differential receiver common mode voltage		0.8		2.5	V
V_{IL}	Single-ended receiver logic LOW input voltage	$\overline{OE}$ = logic "1"			0.8	V
V_{IH}	Single-ended receiver logic HIGH input voltage	$\overline{OE}$ = logic "1"	2.0			V
V_{HYS}	Single-ended receiver Hysteresis voltage	$\overline{OE}$ = logic "1"	0.4		0.7	V
V_{OL}	Logic LOW output voltage	R_L = 1.5kΩ tied to +3.6V			0.3	V
V_{OH}	Logic HIGH output voltage	R_L = 15kΩ tied to GND	2.8		3.6	V
I_{LZ}	OFF-state leakage current				±1	µA
C_{IN}	Transceiver Capacitance	Pin to GND		10		pF
R_{SW}	Internal switch resistance at V_{PU}			30		Ω
Z_{DRV}	Driver output impedance (includes 33 ohm 1% resistor)	Measured with steady-state drive; See Note 3	33	39	44	Ω

Dynamic Operating Characteristics:

Analog I/O Pins (VBUS = 4.1 to 5.5V; VCC = 1.65 to 3.6V)

Driver Characteristics & Timings (Full-speed mode only)

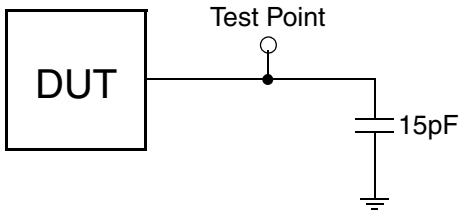
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{FR}	Rise time	C_L = 50 to 125pF, measured 10% to 90% (V_{OH}-V_{OL}); See Figure 6	4		20	ns
t_{FF}	Fall time	C_L = 50 to 125pF, measured 10% to 90% (V_{OH}-V_{OL}); See Figure 6	4		20	ns
FRFM	Differential rise / fall time matching (t_{FR}/t_{FF})	Excluding the first transition from idle state	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle state; See Figure 9	1.3		2.0	V
$t_{PLH(DRV)}$	Driver propagation delay (V_O/V_{PO} ➔ D+/D-, FSEO/V_{MO} ➔ D+/D-	LOW-to-HIGH transition; See Figure 9			18	ns
$t_{PHL(DRV)}$		HIGH-to-LOW transition; See Figure 9			18	ns
t_{PHZ}	Driver disable delay ($\overline{OE}$ ➔ D+/D-)	HIGH-to-OFF; See Figure 7			18	ns
t_{PLZ}		LOW-to-OFF; See Figure 7			18	ns
t_{PZH}	Driver enable delay ($\overline{OE}$ ➔ D+/D-)	OFF-to-HIGH; See Figure 7			15	ns
t_{PZL}		OFF-to-LOW; See Figure 7			15	ns

Note 3: Rev 2.0 states Z_{DRV} must be between 28Ω and 44Ω, when the driver is not high speed capable.

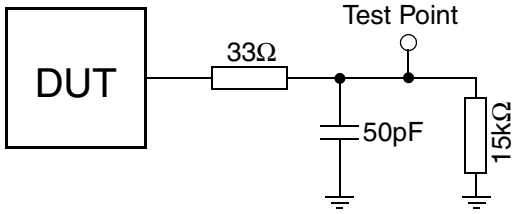
Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (CONT'D)						
Dynamic Operating Characteristics: (cont'd) **Analog I/O Pins (VBUS = 4.1 to 5.5V; VCC = 1.65 to 3.6V)**						
Receiver Timings (Full-speed mode only)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Differential Receiver						
$t_{PLH(RCV)}$	Driver propagation delay (D+/D- ➔ RCV)	LOW-to-HIGH transition; See Figure 8			15	ns
$t_{PHL(RCV)}$		HIGH-to-LOW transition; See Figure 8			15	ns
Single-ended Receiver						
$t_{PLH(SE)}$	Driver propagation delay (D+/D- ➔ V_P, V_M)	LOW-to-HIGH transition; See Figure 8			15	ns
$t_{PHL(SE)}$		HIGH-to-LOW transition; See Figure 8			15	ns

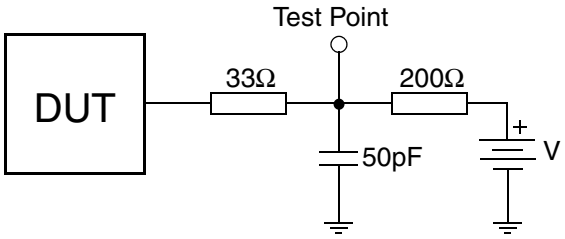
Test Loads



Load for V_P,V_M and RCV delay measurements



Load for D+ and D- delay measurements (Max and Min Timing)



$V = V_{REG}(3.3)$ for t_{PZL} and t_{PLZ}
$V = 0$ v for t_{PZH} and t_{PHZ}

Load for ENABLE and DISABLE delay measurements.

Performance Information

CM2400-05 Typical DC Characteristics (nominal conditions unless specified otherwise)

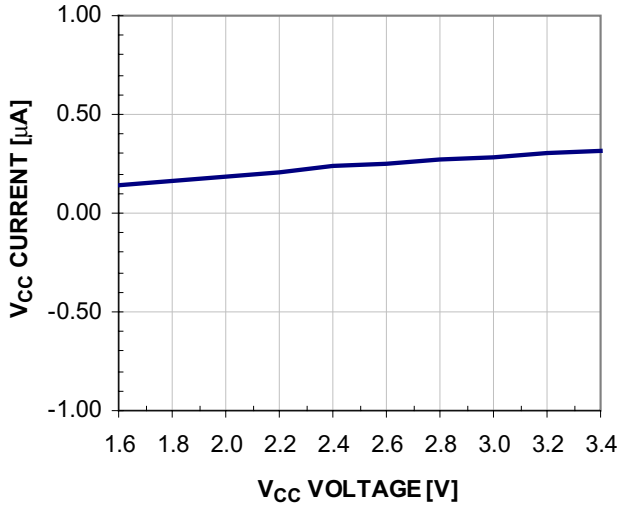


Figure 1. V_{CC} Current in Idle Mode (SPND=LOW)

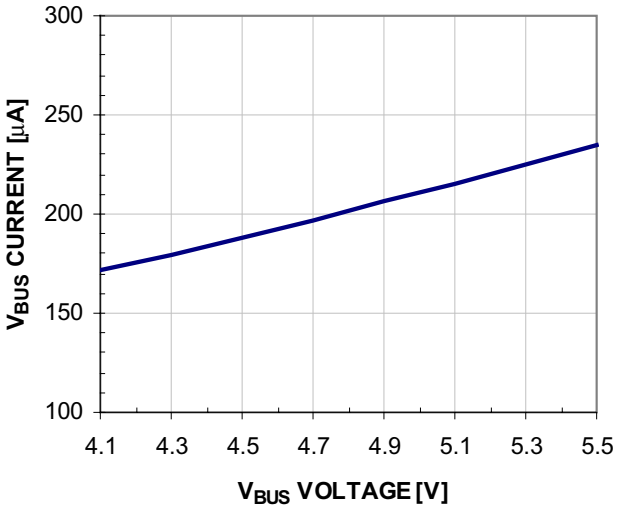


Figure 3. V_{BUS} CURRENT in Idle Mode (SPND=LOW)

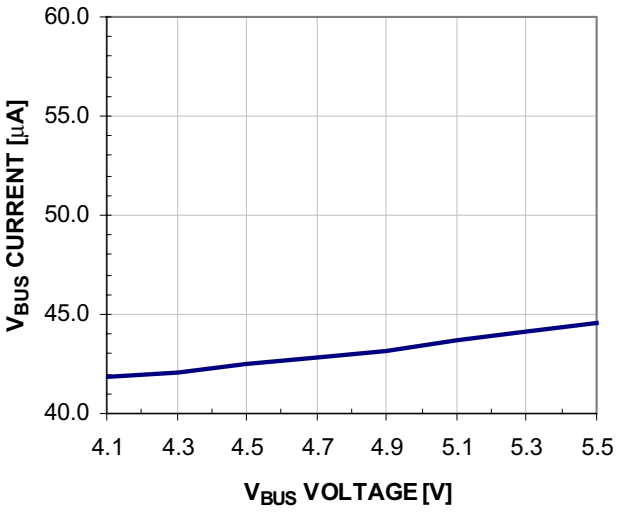


Figure 2. V_{BUS} Current in Suspend Mode (SPND=HIGH)

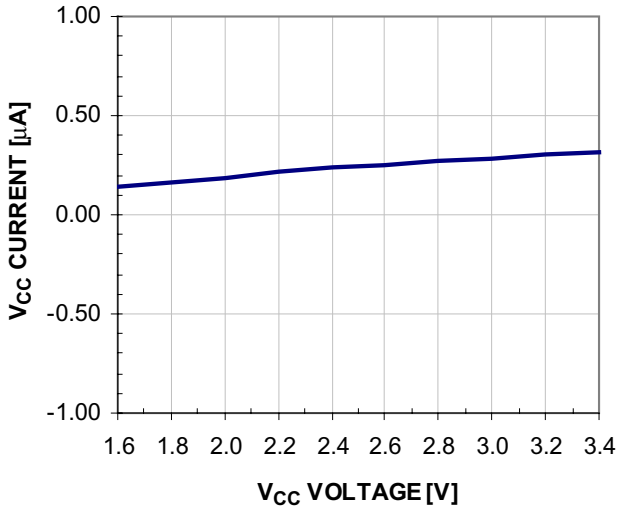


Figure 4. V_{CC} Current in Suspend Mode (SPND=HIGH)

Performance Information (cont'd)

CM2400-05 Typical AC Characteristics (nominal conditions unless specified otherwise)

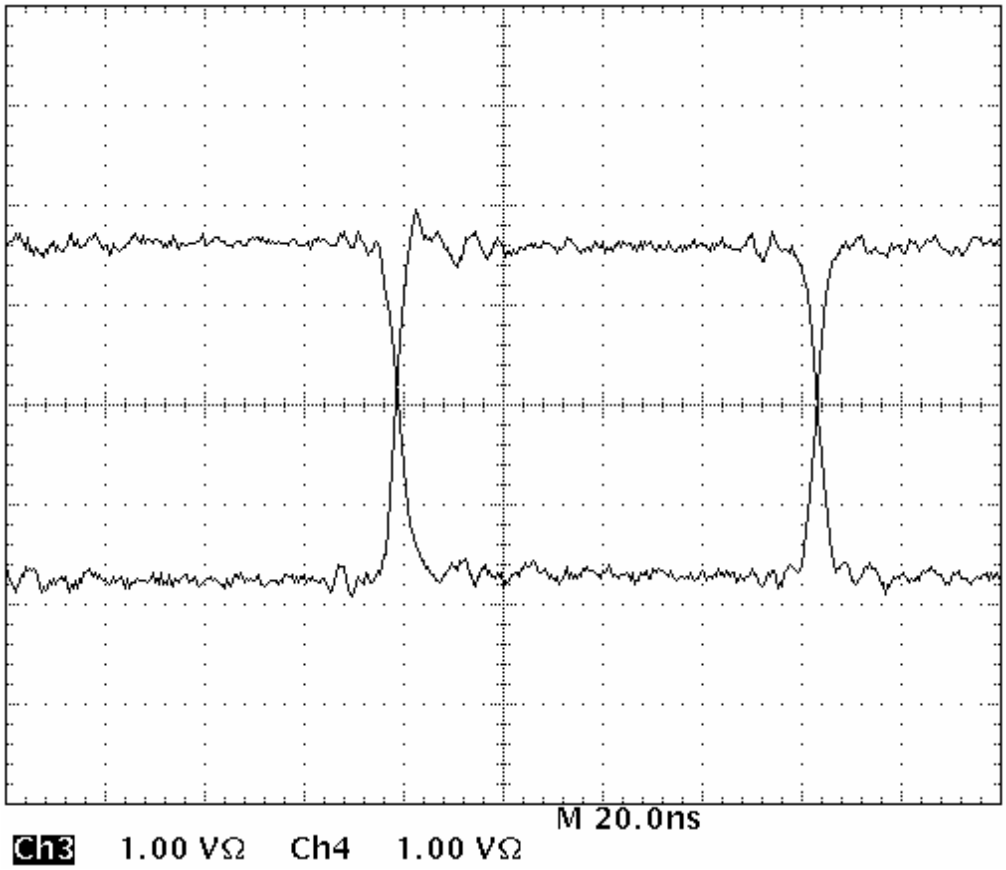


Figure 5. Rise and Fall Time Matching for Full-Speed Mode

Performance Information (cont'd)

CM2400 Timing Diagrams

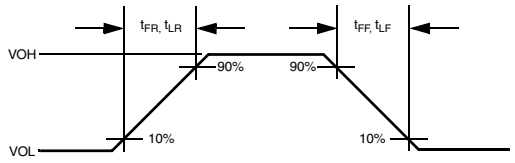


Figure 6. Rise and Fall Timing

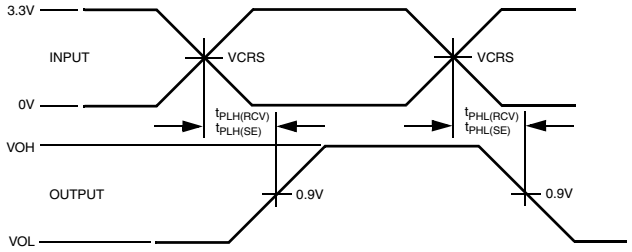


Figure 8. D+, D- to RCV, V_P and V_M Timing

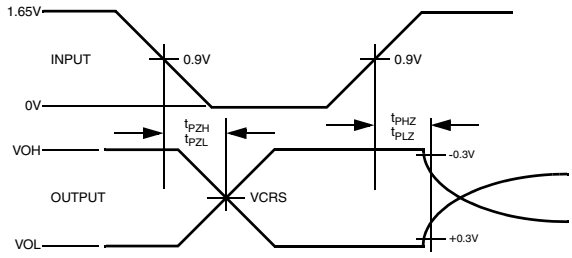


Figure 7. $\overline{OE}$ to D+, D- Timing

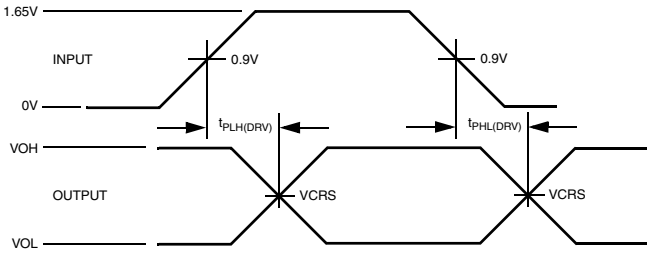


Figure 9. V_O/V_{PO}, FSEO/V_{MO} to D+, D- Timing

Functional Description

The CM2400-05 USB Transceiver supports 3 different power supply configurations, which can be configured dynamically. Table 1 details the various configurations. In **Normal Mode** the internal regulator produces 3.3V from V_{BUS} to power the internal drivers and receivers associated with the USB protocol.

V_{BUS}	V_{CC}	CONFIGURATION
Connected	Connected	Normal Mode
Connected	Not Connected	Disable Mode
Not Connected	Connected	Sharing Mode

Table 1: Power Supply Connections

In **Disable** and **Sharing Mode**, all input/output pins follow the states defined in Table 2. In Sharing mode, D+, D- and V_{PU} can have voltages higher then V_{CC}. This allows other external signals to share D+ and D- while USB signaling is disabled.

PIN	Sharing Mode State	Disable Mode State
V_{BUS}	V_{BUS} < 3.6V	4.1V to 5.5V
V_{REG}	Pulled Down	3.3V Out
V_{CC}	Present	Not Present
V_{PU}	High-Z (off)	High-Z (off)
D+, D-	High-Z	High-Z
V_P/V_{PO}, V_M/V_{MO}	H	Invalid
RCV	L	Invalid
USB_DET	L	Invalid
Inputs	High-Z	High-Z

Table 2: Pin States in Disable or Sharing Mode

Table 3 lists the functions of the modes associated with suspend and $\overline{OE}$ pins. When Suspend is low and $\overline{OE}$ is high, signal levels on D+ and D- are determined by other USB devices and pull-up/down resistors. In **Suspend Mode** (SPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out of suspend signaling is detected via the single-ended receivers V_P and V_M. During suspend and while the output is still enabled ($\overline{OE}$ = LOW), D+ and D- lines are driven to their intended states. This is permitted because driving during suspend is used to signal remote wake-up by driving a 'K' signal for a period of 1 to 15ms.

SUSPEND	$\overline{OE}$	D+ / D-	RCV	V_P/V_{PO},V_M/V_{MO}	Function
L	L	Driver & Receiver Active	Active	Input	Normal driving mode. Differential receiver active
L	H	Receiving	Active	Output	Driver Tri-stated. Differential receiver active.
H	L	Driving	Inactive RCV=L	Input	Driving during 'suspend'. Differential receiver inactive.
H	H	High-Z	Inactive RCV=L	Output	Low-power state.

Table 3: Function Selection.

Functional Description (cont'd)

Detailed in Table 4 is the differential result for all variations on V_P/V_{PO} and V_M/V_{MO}.

V_P/V_{PO}	V_M/V_{MO}	Result
L	L	Logic '0'
L	H	SE0
H	L	Logic '1'
H	H	SE0

Table 4: Operating Mode ($\overline{OE}$ = L)

Table 5 details the receiving function when $\overline{OE}$ is HIGH (driver disabled). RCV denotes the signal level on the output RCV just before an SE0 state occurs. This level is stable during the SE0 period.

D+/D-	RCV	V_P	V_M
Differential Logic '0'	L	L	H
Differential Logic '1'	H	H	L
SE0	RCV*	L	L

Table 5: Receiving Function (SPND = L)

Note 1: Denotes RCV is stable in last state before SE0 condition.

Detection of a V_{BUS} voltage is accomplished via an internal Comparator with hysteresis. The output from this Comparator is fed via the level translator to ensure compatibility with processor core voltages and output to pin USB_DET. When V_{BUS} is over 4.1 volts USB_DET is HIGH. When V_{BUS} is under 3.6 volts USB_DET is LOW.

The CM2400-05 USB transceiver includes an enumeration pin (ENUM) which internally connects V_{PU} to V_{REG} when enabled. This allows a processor running at a core voltage different than 3.3V to switch the pull-up resistor in and out without the need for external circuitry.

Mechanical Details

The CM2400-05 is available in both 16-pin HBCC and 16-lead TQFN packages.

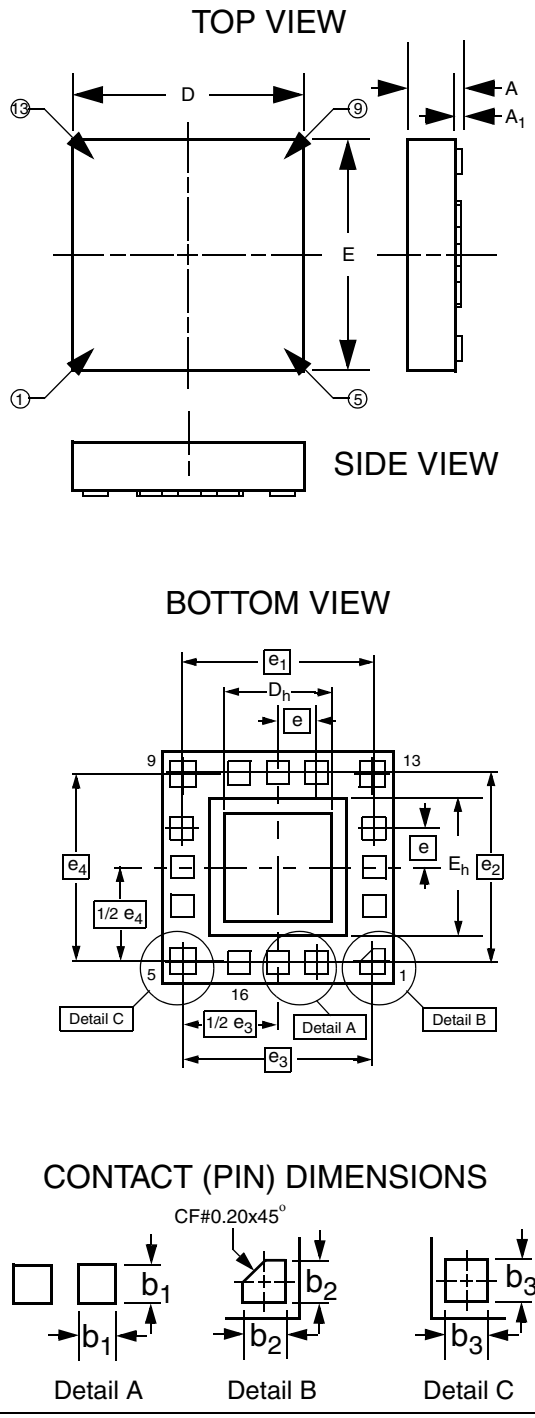
HBCC16 Mechanical Specifications

Dimensions for CM2400-05 devices packaged in 16-pin HBCC packages are presented below.

PACKAGE DIMENSIONS				
Package	HBCC-16			
Pins	16			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	-	0.80		0.0315
A_1	0.05	0.10		0.0039
b_1	0.25	0.35		0.0138
b_2	0.30	0.40		0.0157
b_3	0.30	0.40		0.0157
D	2.90	3.10		0.1220
D_h	1.45	1.55		0.0610
E	2.90	3.10		0.1220
E_h	1.75	1.85		0.0728
e	0.50 TYP.		0.0197 TYP.	
e_1	2.50 TYP.		0.0984 TYP.	
e_2	2.50 TYP.		0.0984 TYP.	
e_3	2.45 TYP.		0.0965 TYP.	
e_4	2.45 TYP		0.0965 TYP.	
# per tube	120 pieces*			
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Dimensions for HBCC16 Package

Mechanical Details (cont'd)

TQFN-16 Mechanical Specifications

Dimensions for CM2400-05 devices packaged in 16-lead TQFN packages are presented below.

For complete information on the TQFN-16 package, see the California Micro Devices TQFN Package Information document.

PACKAGE DIMENSIONS						
Package	TQFN					
Leads	16					
Dim.	**Millimeters**			**Inches**		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80	.028	.030	.031
A1	0.00	0.02	0.05	0.00	.001	.002
A3	0.20 REF			.008		
b	0.20	0.25	0.30	.008	.010	.012
D	2.9	3.0	3.1	.114	.118	.122
D1	1.50 REF			.059 REF		
D2	1.00	1.10	1.20	.039	.043	.047
E	2.9	3.0	3.1	.114	.118	.122
E1	1.50 REF			.059 REF		
E2	1.00	1.10	1.20	.039	.043	.047
e	0.50 TYP.			.020 TYP.		
L	0.30	0.40	0.50	.012	.016	.020
# per tube	120 pieces*					
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

* This is an approximate number which may vary.

Mechanical Package Diagrams

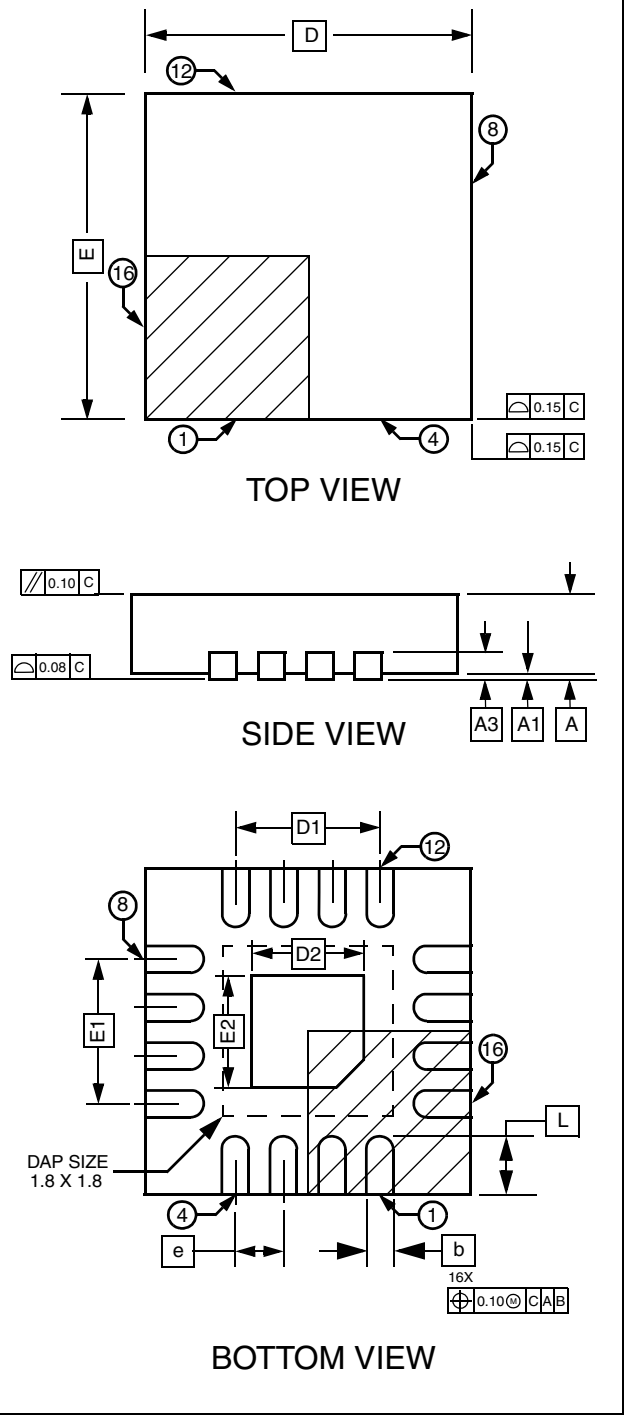


Figure 10. Dimensions for 16-Lead TQFN Package