

## 30 W Quad Half-Bridge Digital Amplifier Power Stage

### Features

- ◆ Configurable Outputs (10% THD+N)
  - 2 x 15 W into 8  $\Omega$ , Full-Bridge
  - 1 x 30 W into 4  $\Omega$ , Parallel Full-Bridge
  - 4 x 7 W into 4  $\Omega$ , Half-Bridge
  - 2 x 7 W into 4  $\Omega$ , Half-Bridge + 1 x 15 W into 8  $\Omega$ , Full-Bridge
- ◆ Space-Efficient Thermally-Enhanced QFN
  - No External Heat Sink Required
- ◆ > 100 dB Dynamic Range - System Level
- ◆ 0.1% THD+N @ 1 W - System Level
- ◆ Built-In Protection with Error Reporting
  - Over-current
  - Thermal Warning and Overload
  - Under-voltage
- ◆ +9 V to +18 V High Voltage Supply
- ◆ PWM Popguard® for Quiet Startup
- ◆ High Efficiency (85%)
- ◆ Low  $R_{DS(ON)}$
- ◆ Low Quiescent Current
- ◆ Low Power Standby Mode

### Common Applications

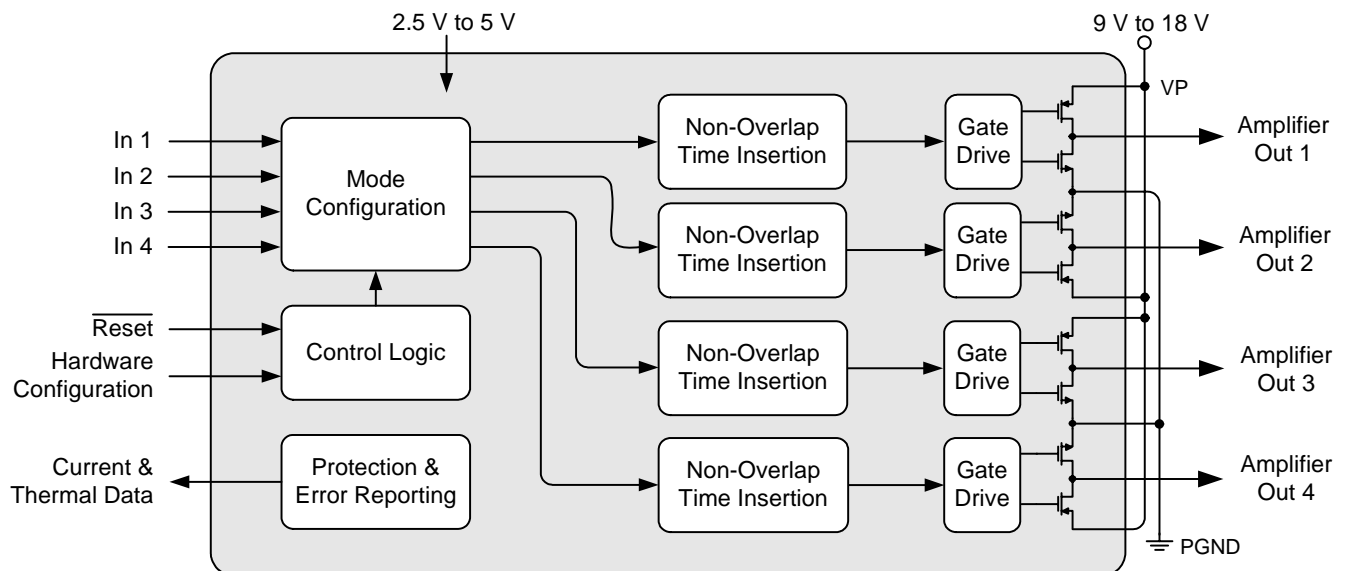
- ◆ Integrated Digital Televisions
- ◆ Portable Docking Stations
- ◆ Mini/Micro Shelf Systems
- ◆ Powered Desktop Speakers

### General Description

The CS4412 is a high-efficiency power stage for digital Class-D amplifiers designed to input PWM signals from a modulator such as the CS4525. The power stage outputs can be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS4412 integrates on-chip over-current, under-voltage, over-temperature protection and error reporting as well as a thermal warning indicator. The low  $R_{DS(ON)}$  outputs can source up to 2.4 A peak current, delivering 85% efficiency. This efficiency provides for a small device package and lower power supplies.

The CS4412 is available in a 48-pin QFN package in Commercial grade (-40 to +70° C). The CRD4412 customer reference design is also available. Please refer to "Ordering Information" on page 22 for complete ordering information.



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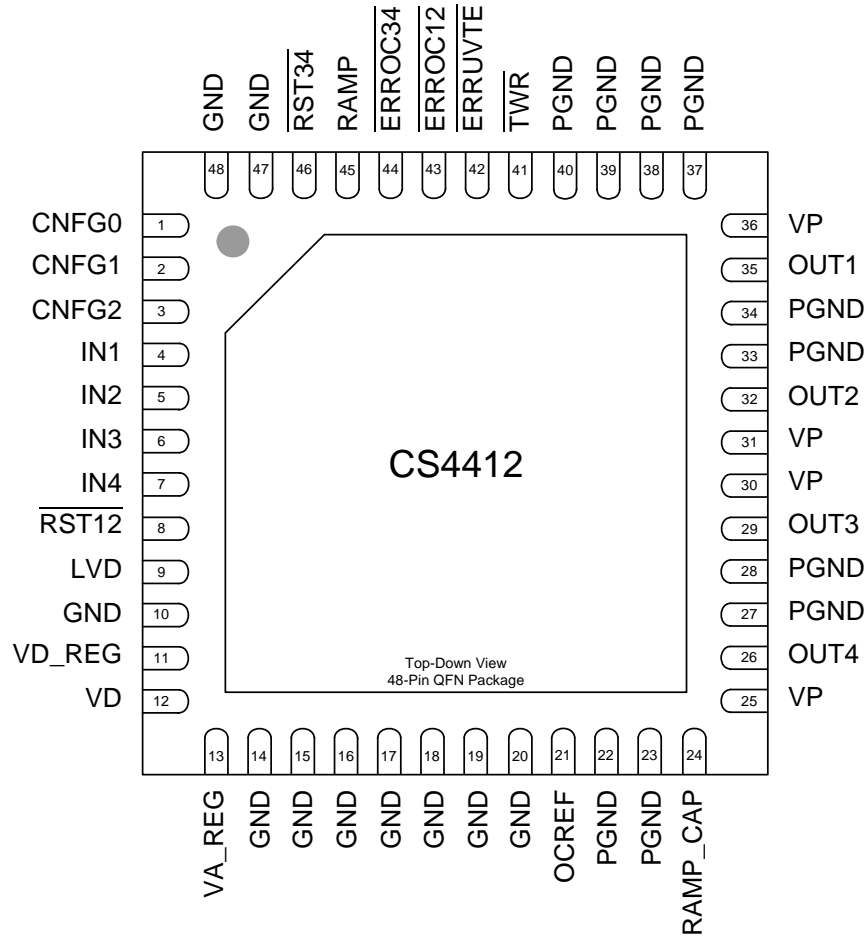
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# 1. PIN DESCRIPTION



Pin Name	Pin #	Pin Description
CNFG0	1	<b>Out Configuration Select (Input)</b> - Used to set the PWM output configuration mode. See <a href="#">“Output Mode Configuration”</a> on page 14.
CNFG1	2	
CNFG2	3	
IN1	4	<b>PWM Input (Input)</b> - Inputs from a PWM modulator.
IN2	5	
IN3	6	
IN4	7	
RST1/2 RST3/4	8 46	<b>Reset Input (Input)</b> - Reset inputs for channels 1/2 and 3/4 respectively. Active low.
LVD	9	<b>VD Voltage Level Indicator (Input)</b> - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be GND.
VD_REG	11	<b>Core Digital Power (Output)</b> - Filter connection for the internally generated power supply for the low voltage digital circuitry.
VD	12	<b>Digital Power (Input)</b> - Low voltage power supply for internal logic.
VA_REG	13	<b>Core Analog Power (Output)</b> - Filter connection for internally generated power supply for the low voltage analog circuitry

Pin Name	Pin #	Pin Description
OCREF	21	<b>Over-current Reference (Input)</b> - Sets over-current trip level. Connect pin through a resistor to GND. See <a href="#">"Device Protection and Error Reporting" on page 17</a> . This pins should not be left floating.
RAMP_CAP	24	<b>Output Ramp Capacitor (Input)</b> - Sets the output ramp time for half-bridge configured outputs.
GND	10,14 15,16 17,18 19,20 47,48	<b>Ground (Input)</b> - Ground for the internal logic and I/O. These pins should be connected to the common system ground.
VP	25,30 31,36	<b>High Voltage Output Power (Input)</b> - High voltage power supply for the individual output power half-bridge devices.
PGND	22,23 27,28 33,34 37,38 39,40	<b>Power Ground (Input)</b> - Ground for the individual output power half-bridge devices. These pins should be connected to the common system ground.
OUT4 OUT3 OUT2 OUT1	26 29 32 35	<b>PWM Output (Output)</b> - Amplified PWM power half-bridge outputs.
$\overline{\text{TWR}}$	41	<b>Thermal Warning Output (Output)</b> - Thermal warning output. Open drain, active low. See <a href="#">"Device Protection and Error Reporting" on page 17</a> .
$\overline{\text{ERRUVTE}}$	42	<b>Thermal and Under-voltage Error Output (Output)</b> - Error flag for thermal shutdown and under-voltage. Open drain, active low. See <a href="#">"Device Protection and Error Reporting" on page 17</a> .
$\overline{\text{ERROC1/2}}$	43	<b>Over-current Error Output (Output)</b> - Over-current error flag for the associated outputs. Open drain, active low. See <a href="#">"Device Protection and Error Reporting" on page 17</a> .
$\overline{\text{ERROC3/4}}$	44	
RAMP	45	<b>Ramp-up/down Select (Input)</b> - Set high to enable ramping. When set low, ramping is disabled. See <a href="#">"PWM Popguard Transient Control" on page 13</a> .

## 2. CHARACTERISTICS AND SPECIFICATIONS

### RECOMMENDED OPERATING CONDITIONS

GND=PGND=0 V, all voltages with respect to ground.

Parameters	Symbol	Min	Nom	Max	Units	
<b>DC Power Supply</b>						
Digital and Analog Core	VD	2.375	2.5	2.625	V	
	VD	3.135	3.3	3.465	V	
	VD	4.75	5.0	5.25	V	
Power Stage	VP	8.1		19.8	V	
<b>Temperature</b>						
Ambient Temperature	Commercial	T <sub>A</sub>	-40	-	+70	°C
Junction Temperature		T <sub>J</sub>		-	+150	°C

### ABSOLUTE MAXIMUM RATINGS

GND = PGND = 0 V; all voltages with respect to ground. (Note 1)

Parameters	Symbol	Min	Max	Units	
<b>DC Power Supply</b>					
Power Stage	Outputs Switching and Under Load	VP	-0.3	19.8	V
Power Stage	No Output Switching	VP	-0.3	23.0	V
Digital and Analog Core	(Note 2)	VD	-0.3	6.0	V
<b>Inputs</b> (Note 2)					
Input Current	(Note 3)	I <sub>in</sub>	-	±10	mA
Digital Input Voltage	(Note 4)	V <sub>IND</sub>	-0.3	VD + 0.4	V
<b>Temperature</b> (Note 2)					
Ambient Operating Temperature - Power Applied	Commercial	T <sub>A</sub>	-40	+85	°C
Storage Temperature		T <sub>stg</sub>	-65	+150	°C

- Notes:**
1. Operation beyond these limits may result in permanent damage to the device.
  2. Normal operation is not guaranteed at these extremes.
  3. Any pin except supplies. Transient currents of up to ±100 mA on the PWM input pins will not cause SCR latch-up.
  4. The maximum over/under voltage is limited by the input current.

## PWM POWER OUTPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): GND = PGND = 0 V; All voltages with respect to ground;  $T_A = 25^\circ\text{C}$ ;  $V_D = 3.3\text{ V}$ ;  $V_P = 18\text{ V}$ ;  $R_L = 8\ \Omega$  for full-bridge,  $R_L = 4\ \Omega$  for half-bridge and parallel full-bridge; PWM Switch Rate = 384 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Input source is CS4525 PWM\_SIG outputs; Performance measurements taken with a full scale 997 Hz sine wave and AES17 filter.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Output per Channel						
Stereo Full-Bridge	$P_O$	THD+N < 10%	-	15	-	W
		THD+N < 1%	-	12	-	W
Half-Bridge		THD+N < 10%	-	7	-	W
		THD+N < 1%	-	5.5	-	W
Parallel Full-Bridge		THD+N < 10%	-	30	-	W
		THD+N < 1%	-	23.5	-	W
Total Harmonic Distortion + Noise						
Stereo Full-Bridge	THD+N	$P_O = 1\text{ W}$	-	0.1	-	%
		$P_O = 0\text{ dBFS} = 11.3\text{ W}$	-	0.3	-	%
Half-Bridge		$P_O = 1\text{ W}$	-	0.1	-	%
		$P_O = 0\text{ dBFS} = 5.0\text{ W}$	-	0.3	-	%
Parallel Full-Bridge		$P_O = 1\text{ W}$	-	0.1	-	%
		$P_O = 0\text{ dBFS} = 22.6\text{ W}$	-	0.3	-	%
Dynamic Range						
Stereo Full-Bridge	DYR	$P_O = -60\text{ dBFS}$ , A-Weighted	-	102	-	dB
		$P_O = -60\text{ dBFS}$ , Unweighted	-	99	-	dB
Half-Bridge		$P_O = -60\text{ dBFS}$ , A-Weighted	-	102	-	dB
		$P_O = -60\text{ dBFS}$ , Unweighted	-	99	-	dB
Parallel Full-Bridge		$P_O = -60\text{ dBFS}$ , A-Weighted	-	102	-	dB
		$P_O = -60\text{ dBFS}$ , Unweighted	-	99	-	dB
MOSFET On Resistance	$R_{DS(ON)}$	$I_d = 0.5\text{ A}$ , $T_J = 50^\circ\text{C}$	-	518	615	m $\Omega$
Efficiency	h	$P_O = 2 \times 11.3\text{ W}$ , $R_L = 8\ \Omega$	-	85	-	%
Minimum Output Pulse Width	$PW_{min}$	No Load	-	50	-	ns
Rise Time of OUTx	$t_r$	Resistive Load	-	20	-	ns
Fall Time of OUTx	$t_f$	Resistive Load	-	20	-	ns
PWM Output Over-Current Error Trip Point	$I_{CE}$	OCREF = 16.2 k $\Omega$	2.4	-	-	A
Junction Thermal Warning Trip Point	$T_{TW}$		-	120	-	$^\circ\text{C}$
Junction Thermal Error Trip Point	$T_{TE}$		-	140	-	$^\circ\text{C}$
VP Under-Voltage Error Trip Point	$V_{UV}$		4.5	-	-	V
Ramp-Up Time - Half-Bridge Configuration	$T_{RU}$	Capacitor = 1000 $\mu\text{F}$	-	0.8	-	s
Ramp-Down Time- Half-Bridge Configuration	$T_{RD}$	Capacitor = 1000 $\mu\text{F}$	-	50	-	s

## DC ELECTRICAL CHARACTERISTICS

GND = PGND = 0 V; All voltages with respect to ground; PWM switch rate = 384 kHz; Unless otherwise specified.

Parameters	Min	Typ	Max	Units	
<b>Normal Operation</b> (Notes 5, 8)					
Power Supply Current	VD = 3.3 V	-	20	-	mA
Power Dissipation	VD = 3.3 V	-	66	-	mW
50 % Duty Cycle VP Idle Current (Note 6)	VP = 18 V	-	20	-	mA
<b>Power-Down Mode</b> (Note 7)					
Power Supply Current	VD = 3.3 V	-	4.3	-	mA
Power Supply Current	VP = 18 V	-	100	-	μA
<b>VD_REG Characteristics</b>					
Nominal Voltage	2.25	2.5	2.75	V	
DC current source	-	-	3	mA	
<b>VA_REG Characteristics</b>					
Nominal Voltage	2.25	2.5	2.75	V	
DC current source	-	-	1	mA	

- Notes:**
- Normal operation is defined as  $\overline{\text{RSTx/y}} = \text{HI}$ .
  - All outputs idle.
  - Power-Down Mode is defined as  $\overline{\text{RSTx/y}} = \text{LOW}$  with all input lines held static.
  - Power supply current increases with increasing PWM switching rates.

## DIGITAL INTERFACE SPECIFICATIONS

GND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

Parameters	Symbol	Min	Max	Units
High-Level Input Voltage	$V_{IH}$	$0.7 \cdot VD\_REG$	VD	V
Low-Level Input Voltage	$V_{IL}$	-	$0.20 \cdot VD\_REG$	V
High-Level Output Voltage	$V_{OH}$	$0.90 \cdot VD$	-	V
Input Leakage Current	$I_{in}$	-	±10	μA
Input Capacitance		-	8	pF

## DIGITAL I/O PIN CHARACTERISTICS

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
VD	1	CNFG0	Input	-	2.5 V-5.0 V
	2	CNFG1	Input	-	2.5 V-5.0 V
	3	CNFG2	Input	-	2.5 V-5.0 V
	4	IN1	Input	-	2.5 V-5.0 V
	5	IN2	Input	-	2.5 V-5.0 V
	6	IN3	Input	-	2.5 V-5.0 V
	7	IN4	Input	-	2.5 V-5.0 V
	8	$\overline{\text{RST12}}$	Input	-	2.5 V-5.0 V
	9	LVD	Input	-	2.5 V-5.0 V
	41	$\overline{\text{TWR}}$	Output	2.5 V-5.0 V, Open Drain	-
	42	$\overline{\text{ERRUVTE}}$	Output	2.5 V-5.0 V, Open Drain	-
	43	$\overline{\text{ERROC12}}$	Output	2.5 V-5.0 V, Open Drain	-
	44	$\overline{\text{ERROC34}}$	Output	2.5 V-5.0 V, Open Drain	-
	45	RAMP	Input	-	2.5 V-5.0 V
46	$\overline{\text{RST34}}$	Input/	-	2.5 V-5.0 V	
VP	35	OUT1	Output	9 V-18 V Power MOSFET	-
	32	OUT2	Output	9 V-18 V Power MOSFET	-
	29	OUT3	Output	9 V-18 V Power MOSFET	-
	26	OUT4	Output	9 V-18 V Power MOSFET	-

**Table 1. I/O Power Rails**



### 3. TYPICAL CONNECTION DIAGRAMS

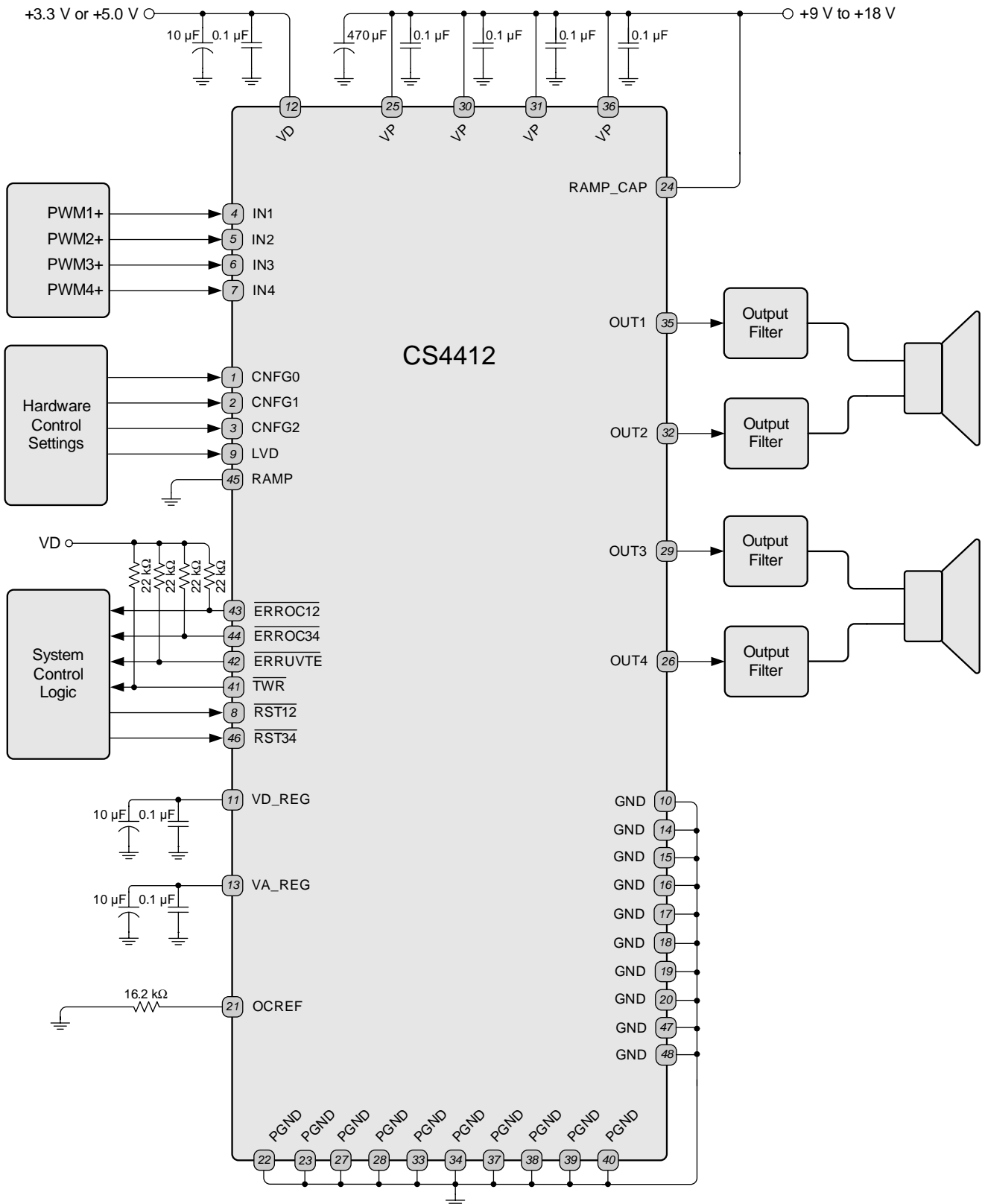
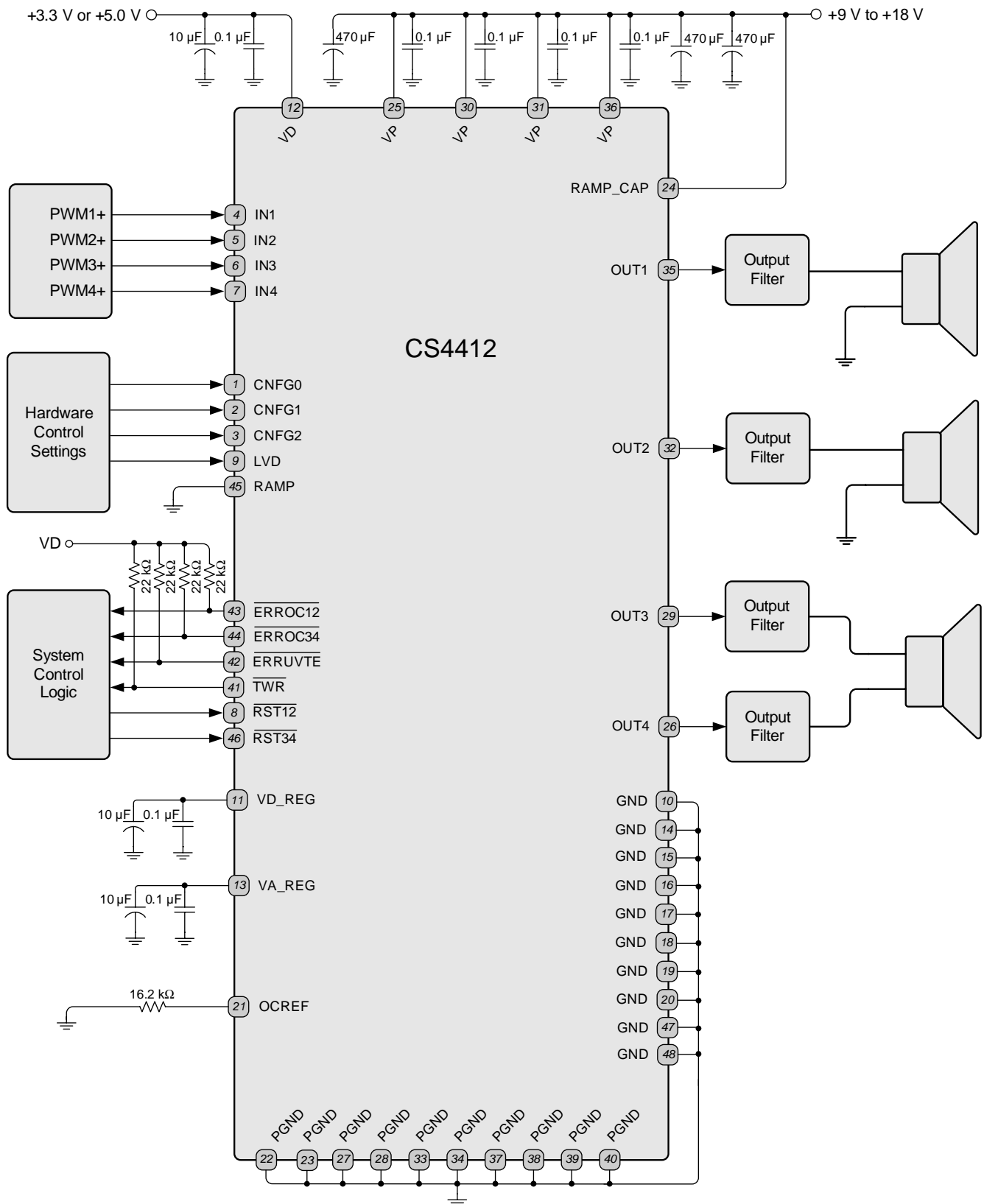
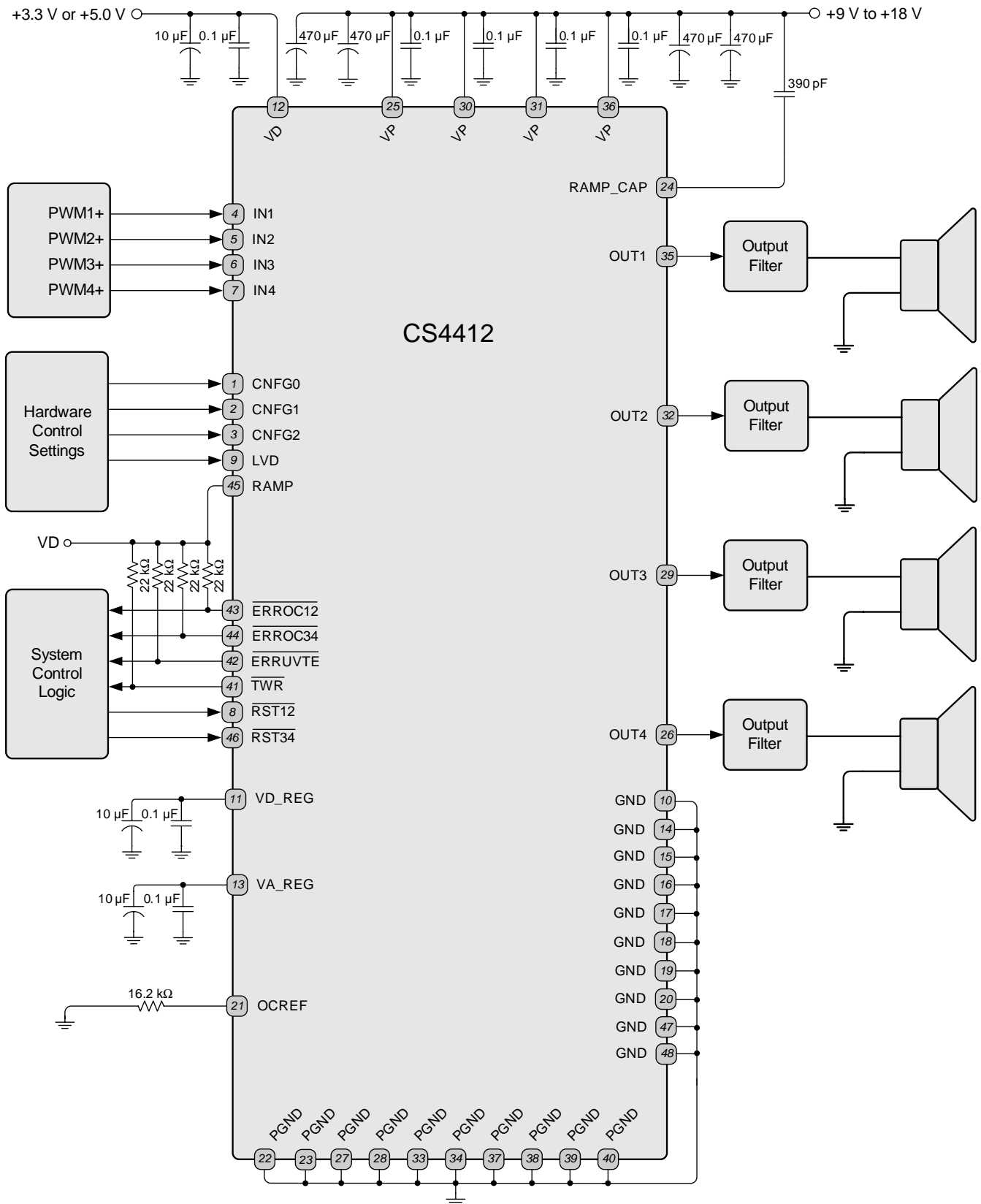


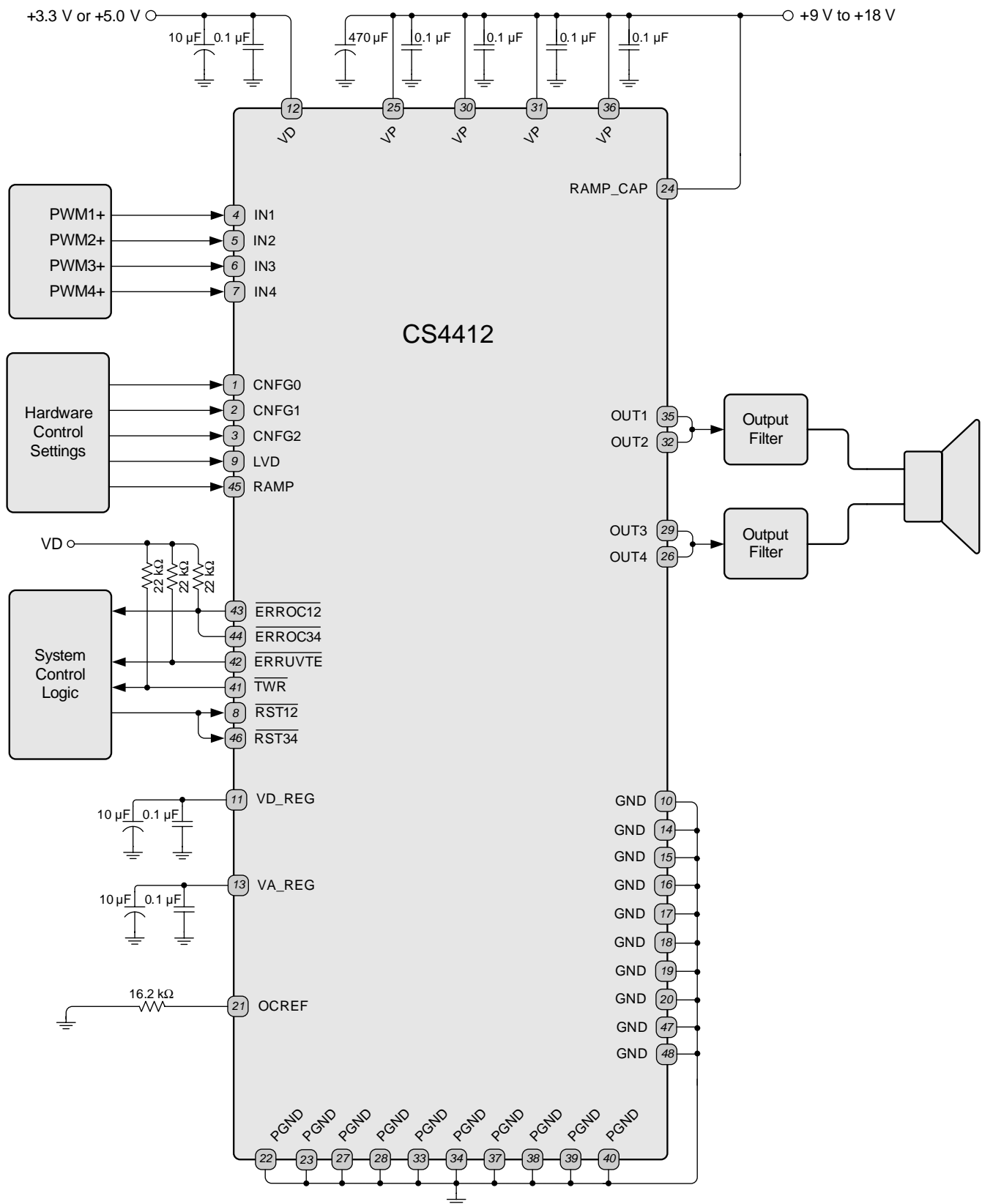
Figure 1. Stereo Full-Bridge Typical Connection Diagram



**Figure 2. 2.1 Channel Typical Configuration Diagram**



**Figure 3. 4-Channel Half-Bridge Typical Connection Diagram**


**Figure 4. Mono Parallel Full-Bridge Typical Connection Diagram**

## 4. APPLICATIONS

### 4.1 Overview

The CS4412 is a high-efficiency power stage for digital Class-D amplifiers designed to be configured as four half-bridge channels, two half-bridge channels and one full-bridge channel, two full-bridge channels, or one parallel full-bridge channel.

The CS4412 integrates on-chip over-current, under-voltage, over-temperature protection and error reporting as well as a thermal warning indicator. The low  $R_{DS(ON)}$  outputs can source up to 2.4 A peak current, delivering 85% efficiency. This efficiency provides for smaller device package, no external heat sink requirements, and smaller power supplies.

### 4.2 Reset and Power-Up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks, and configuration pins are stable. It is also recommended that the  $\overline{RSTx/y}$  pin be activated if the voltage supplies drop below the recommended operating condition to prevent power-glitch-related issues.

When  $\overline{RSTx/y}$  is low, the corresponding channels of the CS4412 enter a low-power mode and all of the channels' internal states are reset and the outputs are set to HI-Z. When  $\overline{RSTx/y}$  is high, the desired mode settings will be loaded and the outputs will begin normal operation.

#### 4.2.1 PWM Popguard Transient Control

The CS4412 uses Popguard technology to minimize the effects of output transients during power-up and power-down for half-bridge configurations. This technique reduces the audio transients commonly produced by half-bridge, single-supply amplifiers when implemented with external DC-blocking capacitors connected in series with the audio outputs.

When the device is configured for ramping (RAMP set high) and  $\overline{RSTx/y}$  is set high, the  $OUTx/y$  outputs will ramp-up to the bias point ( $VP/2$ ). This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient. The  $OUTx/y$  outputs will not begin normal operation until the ramp has reached the bias point. The  $INx/y$  inputs must begin switching before the ramp cycle begins.

When the device is configured for ramping (RAMP set high) and  $\overline{RSTx/y}$  is set low, the  $OUTx/y$  outputs will begin to slowly ramp down from the bias point to PGND, allowing the DC-blocking capacitor to discharge.

The ramp feature should only be used in quad half-bridge configuration. It is not necessary to complete a ramp-up/down sequence before ramping up/down again.

#### 4.2.2 Recommended Power-Up Sequence

1. Turn on the system power.
2. Hold  $\overline{RSTx/y}$  low until the power supply and system clocks are stable. In this state, all associated outputs are HI-Z.
3. Start the PWM modulator output.
4. Once the PWM modulator output is valid, release  $\overline{RSTx/y}$  high. If the CS4412 is configured for ramping, the outputs will ramp to the bias point and then begin switching normally. If the CS4412 is not configured for ramping, the outputs will immediately begin switching normally.

### 4.2.3 Recommended Power-Down Sequence

1. Mute the logic-level PWM inputs present on IN1 - IN4 by applying 50 % duty-cycle inputs.
2. Set  $\overline{\text{RSTx/y}}$  low. If the CS4412 is configured for ramping, the outputs will ramp down to PGND and then become HI-Z. If the CS4412 is not configured for ramping, the outputs will immediately become HI-Z.
3. Power down the remainder of the system.
4. Turn off the system power.

## 4.3 Output Mode Configuration

The CS4412 can be configured for several modes of operation. [Table 2](#) shows the setting of the CNFG[2:0] inputs and the corresponding mode of operation. These pins should remain static during operation ( $\overline{\text{RSTx/y}}$  set high).

CNFG2	CNFG1	CNFG0	Output Config.	Description
0	0	0	Stereo Full-Bridge Tied Loads	IN1 must be inverted from IN2 for full-bridge operation. IN3 must be inverted from IN4 for full-bridge operation.
0	0	1	Stereo Half-Bridge and Mono Full-Bridge Tied Loads	IN1 must be provided for half-bridge operation. IN2 must be provided for half-bridge operation. IN3 must be inverted from IN4 for full-bridge operation.
0	1	0	Mono Parallel Full-Bridge Tied Load	IN1 and IN3 must be inverted from IN2 and IN4 for parallel full-bridge operation.
0	1	1	Quad Half-Bridge Tied Loads	IN1 must be provided for half-bridge operation. IN2 must be provided for half-bridge operation. IN3 must be provided for half-bridge operation. IN4 must be provided for half-bridge operation.
1	0	0	Stereo Full-Bridge Tied Loads With Inversion	IN1 must be provided for full-bridge operation. Wire IN2 to IN1. IN2 is internally inverted for full-bridge operation. IN3 must be provided for full-bridge operation. Wire IN4 to IN3. IN4 is internally inverted for full-bridge operation.
1	0	1	Stereo Half-Bridge & Mono Full-Bridge Tied Loads With Inversion	IN1 must be provided for half-bridge operation. IN2 must be provided for half-bridge operation. IN3 must be provided for full-bridge operation. Wire IN4 to IN3. IN4 is internally inverted for full-bridge operation.
1	1	0	Mono Parallel Full-Bridge Tied Load With Inversion	IN1 must be provided for parallel full-bridge operation. Wire IN4, IN3, and IN2 to IN1. IN2 and IN4 are internally inverted for parallel full-bridge operation.
1	1	1	Quad Half-Bridge Tied Loads	IN1 must be provided for half-bridge operation. IN2 must be provided for half-bridge operation. IN3 must be provided for half-bridge operation. IN4 must be provided for half-bridge operation.

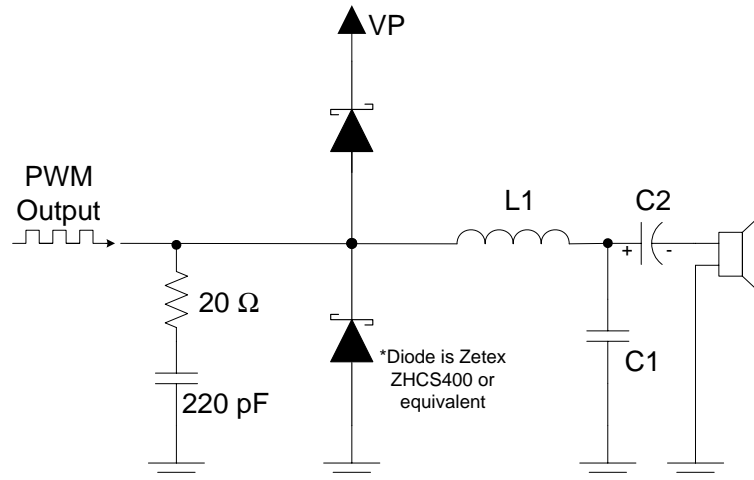
**Table 2. Output Mode Configuration Options**

## 4.4 Output Filters

The filter placed after the PWM outputs can greatly affect the output performance. The filter not only reduces radiated EMI (snubber filter), but also filters high frequency content from the switching output before going to the speaker (low-pass LC filter).

### 4.4.1 Half-Bridge Output Filter

Figure 5 shows the output filter for a half-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a resistor ( $20\ \Omega$ ,  $\frac{1}{4}\text{ W}$ ) and capacitors ( $220\ \text{pF}$ ) and should be placed as close as possible to the corresponding PWM output pin to greatly reduce radiated EMI.



**Figure 5. Output Filter - Half-Bridge**

The inductor, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 3 shows the component values for L1 and C1 based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

Load	L1	C1
4 $\Omega$	22 $\mu\text{H}$	1.0 $\mu\text{F}$
6 $\Omega$	33 $\mu\text{H}$	0.68 $\mu\text{F}$
8 $\Omega$	47 $\mu\text{H}$	0.47 $\mu\text{F}$

**Table 3. Low-Pass Filter Components - Half-Bridge**

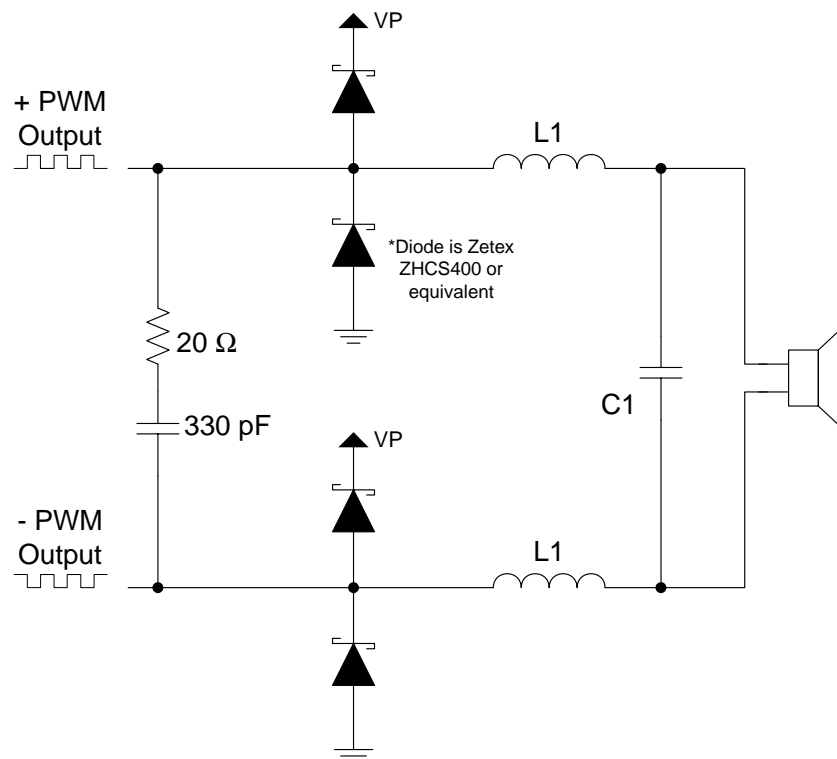
C2 is the DC-blocking capacitor. Table 4 shows the component values for C2 based on corner frequency (-3 dB point) and a nominal speaker (load) impedances of 4  $\Omega$ , 6  $\Omega$ , and 8  $\Omega$ . This capacitor should also be chosen to have a ripple current rating above the amount of current that will be passed through it.

Load	Corner Frequency	C2
4 Ω	40 Hz	1000 μF
	58 Hz	680 μF
	120 Hz	330 μF
6 Ω	39 Hz	680 μF
	68 Hz	390 μF
	120 Hz	220 μF
8 Ω	42 Hz	470 μF
	60 Hz	330 μF
	110 Hz	180 μF

**Table 4. DC-Blocking Capacitors Values - Half-Bridge**

#### 4.4.2 Full-Bridge Output Filter (Stereo or Parallel)

Figure 6 shows the output filter for a full-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a resistor (20 Ω) and capacitor (330 pF) and should be placed as close as possible to the corresponding PWM output pins to greatly reduce radiated EMI. The inductors, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 5 shows the component values based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.


**Figure 6. Output Filter - Full-Bridge**

Load	L1	C1
4 Ω	10 μH	1.0 μF
6 Ω	15 μH	0.47 μF
8 Ω	22 μH	0.47 μF

**Table 5. Low-Pass Filter Components - Full-Bridge**



## 4.5 Device Protection and Error Reporting

The CS4412 has built-in protection circuitry for over-current, under-voltage, and thermal warning/overload conditions. The levels of the over-current error, thermal error, and VP under-voltage trip points are listed in the [PWM Power Output Characteristics](#) table on [page 6](#). Automatic shut-down will occur whenever any of these preset thresholds are crossed.

Each error and warning pin implements an active-low open-drain driver and requires an external pull-up for proper operation.

### 4.5.1 Over-current Protection

Over-current errors are reported on the  $\overline{\text{ERROCx/y}}$  pins. For example, an over-current error on OUT1 is reported by the  $\overline{\text{ERROC1/2}}$  pin. The power output of the channel which is reporting the over-current condition will be set to high-impedance until the error condition has been removed and the  $\overline{\text{RSTx/y}}$  signal for that channel has been toggled from low to high.

ERROCx/y	Reported Condition
0	Over-current error on channel x or channel y.
1	Operating current of channel x and y within allowable limits.

**Table 6. Over-current Error Conditions**

### 4.5.2 Thermal Warning, Thermal Error, and Under-Voltage Error

[Table 7](#) shows the behavior of the  $\overline{\text{TWR}}$  and  $\overline{\text{ERRUVTE}}$  pins. When the junction temperature exceeds the junction thermal warning trip point, the  $\overline{\text{TWR}}$  pin will be set low. If the junction temperature continues to increase beyond the junction thermal error trip point, the  $\overline{\text{ERRUVTE}}$  pin will be set low. If the voltage on VP falls below the VP under-voltage error trip point,  $\overline{\text{ERRUVTE}}$  will be set low.

When the thermal error or VP under-voltage trip point is crossed, all power outputs will be set to high-impedance until the error condition has been removed and the  $\overline{\text{RSTx/y}}$  signals have been toggled from low to high.

TWR	ERRUVTE	Reported Condition
0	0	Thermal warning and thermal error and/or under-voltage error.
0	1	Thermal warning only.
1	0	Under-voltage error.
1	1	Junction temperature and VP voltage within normal limits.

**Table 7. Thermal and Under-Voltage Error Conditions**

## 5. POWER SUPPLY, GROUNDING, AND PCB LAYOUT

### 5.1 Power Supply and Grounding

The CS4412 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. It is necessary to decouple the power supply by placing capacitors directly between the power and ground of the CS4412. Decoupling capacitors should be as close to the pins of the CS4412 as possible. The lowest value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS4412 to minimize inductance effects. The CRD4412 reference design demonstrates the optimum layout and power supply arrangements.

#### 5.1.1 Integrated VD Regulator

The CS4412 includes two internal linear regulators, one from the VD supply voltage to provide a fixed 2.5 V supply to its internal digital blocks, and another from the VD supply voltage to provide a fixed 2.5 V supply to its internal analog blocks. The LVD pin must be set to indicate the voltage present on the VD pin as shown in Table 8 below.

LVD	Indicated VD Supply Level
Low	2.5 V or 3.3 V Nominal
High	5 V Nominal

**Table 8. VD Supply Level Indication**

The output of the digital regulator is presented on the VD\_REG pin and may be used to provide an external device with up to 3 mA of current at its nominal output voltage of 2.5 V. The output of the analog regulator is presented on the VA\_REG pin and must only be connected to the bypass capacitors as shown in the typical connection diagrams.

If a nominal supply voltage of 2.5 V is used as the VD supply (see the Recommended Operating Conditions table on page 5), the VD, VD\_REG, and VA\_REG pins must all be connected to the VD supply source. In this configuration, the internal regulators are bypassed and the external supply source is used to directly drive the internal digital and analog sections.

### 5.2 QFN Thermal Pad

The CS4412 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of thermal vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. The CRD4412 reference design demonstrates the optimum thermal pad and via configuration.

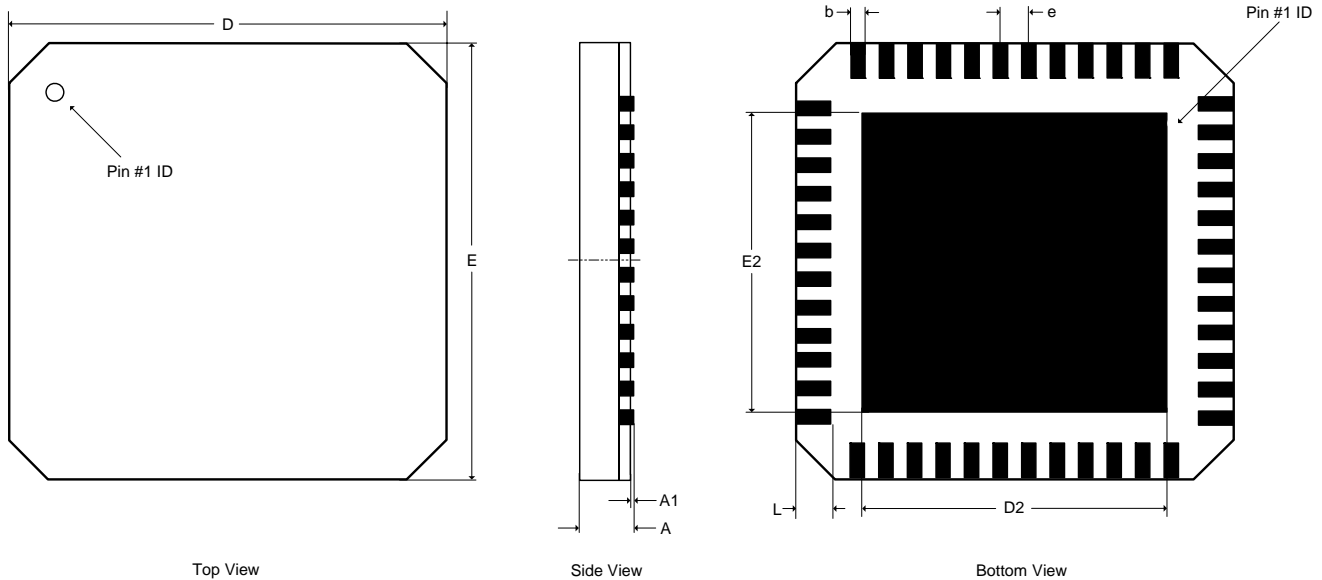
## **6. PARAMETER DEFINITIONS**

### **Dynamic Range (DYR)**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

### **Total Harmonic Distortion + Noise (THD+N)**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

**7. PACKAGE DIMENSIONS**
**48L QFN (9 × 9 MM BODY) PACKAGE DRAWING**


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0354	--	--	0.90	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0118	0.0138	0.0157	0.30	0.35	0.40	1,2
D	0.3543 BSC			9.00 BSC			1
D2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
E	0.3543 BSC			9.00 BSC			1
E2	0.2618	0.2677	0.2736	6.65	6.80	6.95	1
e	0.0256 BSC			0.65 BSC			1
L	0.0177	0.0217	0.0276	0.45	0.55	0.70	1

**JEDEC #: MO-220**

*Controlling Dimension is Millimeters.*

- Notes:**
1. Dimensioning and tolerance per ASME Y4.5M - 1994.
  2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

## 8. THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Junction to Case Thermal Impedance	$\theta_{JC}$	-	1	-	°C/Watt

### 8.1 Thermal Flag

This device is designed to have the metal flag on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS4412. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$$\theta_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$$

where,

$\theta_{CA}$  = Thermal resistance of the metal plane in °C/Watt

$T_{J(MAX)}$  = Maximum rated operating junction temperature in °C, equal to 150 °C

$T_A$  = Ambient temperature in °C

$P_D$  = RMS power dissipation of the device, equal to  $0.15 \cdot P_{RMS-IN}$  or  $0.176 \cdot P_{RMS-OUT}$  (assuming 85% efficiency)

$\theta_{JC}$  = Junction-to-case thermal resistance of the device in °C/Watt

## 9. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS4412	30 W Quad Half-Bridge Digital Amplifier Power Stage	48-QFN	Yes	Commercial	-40° to +70°C	Rail	CS4412-CNZ
						Tape and Reel	CS4412-CNZR
CRD4412	1 x 30 W Reference Design Daughter Card	-	-	-	-	-	CRD4412
CRD4525	2 x 15 W Reference Design Main Board	-	-	-	-	-	CRD4525

## 10. REVISION HISTORY

Release	Changes
A1	Initial Release

### Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

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