SONY

# CXA1622M/P

## Stereo Power Amplifier/Monaural BTL Power Amplifier

### Description

The CXA1622M/P is a bipolar IC developed as power amplifier for compact radio cassettes with built-in pre-amplifier and power amplifier electrical volume.

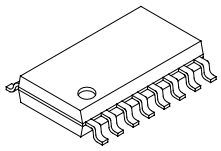
### Features

- Use one channel in stereo mode
  - · EIAJ output=110 mW (Typ.), $V_{CC}$=3 V, $R_L$=8 Ω (CXA1622M)
  - · EIAJ output=450 mW (Typ.), $V_{CC}$=6 V, $R_L$=8 Ω (CXA1622P)
- BTL mode
  - · EIAJ output=320 mW (Typ.), $V_{CC}$=3 V, $R_L$=8 Ω (CXA1622M)
  - · EIAJ output=360 mW (Typ.), $V_{CC}$=3 V, $R_L$=8 Ω (CXA1622P)
- Built-in electrical volume
- Built-in ripple filter (ripple rejection 34.5 dB typ.)
- Selection between stereo power amplifier and monaural BTL power amplifier is possible by switching Pin 2.

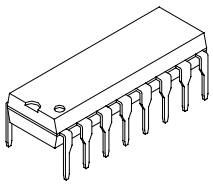
### Applications

Suitable for audio power amplifier for stereo and monaural radios and power amplifier for radio cassette and Walkman.

CXA1622M
16 pin SOP (Plastic)



CXA1622P
16 pin DIP (Plastic)



### Structure

Bipolar silicon monolithic IC

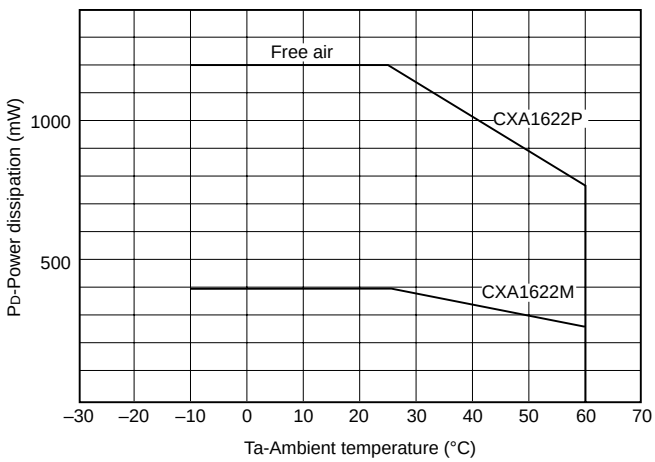
### Absolute Maximum Ratings (Ta=25 °C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC}$ | 8 | V |
| • Operating temperature | Topr | –10 to +60 | °C |
| • Storage temperature | Tstg | –65 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 410 (CXA1622M) | mW |
| | | 1200 (CXA1622P) | mW |

### Operating Conditions (Ta=25 °C)

- Supply voltage
- Stereo mode { 1.8 V to 4.5 V (CXA1622M); 1.8 V to 7.0 V (CXA1622P)
- Monaural BTL mode 1.8 V to 4.5 V (3 V recommended)

Power dissipation curve

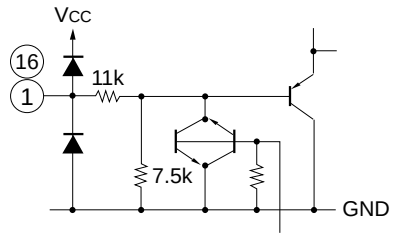
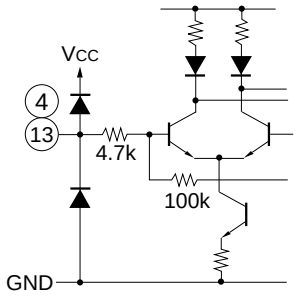
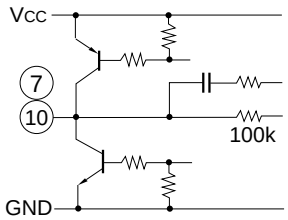
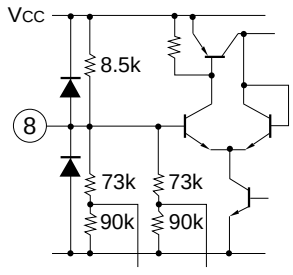


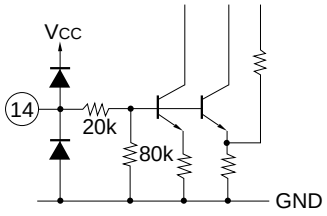
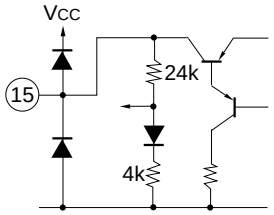
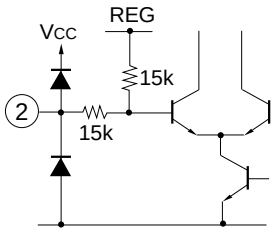





E92121B79-TE

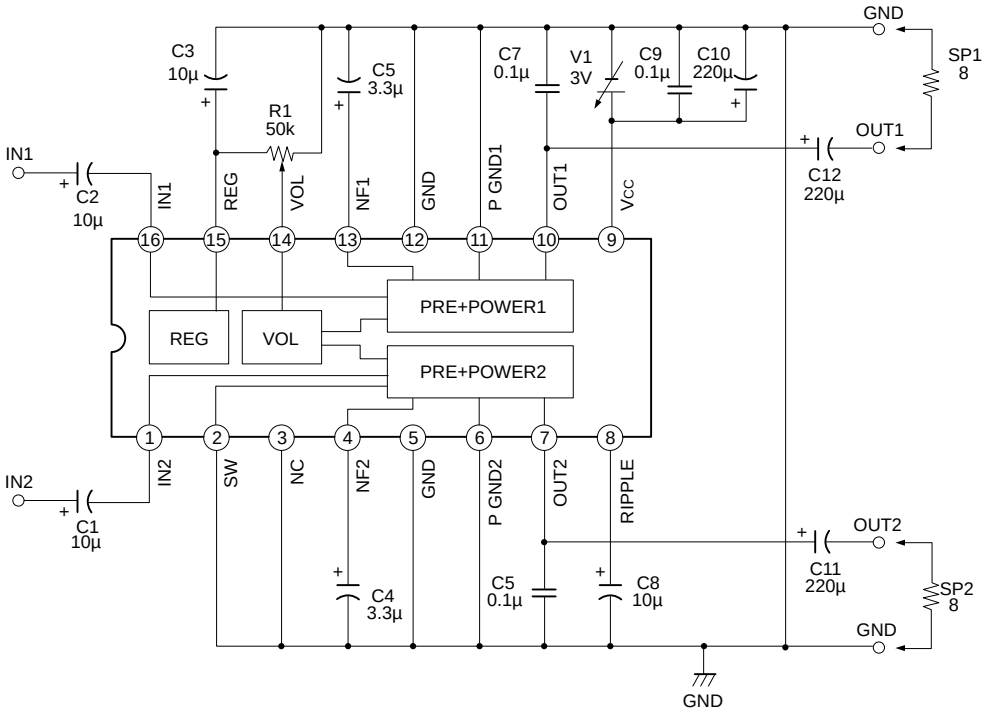
**Pin Description**

| Pin No. | Symbol | Equivalent circuit | Pin voltage | | Description |
|---|---|---|---|---|---|
| | | | 3 V | 6 V | |
| 1, 16 | IN1<br>IN2 |  | 0 | 0 | Input |
| 3 | NC | | — | — | |
| 4, 13 | NF1<br>NF2 |  | 1.5 | 3 | Power amplifier NF.<br>Connected to time constant 4.7 µF. |
| 5, 12 | GND1<br>GND2 | | 0 | 0 | Pre-amplifier GND |
| 6, 11 | P-GND1<br>P-GND2 | | 0 | 0 | Power amplifier GND |
| 7, 10 | OUT1<br>OUT2 |  | 1.5 | 3 | Power amplifier output |
| 8 | RIPPLE |  | 2.72 | 5.43 | Connected to time constant 10 µF for ripple filter. |
| 9 | Vcc | | 3 | 6 | Vcc |

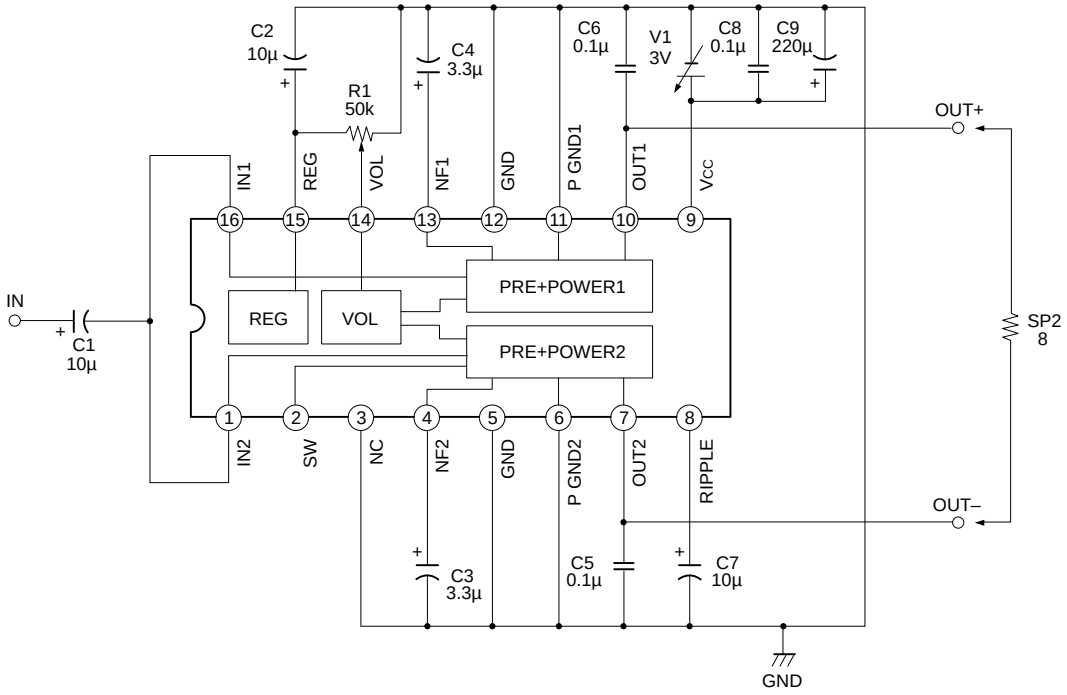
| Pin No. | Symbol | Equivalent circuit | Pin voltage 3 V | Pin voltage 6 V | Description |
|---|---|---|---|---|---|
| 14 | VOL |  | 0 to 1.25 | 0 to 1.25 | Control gain with change in voltage (0 to 1.25 V) to electrical volume control pin. |
| 15 | REG |  | 1.25 | 1.25 | Regulator pin |
| 2 | SW |  | 1.25 | 1.25 | Mode selection SW<br>• BTL mode when open<br>• Stereo mode when connected to GND |

**Block Diagram, Pin Configuration, and Application Circuit**

1) Stereo mode



2) BTL mode




* The input signal enters the pre-amplifier with attenuation controlled with DC at Pin 14 and then it is amplified by the approximately 30 dB (fixed) power amplifier.
* The state of Pin 2 can be used to select between stereo mode and monaural BTL mode.
  The pre-power 1 and pre-power 2 output are positive phase output when Pin 2 is GND. Pre-power 2 is inverse output of pre-power 1 output when Pin 2 is open.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Stereo mode { Upper : CXA1622M ($V_{CC}$=3 V)
Lower : CXA1622P ($V_{CC}$=6 V)

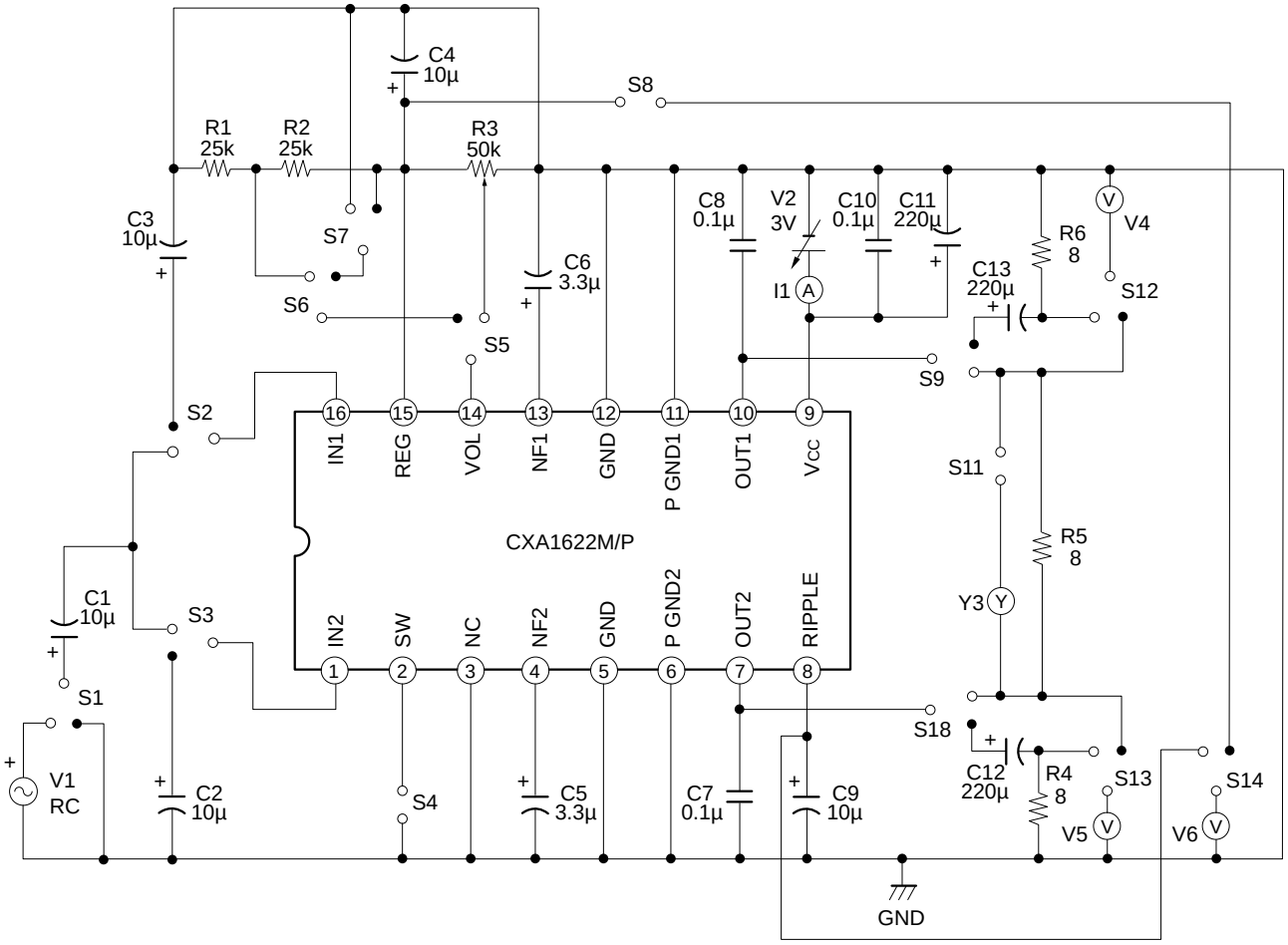
| Function block | Test No. | Test item | BIAS SW conditions | | | | | | | | | | | | | | Input point | Input waveform and bias description | Test point | Output waveform and description of test method | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | | | | | | | | |
| Typical conditions for each bias | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | Circuit current during no signal | OFF | OFF | OFF | ON | OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | | | $I_1$ | Circuit current during no signal | 1.0<br>1.0 | 3.0<br>3.0 | 8.2<br>7.7 | mA |
| | 2 | Audio voltage gain Lch | ON | ON | OFF | | | | | | | | | ON | ↓ | | | | $V_4$ | $V_1$=–40 dBm 1 kHz | 28<br>27 | 33.7<br>32.6 | 38<br>36 | dB |
| | 3 | Audio voltage gain Rch | | OFF | ON | | | | | | | | | OFF | ON | | | | $V_5$ | $V_1$=–40 dBm 1 kHz | 28<br>27 | 33.7<br>32.6 | 38<br>36 | dB |
| | 4 | Channel balance | | ↓ | ↓ | | | ↓ | | | | | | ↓ | ↓ | | | | $V_4$<br>$V_5$ | L and R channel balance | –3 | 0 | 3 | dB |
| | 5 | Attenuation Lch | | ON | OFF | | | ON | | | | | | ON | OFF | | | | $V_4$ | $V_1$=–40 dBm 1 kHz<br>Output level difference between max volume and half volume | 1.5<br>1.0 | 5.8<br>4.3 | 12<br>12 | dB |
| | 6 | Attenuation Rch | | OFF | ON | | ↓ | | | | | | | OFF | ON | | | | $V_5$ | $V_1$=–40 dBm 1 kHz<br>Output level difference between max volume and half volume | 1.5<br>1.0 | 5.8<br>4.3 | 12<br>12 | dB |
| | 7 | EIAJ output Lch | | ON | OFF | | ON | | | | | | | ON | OFF | | | | $V_4$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Output level where THD=10 % | 350<br>90 | 450<br>110 | | mW |
| | 8 | EIAJ output Rch | | OFF | ON | | | | | | | | | OFF | ON | | | | $V_5$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Output level where THD=10 % | 350<br>90 | 450<br>110 | | mW |
| | 9 | Audio distortion factor Lch | | ON | OFF | | | | | | | | | ON | OFF | | | | $V_4$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Distortion factor when output is 50 mW | | 0.7 | 2.5 | % |
| | 10 | Audio distortion factor Rch | ↓ | OFF | ON | | ↓ | ↓ | | | | | | OFF | ON | | | | $V_5$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Distortion factor when output is 50 mW | | 0.7 | 2.5 | % |
| | 11 | Residual noise level Lch | OFF | OFF | OFF | | OFF | OFF | | | | | | ON | OFF | | | | $V_4$ | Noise level during no signal at max volume | | –65 | –60 | dBm |
| | 12 | Residual noise level Rch | ↓ | ↓ | | | | | | | | | | OFF | ON | | | | $V_5$ | Noise level during no signal at max volume | | –65 | –60 | dBm |
| | 13 | Crosstalk L → R | ON | ON | ↓ | | | | | | | | | ↓ | ↓ | | | | | $V_1$=–40 dBm 1 kHz<br>Rch output level when Lch is input | | –60 | –56 | dBm |
| | 14 | Crosstalk R → L | ↓ | OFF | ON | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ON | OFF | ↓ | | | | $V_1$=–40 dBm 1 kHz<br>Lch output level when Rch is input | | –60 | –56 | dBm |

BTL mode $V_{CC}$=3 V

Upper : CXA1622M
Lower : CXA1622P

| Function block | Test No. | Test item | BIAS SW conditions | | | | | | | | | | | | | | Input point | Input waveform and bias description | Test point | Output waveform and description of test method | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | | | | | | | | |
| Typical conditions for each bias | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | Circuit current during no signal | OFF | ON | ON | OFF | OFF | OFF | ON | OFF | ON | ON | OFF | ON | ON | OFF | | | $I_1$ | Circuit current during no signal | | 3 | 7 | mA |
| | 2 | Output DC bias lag | ↓ | | | | | | | | | | ON | | | | | | $\|V_3\|$ | Output DC bias lag | | 0 | 30 | mV |
| | 3 | Audio voltage gain | ON | | | | | ↓ | | | | | | | | | | | $V_3$ | $V_1$=–40 dBm 1 kHz | 34<br>30 | 38<br>37 | 42<br>43 | dB |
| | 4 | Attenuation | | | | | ↓ | ON | | | | | | | | | | | $V_3$ | $V_1$=–40 dBm 1 kHz<br>Output level difference between max volume and half volume | 1.5<br>1.0 | 6.0<br>5.0 | 12<br>12 | dB |
| | 5 | EIAJ output | | | | | ON | | | | | | | | | | | | $V_3$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Output level where THD=10 % | 260<br>220 | 360<br>320 | | mW |
| | 6 | Audio distortion factor | | | | | ↓ | ↓ | | | | | | | | | | | $V_3$ | $V_1$=–20 dBm 1 kHz, $R_L$=8 Ω<br>Distortion factor when output is 50 mW | | | 2.5 | % |
| | 7 | Residual noise level | ↓ | ↓ | ↓ | ↓ | OFF | OFF | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | | | $V_3$ | Noise level during no signal at max volume | | –65 | –62 | dBm |

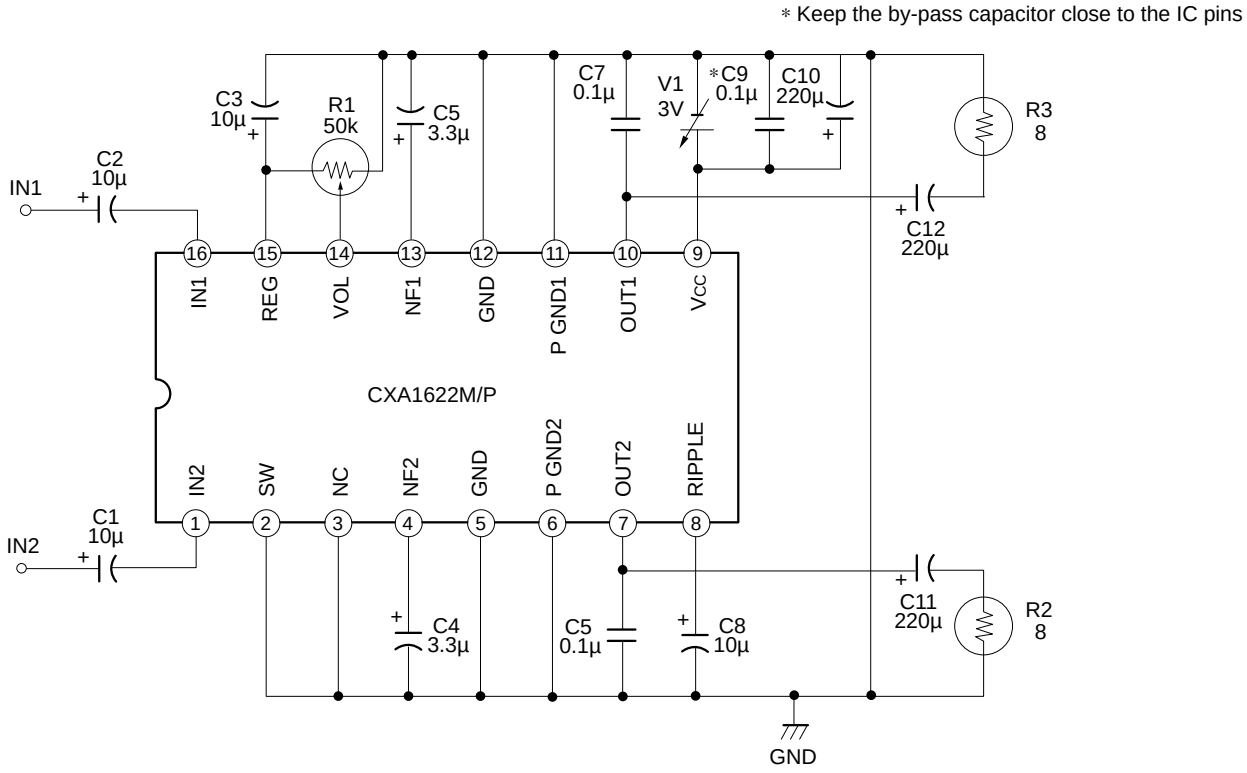
**Electrical Characteristics Test Circuit**



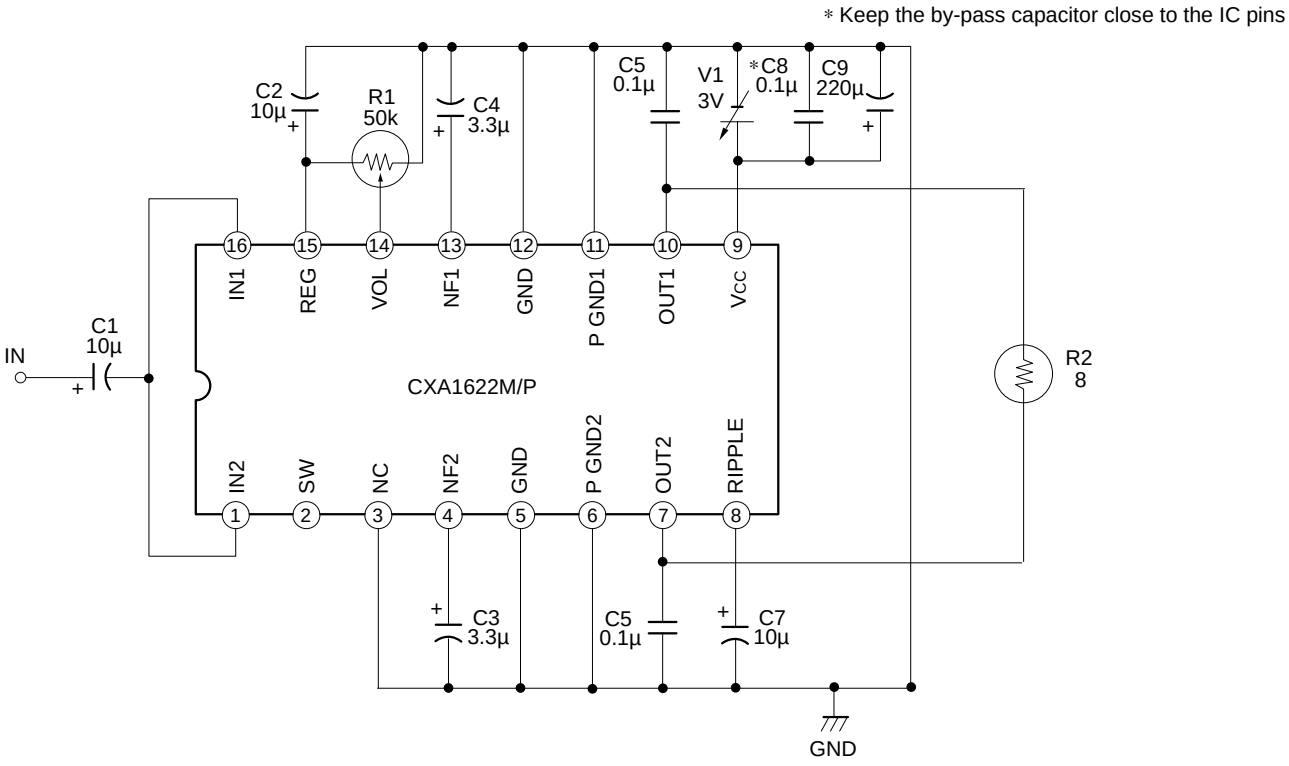

**Notes on Operation**

- Set print pattern to low impedance because Pins 6 and 11 are GND of power amplifier output stage.
- The value of the phase correction capacitance attached to Pins 7 and 10 varies slightly according to the print pattern.
- Provide a large land for DIP type Pin 5 because it also serves as heat dissipation pin.
- Place the by-pass capacitor of $V_{CC}$ (Pin 9) as close to the pin as possible.

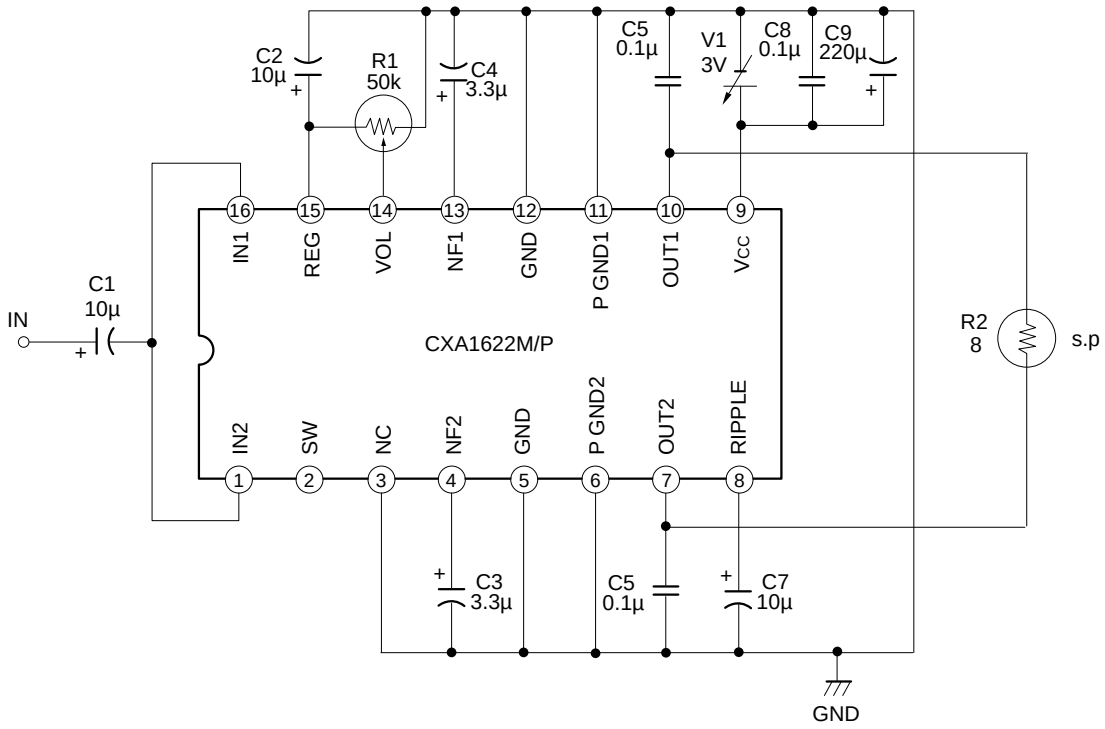
Stereo output single mode



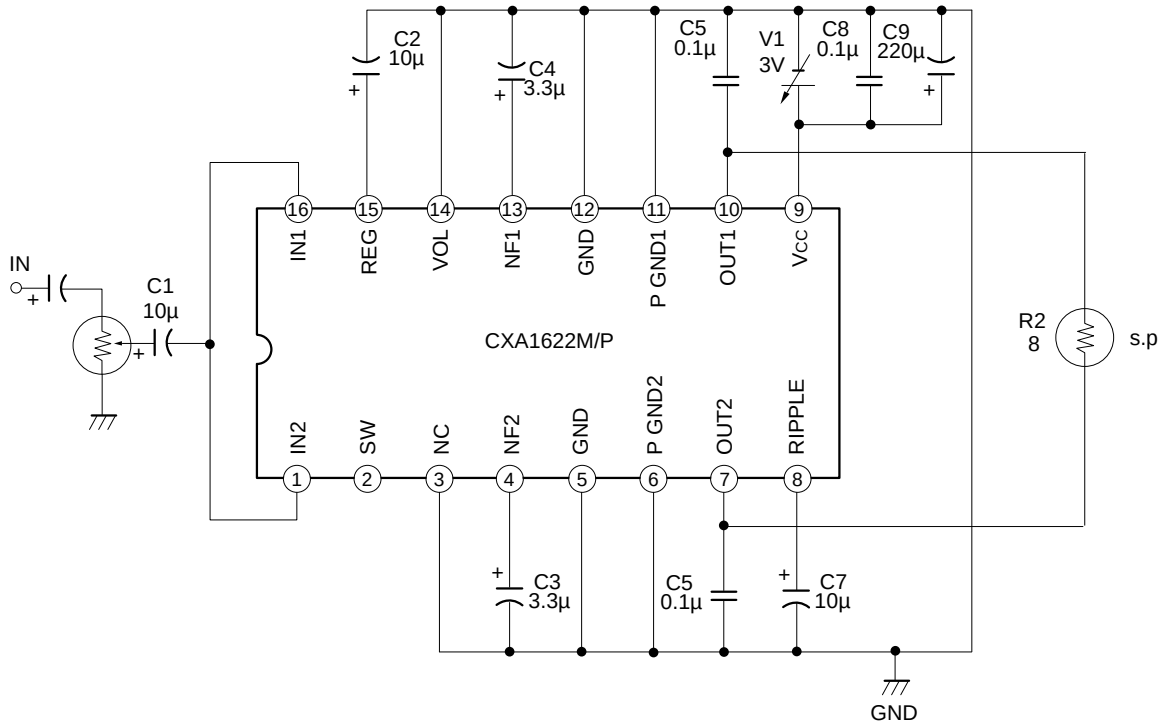

Monaural output BTL mode



When using internal IC electrical volume in BTL mode

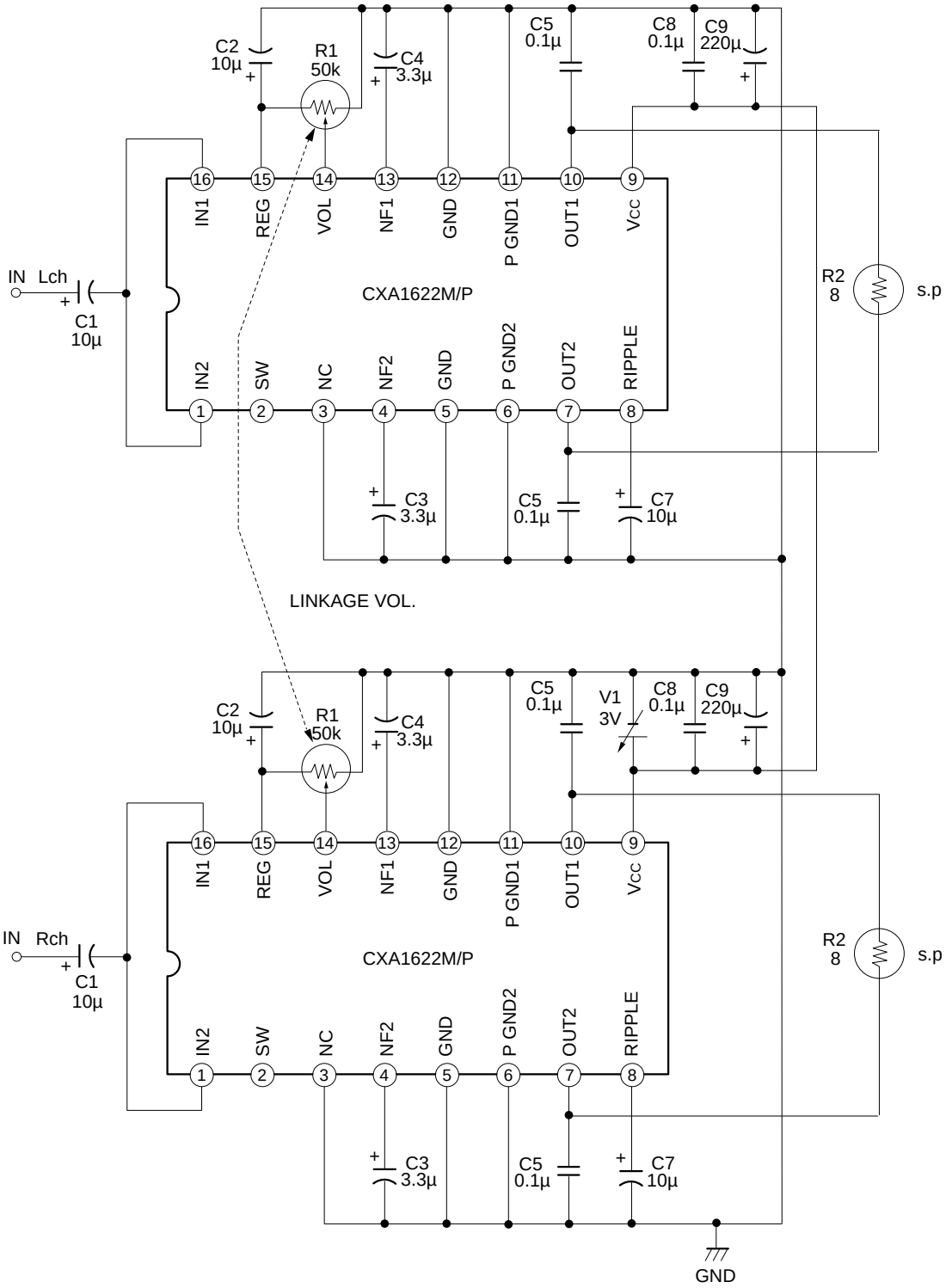



When using IC as fixed gain amplifier in BTL mode
Pin14 → GND (IC Gain MAX)



**BTL, Stereo Application Circuit**

When using internal IC electrical volume

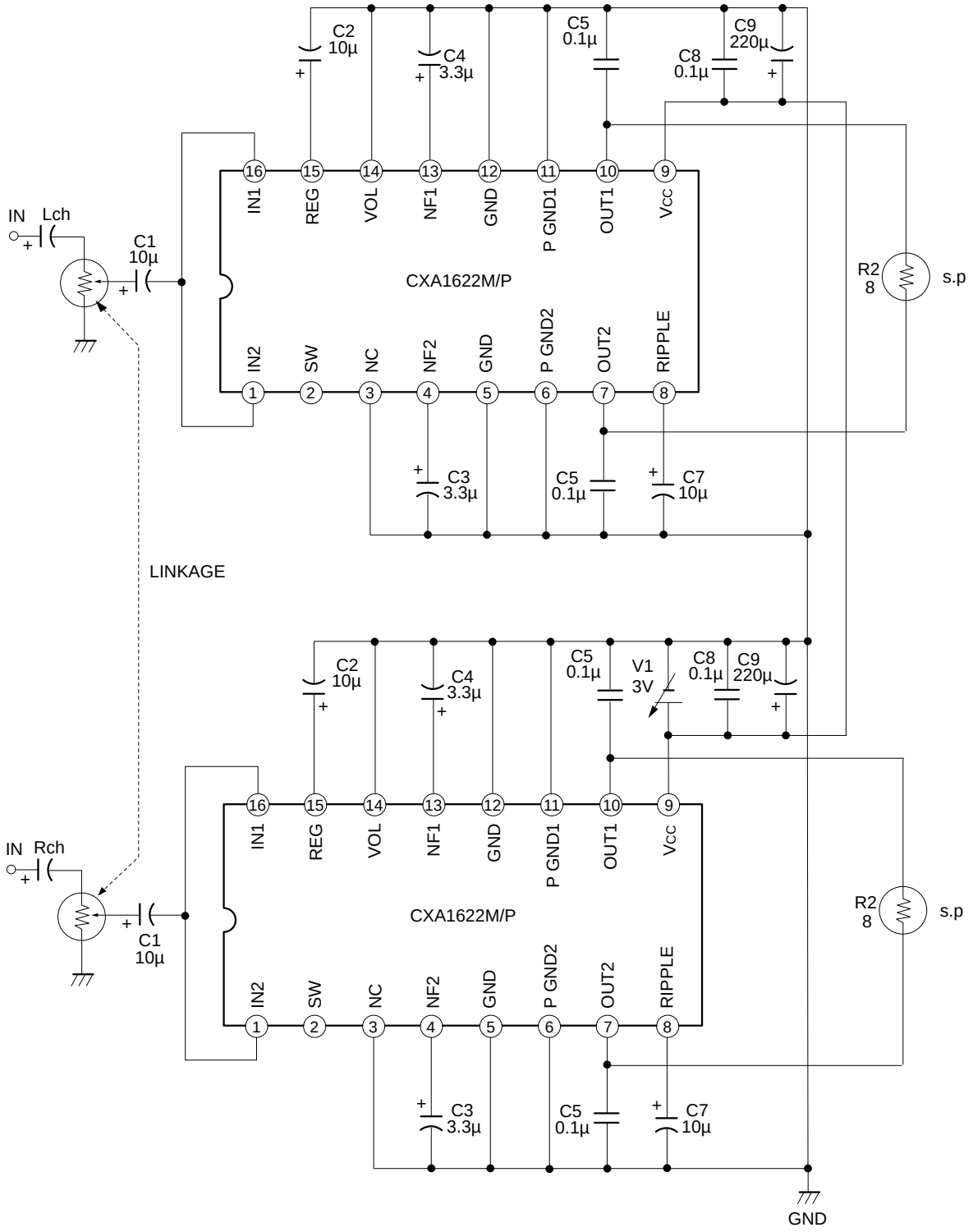



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**BTL, Stereo Application Circuit**

When using IC as fixed gain amplifier

Pin14 → GND (IC Gain Max)

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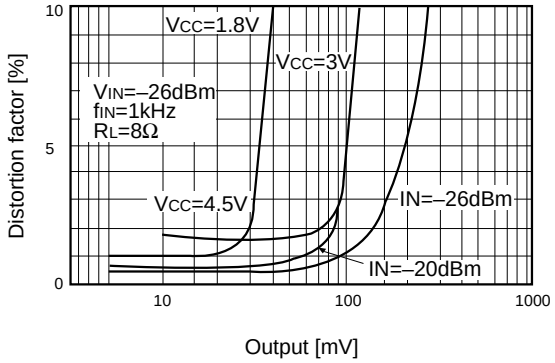
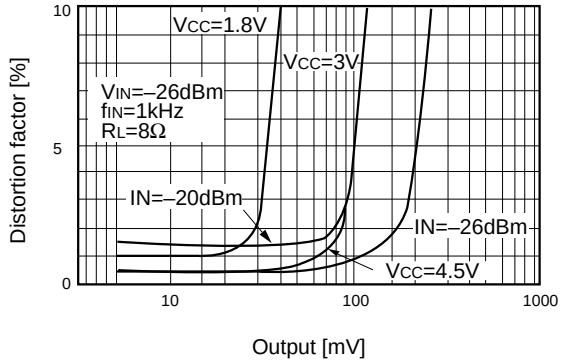
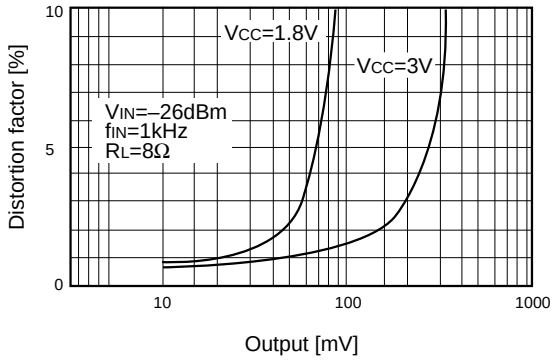
Output vs Distortion 1 CXA1622P
stereo mode single-channel input



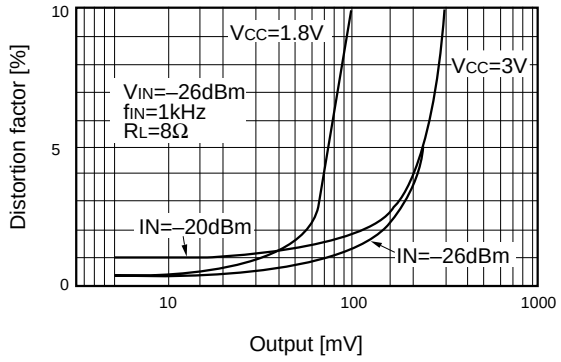

Output vs Distortion 2 CXA1622M
stereo mode single-channel input



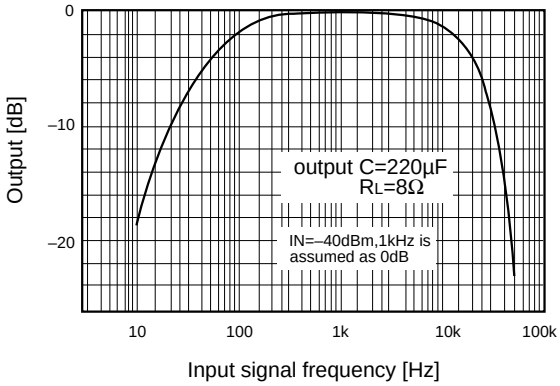

Output vs Distortion factor 3
CXA1622P BTL mode



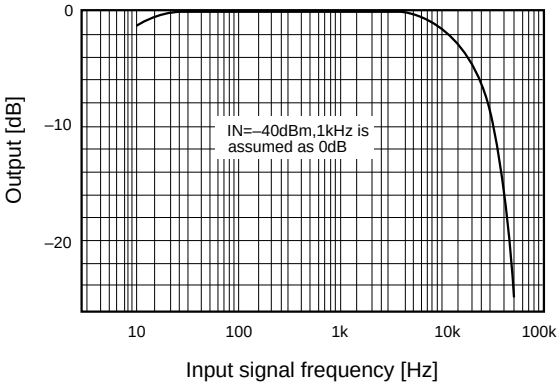

Output vs Distortion 4 CXA1622M BTL mode




Stereo mode frequency characteristics
VIN=–40dBm VOL MAX VCC=3V



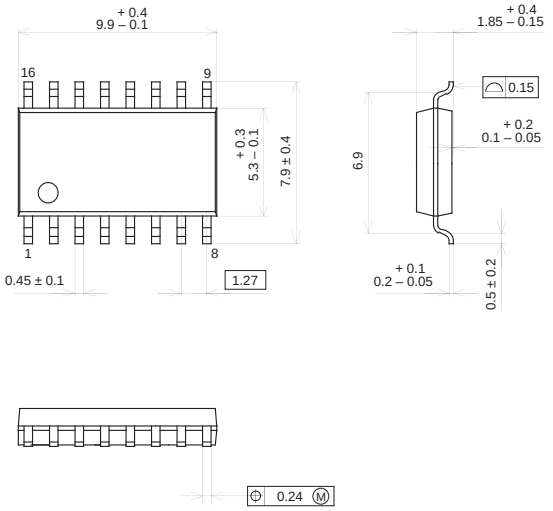

BTL mode frequency characteristics
VIN=–40dBm VOL MAX VCC=3V



**Package Outline** Unit : mm

CXA1622M

16PIN SOP (PLASTIC)



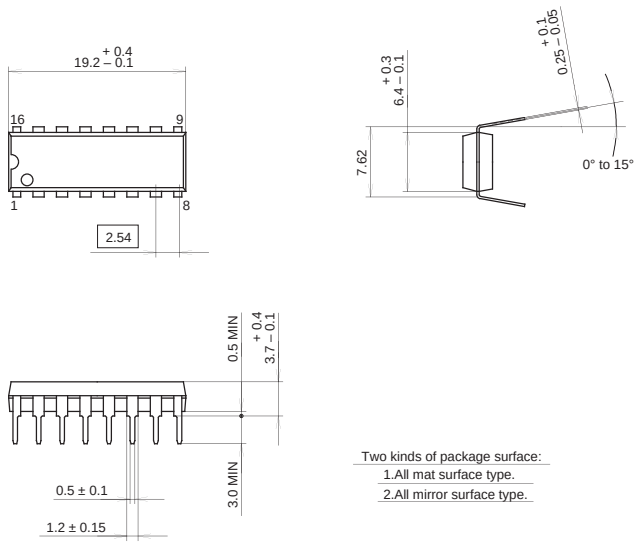

PACKAGE STRUCTURE

| | |
|---|---|
| SONY CODE | SOP-16P-L01 |
| EIAJ CODE | SOP016-P-0300 |
| JEDEC CODE | ———— |

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 0.2g |

CXA1622P

16PIN DIP (PLASTIC)




Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

PACKAGE STRUCTURE

| | |
|---|---|
| SONY CODE | DIP-16P-01 |
| EIAJ CODE | DIP016-P-0300 |
| JEDEC CODE | Similar to MO-001-AE |

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 1.0 g |