SONY

CXA1702AR

4-channel REC/PB Amplifier for 8 mm VCR

Description

The CXA1702AR is a bipolar IC designed as recording/playback amplifiers for Hi8-compatible VCRs.

Features

●Recording/playback system

- Hi8-compatible wideband recording/playback amplifier.
- Enables electric variable resistor (EVR) control.

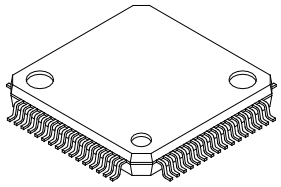
●Recording system

- Feedback damping provided in the recording amplifier and its EVR control function facilitate printed circuit board design.
- Five-input (Y, chroma, AFM, ATF, PCM) mix amplifier and EVR control function for Y/low-band recording level.
- Ramp circuit for the recording amplifier output bias current.

●Playback system

- Feedback dumping provided in the playback amplifier facilitates printed circuit board design.
- Middle-frequency tuner on chip; EVR permits independent adjustment of its center frequency fo, Q and boost amount by EVR.
- RF AGC and dropout detection circuit.

64 pin LQFP (Plastic)



Application

8 mm VCR

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

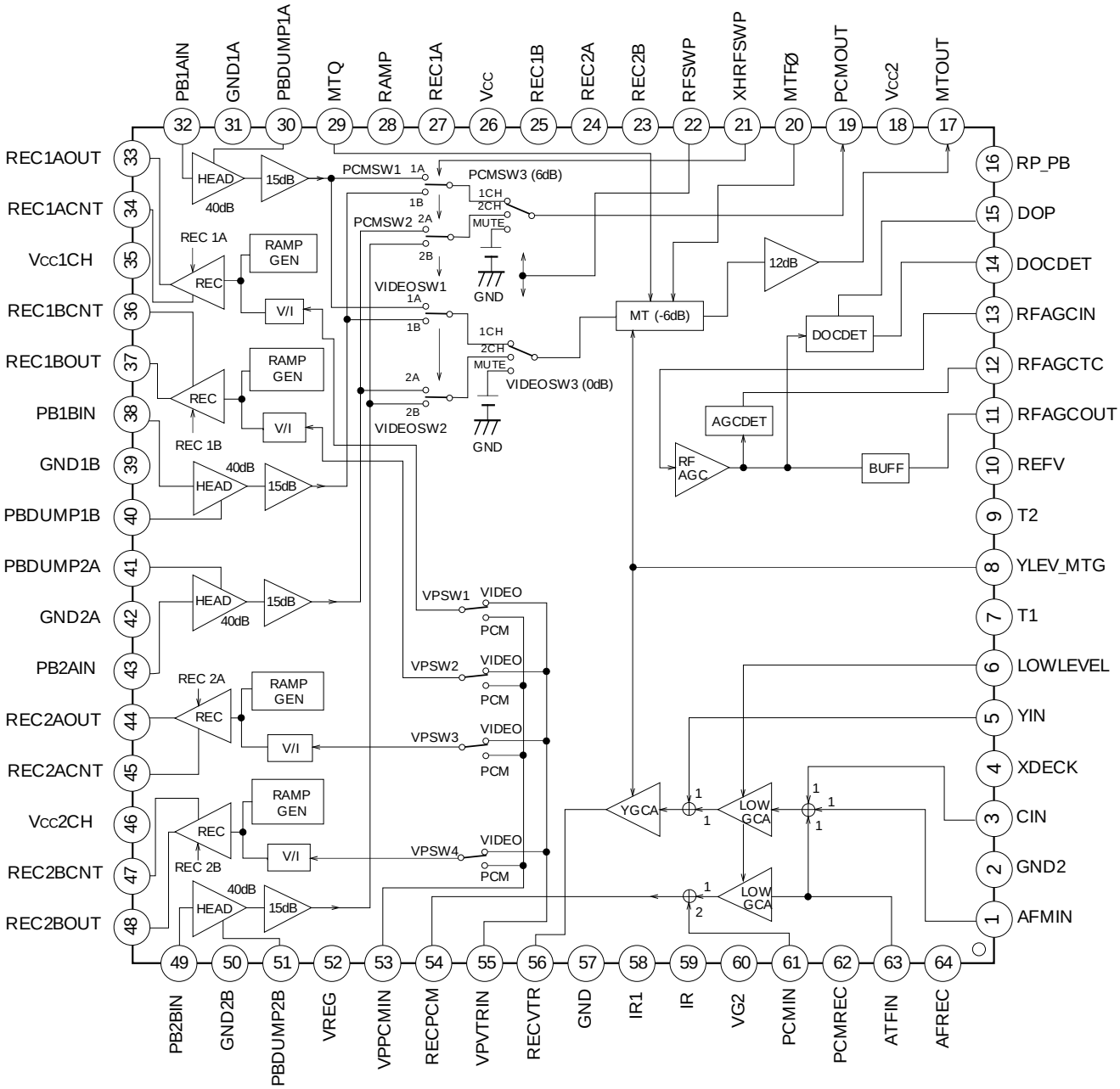
• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–10 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1010 (when mounted on board)	mW

Operating Condition

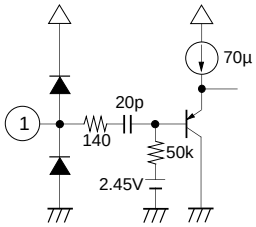
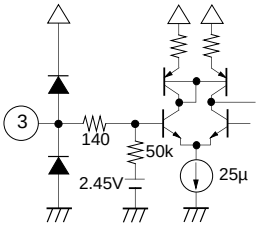
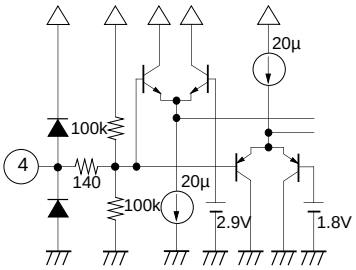
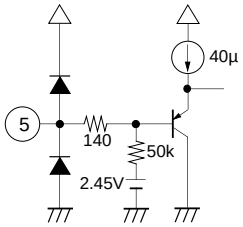
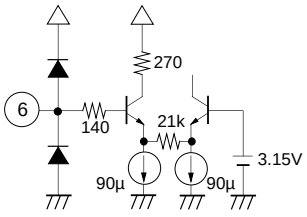
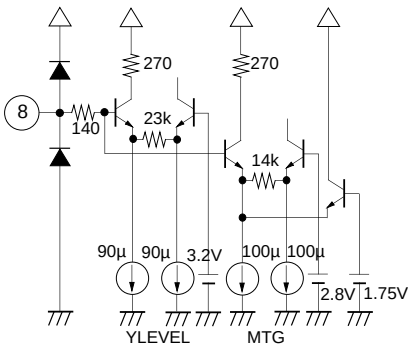
Supply voltage	V_{CC}	$4.75^{+0.5}_{-0.25}$	V

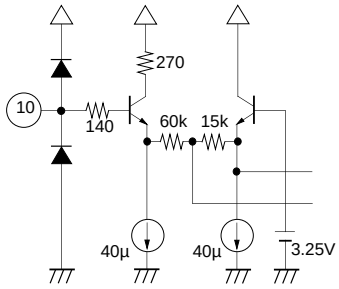
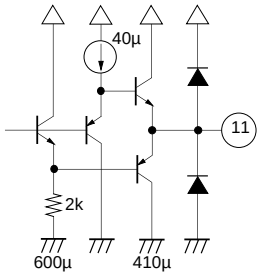
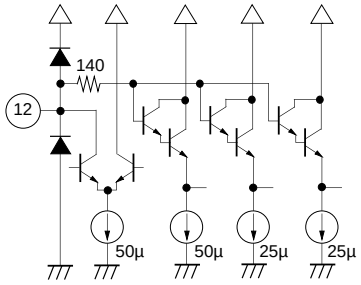
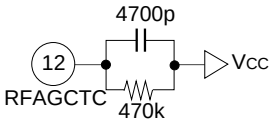
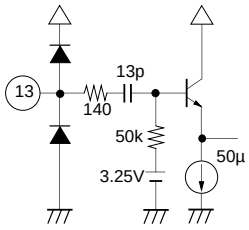
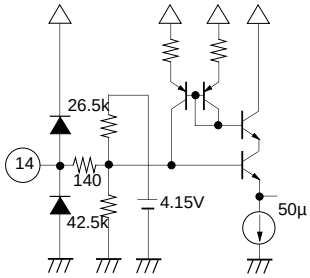
E93Z32-TE

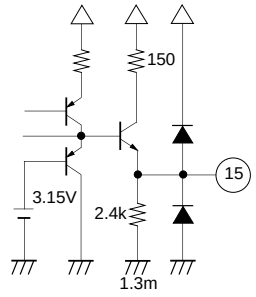
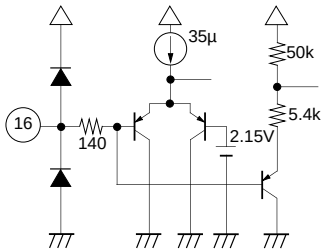
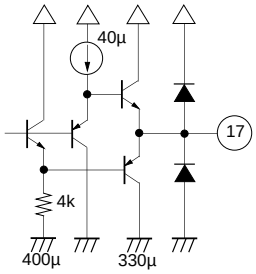
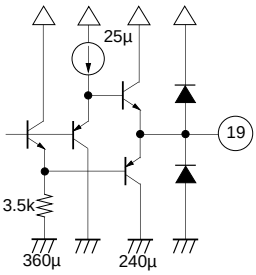
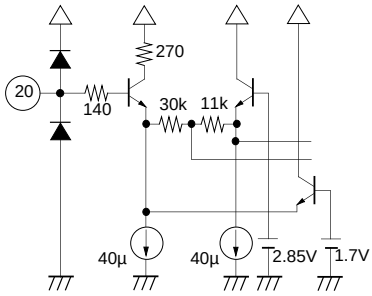
Block Diagram and Pin Configuration

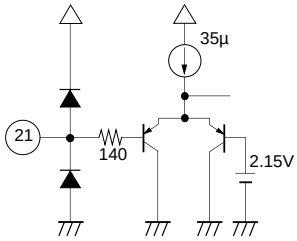
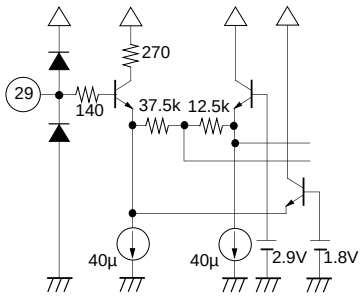


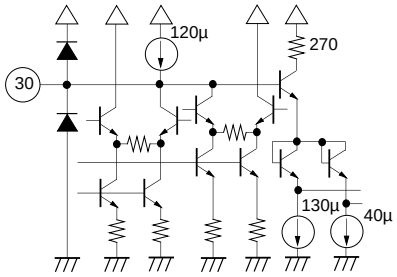
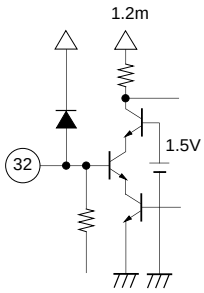
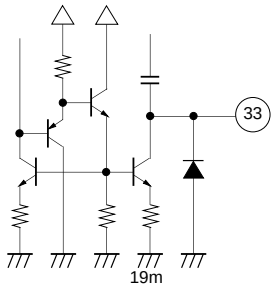
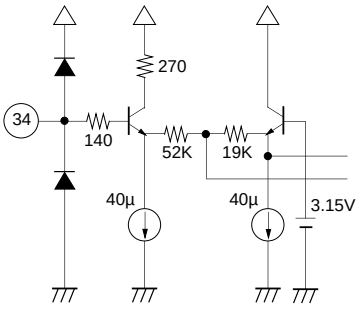
Pin Description (Vcc, Vcc2, Vcc1CH, Vcc2CH=4.75V, Ta=25°C)

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	Description
1	AFM IN	—	125mVp-p input		Input pin for recording AFM signal. Input signal bias should be in the range from 1 V to 3.5 V. Connect to Vcc when the pin is not in use.
2	GND2	0V	—		GND pin
3	CIN	2.45V	500mVp-p input		Input pin for recording chroma signal.
4	XDECK	2.4V (when pin is open) H: 4.3 V or more L: 0.6 V or less input	—		DECK and NORM switching pin H : NORM (4ch) L : Open : } DECK (2ch)
5	YIN	2.45V	500mVp-p input		Input pin for recording Y signal.
6	LOW LEVEL	1.8V to 4.75V input	—		EVR adjusting pin for low-band recording signal (chroma, AFM, video path ATF, PCM path ATF) level. Increasing the input voltage lowers the signal level.
7	T1	—	—	—	Test pin. Set the pin open.
8	YLEV_MTG	1.8V to 4.75V input	—		EVR adjusting pin for recording Y signal level and middle tune boost amount. Adjusts the former during recording and the latter during playback. Increasing the input voltage lowers recording Y signal level and boost amount.

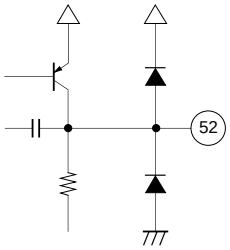
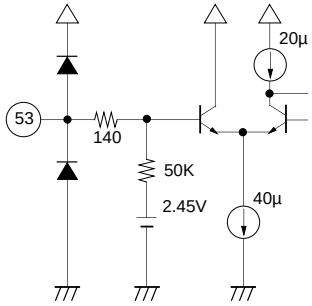
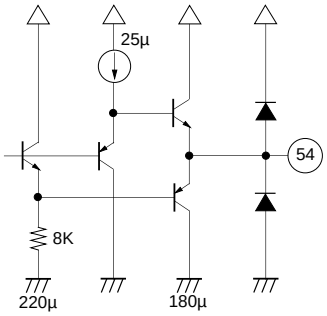
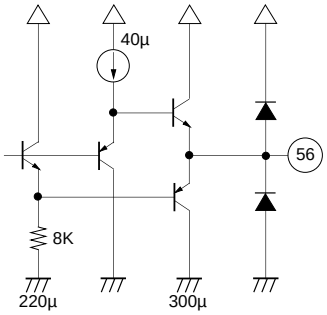
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
9	T2	—	—		Test pin. Connect decoupling capacitance between this pin and GND.
10	REFV	Hi8:4.45V Nor:3.6V input			EVR adjusting pin to decide the adjustment range of middle tune fo. Input the following: Hi8 : 4.45 V Nor : 3.6 V
11	RFAGC OUT	1.9V	400mVp-p output		Output pin for playback Y signal.
12	RFAGCTC	2.5V to 4.75V input (during EVR adjustment)	—		RFAGC time constant pin.  RFAGC gain may be adjusted by EVR. Increasing the input voltage increases gain.
13	RFAGC IN	—	220mVp-p input		Input pin for playback Y signal. Playback Y signal is separated from playback video signal output to Pin 17 (MTOUT), then input to Pin 13 (RFAGCIN). Set input signal bias in the range from 1 V to 3.5 V. Connect to Vcc when this pin is not in use.
14	DOCDET	2.55V (when pin is open)	—		Pin for deciding dropout detection level. Connect decoupling capacitance between this pin and GND. For adjustment, input voltage proportional to Pin 52 (VREG) output voltage. Increasing the input voltage increases the detection level.

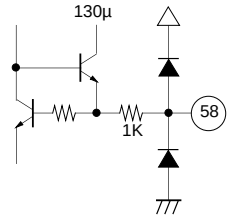
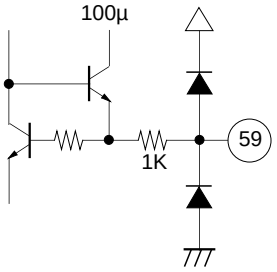
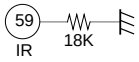
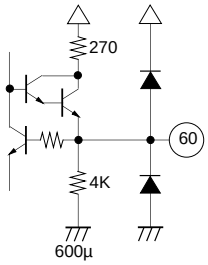
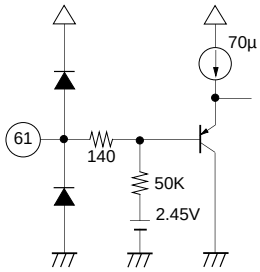
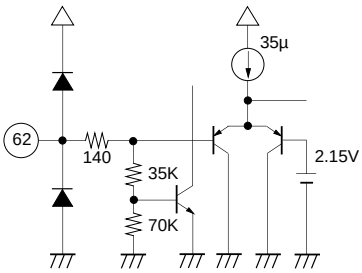
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
15	DOP	H: 3.15V L: 0V output	—		Output pin for dropout detection signal. Goes High at the time of dropout.
16	RP_PB	H: 2.3V or more L: 0.6V or less input	—		Input pin for REC/PB switching signal. H : PB L : REC
17	MTOUT	2.4V	220mVp-p (playback Y signal) output		Output pin for playback video signal.
18	Vcc2	4.75V	—		Power supply pin.
19	PCMOUT	1.95V	220mVp-p output		Output pin for playback PCM signal.
20	MTF0	1.8V to 4.75V input	—		EVR adjusting pin for middle tune fo. Increasing the input voltage increases fo.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
21	XHRFSWP	H: 2.3V or more L: 0.6V or less input	—		Input pin for $\overline{1/2RFSWP}$ signal.
22	RFSWP	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Input pin for RFSWP signal.
23	REC2B	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Goes L during recording and turns on 2Bch recording amplifier output bias current.
24	REC2A	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Goes L during recording and turns on 2Ach recording amplifier output bias current.
25	REC1B	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Goes L during recording and turns on 1Bch recording amplifier output bias current.
26	V_{CC}	4.75V	—	—	Power supply pin for main blocks excluding recording and head amplifiers.
27	REC1A	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Goes L during recording and turns on 1Ach recording amplifier output bias current.
28	RAMP	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21	Goes H during after-recording and turns on recording amplifier output bias current.
29	MTQ	1.8V to 4.75V input	—		EVR adjusting pin for middle tune Q. Increasing the input voltage increases Q.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
30	PBDUMP1A	2.6V	—		Dumping adjusting pin for 1Ach head amplifier. Increasing the external resistance reduces the peaking amount. 
31	GND1A	0V	—	—	GND pin for 1Ach recording and head amplifiers.
32	PB1AIN	0.7V	200µVp-p input		Playback signal 1Ach input pin.
33	REC1A OUT	(19mA output)	(21mAp-p output)		Recording signal 1Ach output pin. Open collector.
34	REC1A CNT	1.8V to 4.75V input	—		EVR adjusting pin for 1Ach recording amplifier dumping. Increasing the input voltage increases the peaking amount.
35	Vcc1CH	4.75V	—	—	Power supply pin for 1Ach and 1Bch recording and head amplifiers.
36	REC1B CNT	1.8V to 4.75V input	—	Same as for Pin 34.	EVR adjusting pin for 1Bch recording amplifier dumping.
37	REC1B OUT	(19mA output)	(21mAp-p output)	Same as for Pin 33.	Recording signal 1Bch output pin. Open collector.
38	PB1BIN	0.7V	200µVp-p input	Same as for Pin 32.	Playback signal 1Bch input pin.

Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
39	GND1B	0V	—	—	GND pin for 1Bch recording and head amplifiers.
40	PBDUMP1B	2.6V	—	Same as for Pin 30.	Dumping adjusting pin for 1Bch head amplifier.
41	PBDUMP2A	2.6V	—	Same as for Pin 30.	Dumping adjusting pin for 2Ach head amplifier.
42	GND2A	0V	—	—	GND pin for 2Ach recording and head amplifiers.
43	PB2AIN	0.7V	200µVp-p input	Same as for Pin 32.	Playback signal 2Ach input pin.
44	REC2AOUT	(19mA output)	(21mAp-p output)	Same as for Pin 33.	Recording signal 2Ach output pin. Open collector.
45	REC2ACNT	1.8V to 4.75V input	—	Same as for Pin 34.	EVR adjusting pin for 2Ach recording amplifier dumping.
46	V_{CC}2CH	4.75V	—	—	Power supply pin for 2Ach and 2Bch recording and head amplifiers.
47	REC2BCNT	1.8V to 4.75V input		Same as for Pin 34.	EVR adjusting pin for 2Bch recording amplifier dumping.
48	REC2BOUT	(19mA output)	(21mAp-p output)	Same as for Pin 33.	Recording signal 2Bch output pin. Open collector.
49	PB2BIN	0.7V	200µVp-p input	Same as for Pin 32.	Playback signal 2Bch input pin.
50	GND2B	0V	—	—	GND pin for 2Bch recording and head amplifiers.
51	PBDUMP2B	2.6V	—	Same as for Pin 30.	Dumping adjusting pin for 2Bch head amplifier.

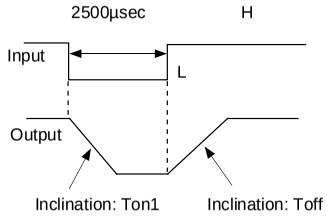
Pin No.	Symbol	Pin voltage		Equivalent circuit	Description
		DC	AC		
52	VREG	4.15V	—		Output pin for 4.15 V regulator. Connect decoupling capacitance between this pin and GND. Up to 0.5 mA current can be led outside IC.
53	VPPCMIN	2.45V	200mVp-p (recording PCM signal) input		VPSW input pin for recording PCM path. Input Pin 54 (RECPCM) signal after cutting DC component with external capacitance.
54	RECPCM	2.4V	200mVp-p (recording PCM signal) output		Output pin for recording PCM path. Outputs signal obtained by mixing recording PCM signal and recording ATF signal.
55	VPVTRIN	2.45V	200mVp-p (recording Y signal) input	Same as for Pin 53.	VPSW input pin for recording video path. Input Pin 56 (RECVTR) signal after cutting DC component with external capacitance.
56	RECVTR	2.4V	200mVp-p (recording Y signal) output		Output pin for recording video path. Outputs signal obtained by mixing recording Y signal, recording chroma signal, recording AFM signal and recording ATF signal.
57	GND	0V	—	—	GND pin for main blocks excluding recording and head amplifiers.

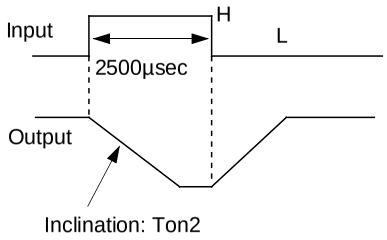
Pin No	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	Description
58	IR1	1.95V (when resistor is connected)	—		Pin for external reference current source. Connect external resistor 15kΩ between this pin and GND. Be careful not to cause cross talk. 
59	IR	1.9V (when resistor is connected)	—		Pin for external reference current source. Connect external resistor 18 kΩ between this pin and GND. Be careful not to cause cross talk. 
60	VG2	2.45V	—		Pin for internal reference voltage source. Connect decoupling capacitance between this pin and GND. Not for outside IC use.
61	PCMIN	2.45V	300mVp-p input		Input pin for recording PCM signal.
62	PCMREC	H: 2.3V or more L: 0.4V or less input	—		PCM recording switching pin. H: PCM recording also, RFAGC gain is held when Pin 16 (RP_PB):H and Pin 62 (PCMREC): H
63	ATFIN	2.45V	125mVp-p input	Same as for Pin 61.	Input pin for recording ATF signal.
64	AFREC	H: 2.3V or more L: 0.6V or less input	—	Same as for Pin 21.	After-recording mode switching pin. H: after-recording

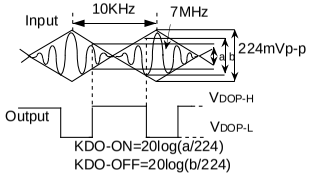
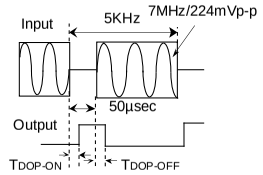
Electrical Characteristics (V_{CC}, $V_{CC}2$, $V_{CC}1CH$, $V_{CC}2CH$ = 4.75 V, Ta = 25 °C, See the Electrical Characteristics Measurement Circuit and the Control Logic Truth Table.

∗Start taking measurement after making adjustment described in Notes on Measurement.)

NO	Item	Symbol	Measurement condition				Measurement pin or ammeter name	Measurement method	Ratings			
			Input condition			Control logic			Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency							
1	Recording circuit current	I_{REC}	—	—	—	A1	I_{VCC}	Current consumption inside IC during recording (including recording amplifier output bias current)	45	64	83	mA
2	Playback circuit current	I_{PB}	—	—	—	J	I_{VCC}	Current consumption inside IC during playback	44	63	82	mA
3	After-recording circuit current	I_{AFREC}	—	—	—	T	I_{VCC}	Current consumption inside IC during after-recording (including recording amplifier output bias current)	68	96	125	mA
4	VREG pin voltage	V_{REG}	—	—	—	S	52	Pin voltage measurement	3.95	4.15	4.35	V
	Recording system											
5	Recording Y signal GCA minimum gain	G_{Ymin}	5	500mV_{P-P}	300KHz	A	56	Pin 8 (YLEV_MTG)=4.75V	—	-16.3	-14.0	dB
6	Recording Y signal GCA maximum gain	G_{Ymax}	5	200mV_{P-P}	300KHz	A	56	Pin 8 (YLEV_MTG)=1.8V	-4.0	-1.7	—	dB
7	Recording Y signal GCA frequency response	V_{FY}	5	500mV_{P-P}	14MHz, 300KHz	A	56	14 MHz level/300 kHz level	-1.5	-0.5	0.5	dB
8	Recording Y signal GCA secondary distortion	D_Y	5	500mV_{P-P}	7MHz	A	56		—	-55	—	dB
9	Low-band signal GCA (video, chroma path) minimum gain	G_{LVmin}	3	500mV_{P-P}	300KHz	A	56	Pin 6 (LOWLEVEL)=4.75V	—	-31.9	-26.5	dB
10	Low-band signal GCA (video, chroma path) maximum gain	G_{LVmax}	3	500mV_{P-P}	300KHz	A	56	Pin 6 (LOWLEVEL)=1.8V	-14.5	-12.4	—	dB
11	Recording chroma path secondary distortion	D_C	3	500mV_{P-P}	750KHz	A	56	When Pin 6 (LOWLEVEL)=1.8 V gain at maximum	—	-50	—	dB
12	Recording AFM path gain	G_{AFM}	1	125mV_{P-P}	1.7MHz	A	56	When Pin 6 (LOWLEVEL)=1.8 V gain at maximum	-14.5	-12.3	—	dB
13	Recording AFM path secondary distortion	D_{AFM}	1	125mV_{P-P}	1.7MHz	A	56	When Pin 6 (LOWLEVEL)=1.8 V gain at maximum	—	-55	—	dB
14	Recording ATF (video path) gain	G_{VATF}	63	125mV_{P-P}	100KHz	A	56	When Pin 6 (LOWLEVEL)=1.8 V gain at maximum	-14.5	-12.3	—	dB
15	Low-band signal GCA (PCM, ATF path) minimum gain	G_{LPmin}	63	125mV_{P-P}	100KHz	A	54	Pin 6 (LOWLEVEL)=4.75V	—	-31.8	-26.5	dB

NO	Item		Symbol	Measurement condition				Measurement pin or ammeter name	Measurement method	Ratings			
				Input condition			Control logic			Min.	Typ.	Max.	Unit
				Input pin	Level	Frequency							
16	Low-band signal GCA (PCM, ATF path) maximum gain		G_{LPmax}	63	125mVp-p	100KHz	A	54	Pin 6 (LOWLEVEL)=1.8V	-14.5	-12.6	—	dB
17	Recording PCM path gain		G_P	61	300mVp-p	300KHz	A	54		-4.5	-3.7	-2.9	dB
18	Recording PCM path frequency response		V_{FP}	61	300mVp-p	14MHz, 300KHz	A	54	14 MHz level/300 kHz level	-0.7	0.1	0.9	dB
19	Recording PCM path secondary distortion		D_P	61	300mVp-p	7MHz	A	54		—	-55	—	dB
20	Recording amplifier output bias current	1A	I_{B1A}	—	—	—	A1	I_{B1A}	DC current measurement 34 pin (REC1ACNT), 45 pin (REC2ACNT), 36 pin (REC1BCNT), 47 pin (REC2BCNT)=3.55V	14.55	18.8	23.05	mA
		2A	I_{B2A}				A2	I_{B2A}					
		1B	I_{B1B}				A3	I_{B1B}					
		2B	I_{B2B}				A4	I_{B2B}					
21	Recording amplifier output current	1A	I_{R1A}	55	200mVp-p	1MHz	A1	33	34 pin (REC1ACNT), 45 pin (REC2ACNT), 36 pin (REC1BCNT), 47 pin (REC2BCNT)=3.55V Output level (Vp-p)/51(Ω)	18.1	20.7	23.3	mAp-p
		2A	I_{R2A}				A2	44					
		1B	I_{R1B}				A3	37					
		2B	I_{R2B}				A4	48					
22	Recording amplifier frequency response	1A	V_{FR1A}	55	200mVp-p	10MHz 1MHz	A1	33	10 MHz level/1 MHz level	—	-0.5	—	dB
		2A	V_{FR2A}				A2	44					
		1B	V_{FR1B}				A3	37					
		2B	V_{FR2B}				A4	48					
23	Ramp rising edge inclination 1	1A	T_{on1}	27	See Measurement method.		A	33		—	32	—	µA/µs
		2A		24				44					
		1B		25				37					
		2B		23				48					
24	Ramp falling edge inclination	1A	T_{off}	27				33		—	32	—	µA/µs
		2A		24				44					
		1B		25				37					
		2B		23				48					

NO	Item		Symbol	Measurement condition				Measurement pin or ammeter name	Measurement method	Ratings			
				Input condition			Control logic			Min.	Typ.	Max.	Unit
				Input pin	Level	Frequency							
25	Ramp rising edge inclination 2	1A	T_{on2}	28	See Measurement method.		R	33		—	17	—	µA/µs
		2A					S	44					
		1B					T	37					
		2B					U	48					
	Playback system												
26	Head amplifier MTOUT gain	1A	G_{V1A}	32	200µVp-p	300KHz	J	17	Pin 8 (YLEV_MTG)=4.75V	58.0	61.5	65.0	dB
		2A	G_{V2A}	43			K						
		1B	G_{V1B}	38			L						
		2B	G_{V2B}	49			M						
27	Head amplifier PCMOUT gain	1A	G_{P1A}	32	200µVp-p	300KHz	M	19		57.7	61.2	64.7	dB
		2A	G_{P2A}	43			J						
		1B	G_{P1B}	38			K						
		2B	G_{P2B}	49			L						
28	RFAGC standard output		V_{AGC1}	13	224mVp-p	7MHz	J	11	Measure output level, applying time constant to Pin 12 (RFAGCTC). Pin 10 (REFV)=4.45V	325	395	465	mVp-p
29	RFAGC cover range High		V_{AGC2}	13	56mVp-p	7MHz	J	11		300	365	—	mVp-p
30	RFAGC cover range Low		V_{AGC3}	13	896mVp-p	7MHz	J	11		—	405	475	mVp-p
31	RFAGC minimum gain		G_{AGC}min	13	1.2Vp-p	7MHz	J	11	Pin 12 (RFAGCTC)=2.7V, Pin 10 (REFV)=4.45V	—	-7.7	—	dB
32	RFAGC maximum gain		G_{AGC}max	13	50mVp-p	7MHz	J	11	Pin 12 (RFAGCTC)=4.75V, Pin 10 (REFV)=4.45V	—	20.1	—	dB

NO	Item	Symbol	Measurement condition				Measurement pin or ammeter name	Measurement method	Ratings			
			Input condition			Control logic			Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency							
33	Dropout detection ON level	K_{DO-ON}	13	See Measurement method.		J	15	Apply time constant to Pin 12 (RFAGCTC). 	-15.5	-12.5	-9.5	dB
34	Dropout detection OFF level	K_{DO-OFF}							-9.5	-6.5	-3.5	dB
35	Dropout pulse Low level	V_{DOP-L}							0	0.01	0.2	V
36	Dropout pulse High level	V_{DOP-H}							2.9	3.15	3.4	V
37	Dropout ON detection time	T_{DOP-ON}	13	See Measurement method.		J	15	Apply time constant to Pin 12 (RFAGCTC). 	—	1.1	—	µs
38	Dropout OFF detection time	$T_{DOP-OFF}$							—	2.0	—	µs

Control Logic Truth Table

Name of control logic condition / Input condition and operation	Control logic input condition											Operation of each section under respective input condition																Operation	Mode
												Recording										Playback									
	⑯ RP_PB	㉗ REC1A	㉕ REC1B	㉔ REC2A	㉓ REC2B	㉘ RAMP	㉒ RFSWP	㉑ XHRFSWP	㊹ AFREC	㉖ PCMREC	④ XDECK	㊻ RECVTR	㊹ RECPCM	VPSW1	VPSW2	VPSW3	VPSW4	㉝ REC1AOUT	㊲ REC1BOUT	㊹ REC2AOUT	㊽ REC2BOUT	PBAmp1A	PBAmp1B	PBAmp2A	PBAmp2B	⑲ PCMOUT	⑰ MTOUT	⑪ RFAGCOUT	DOCDET		
A	L	H	H	H	H	—	—	—	—	L	—	V	P	V	V	V	V	S	S	S	S	×	×	×	×	×	×	×	×	Video REC (power save)	
A1	L	L	H	H	H	—	—	—	—	L	—	V	P	V	V	V	V	V	S	S	S	×	×	×	×	×	×	×	×	Video REC 1A	REC
A2	L	H	H	L	H	—	—	—	—	L	—	V	P	V	V	V	V	S	S	V	S	×	×	×	×	×	×	×	×	2A	
A3	L	H	L	H	H	—	—	—	—	L	—	V	P	V	V	V	V	S	V	S	S	×	×	×	×	×	×	×	×	1B	
A4	L	H	H	H	L	—	—	—	—	L	—	V	P	V	V	V	V	S	S	S	V	×	×	×	×	×	×	×	×	2B	
B	L	L	H	H	H	—	L	H	—	H	H	V	P	P	V	V	V	P	S	S	S	×	×	×	×	×	×	×	×	PCM REC 1A	
C	L	H	H	L	H	—	H	L	—	H	H	V	P	V	V	P	V	S	S	P	S	×	×	×	×	×	×	×	×	2A	
D	L	H	L	H	H	—	L	L	—	H	H	V	P	V	P	V	V	S	P	S	S	×	×	×	×	×	×	×	×	1B	
E	L	H	H	H	L	—	H	H	—	H	H	V	P	V	V	V	P	S	S	S	P	×	×	×	×	×	×	×	×	2B	
F	L	L	H	H	H	—	H	H	—	H	O,L	V	P	P	V	V	V	P	S	S	S	×	×	×	×	×	×	×	×	DECK PCM REC 1A	
G	L	H	L	H	H	—	H	L	—	H	O,L	V	P	V	P	V	V	S	P	S	S	×	×	×	×	×	×	×	×	1B	
H	L	H	H	L	H	—	L	L	—	H	O,L	V	P	V	V	P	V	S	S	P	S	×	×	×	×	×	×	×	×	2A	
I	L	H	H	H	L	—	L	H	—	H	O,L	V	P	V	V	V	P	S	S	S	P	×	×	×	×	×	×	×	×	2B	
J	H	—	—	—	—	—	H	L	L	L	H	×	×	×	×	×	×	×	×	×	×	O	O	O	O	2A	1A	O	O	PB 1A	PB
K	H	—	—	—	—	—	L	L	L	L	H	×	×	×	×	×	×	×	×	×	×	O	O	O	O	1B	2A	O	O	2A	
L	H	—	—	—	—	—	H	H	L	L	H	×	×	×	×	×	×	×	×	×	×	O	O	O	O	2B	1B	O	O	1B	
M	H	—	—	—	—	—	L	H	L	L	H	×	×	×	×	×	×	×	×	×	×	O	O	O	O	1A	2B	O	O	2B	
N	H	—	—	—	—	—	H	L	L	L	O,L	×	×	×	×	×	×	×	×	×	×	O	O	O	O	1B	1A	O	O	DECK PB 1A	
O	H	—	—	—	—	—	H	H	L	L	O,L	×	×	×	×	×	×	×	×	×	×	O	O	O	O	1A	1B	O	O	1B	
P	H	—	—	—	—	—	L	H	L	L	O,L	×	×	×	×	×	×	×	×	×	×	O	O	O	O	2B	2A	O	O	2A	
Q	H	—	—	—	—	—	L	L	L	L	O,L	×	×	×	×	×	×	×	×	×	×	O	O	O	O	2A	2B	O	O	2B	
R	H	—	—	—	—	H	L	H	H	H	H	×	P	P	V	V	V	P	S	S	S	×	O	O	O	Mu	Mu	O	O	PCM after-recording 1A	PCM after-recording
S	H	—	—	—	—	H	H	L	H	H	H	×	P	V	V	P	V	S	S	P	S	O	O	×	O	Mu	Mu	O	O	2A	
T	H	—	—	—	—	H	L	L	H	H	H	×	P	V	P	V	V	S	P	S	S	O	×	O	O	Mu	Mu	O	O	1B	
U	H	—	—	—	—	H	H	H	H	H	H	×	P	V	V	V	P	S	S	S	P	O	O	O	×	Mu	Mu	O	O	2B	
V	H	—	—	—	—	H	H	H	H	H	O,L	×	P	P	V	V	V	P	S	S	S	×	O	O	O	Mu	Mu	O	O	DECK PCM after-recording 1A	
W	H	—	—	—	—	H	H	L	H	H	O,L	×	P	V	P	V	V	S	P	S	S	O	×	O	O	Mu	Mu	O	O	1B	
X	H	—	—	—	—	H	L	L	H	H	O,L	×	P	V	V	P	V	S	S	P	S	O	O	×	O	Mu	Mu	O	O	2A	
Y	H	—	—	—	—	H	L	H	H	H	O,L	×	P	V	V	V	P	S	S	S	P	O	O	O	×	Mu	Mu	O	O	2B	

During DECK PCM after-recording ④ XDECK=O····· Inclination of the rising edge of the recording amplifier output bias current 32µA/µs (typ.)
④ XDECK=L····· Inclination of the rising edge of the recording amplifier output bias current 17µA/µs (typ.)

1. Description of input conditions
H ··· Control logic input voltage 2.3 V or more
L ··· Control logic input voltage 0.6 V or less
—··· Independent of H and L
Only for ④ XDECK
H ··· Control logic input voltage 4.3 V or more (Vcc = 4.75 V)
L ··· Control logic input voltage 0.6 V or less (Vcc = 4.75 V)
O ··· Open
Only for ㊷ PCMREC
H ··· Control logic input voltage 2.3 V or more
L ··· Control logic input voltage 0.4 V or less

2. Description of operation mode
O ···Operating
× ···Not operating
V ···Video signal is output.
P ···PCM signal is output.
S··· Recording amplifier standby. Output bias current is not flowing.
1A ···1Ach playback signal is output. 1B···1Bch playback signal is output.
2A ···2Ach playback signal is output. 2B···2Bch playback signal is output.
Mu···Playback signal is muted during PCM after-recording and, at the same time, RFAGC gain is held.

Rising/Falling Edge Inclination of Recording Amplifier Output Bias Current (typ.)

(See the Control Logic Truth Table.)

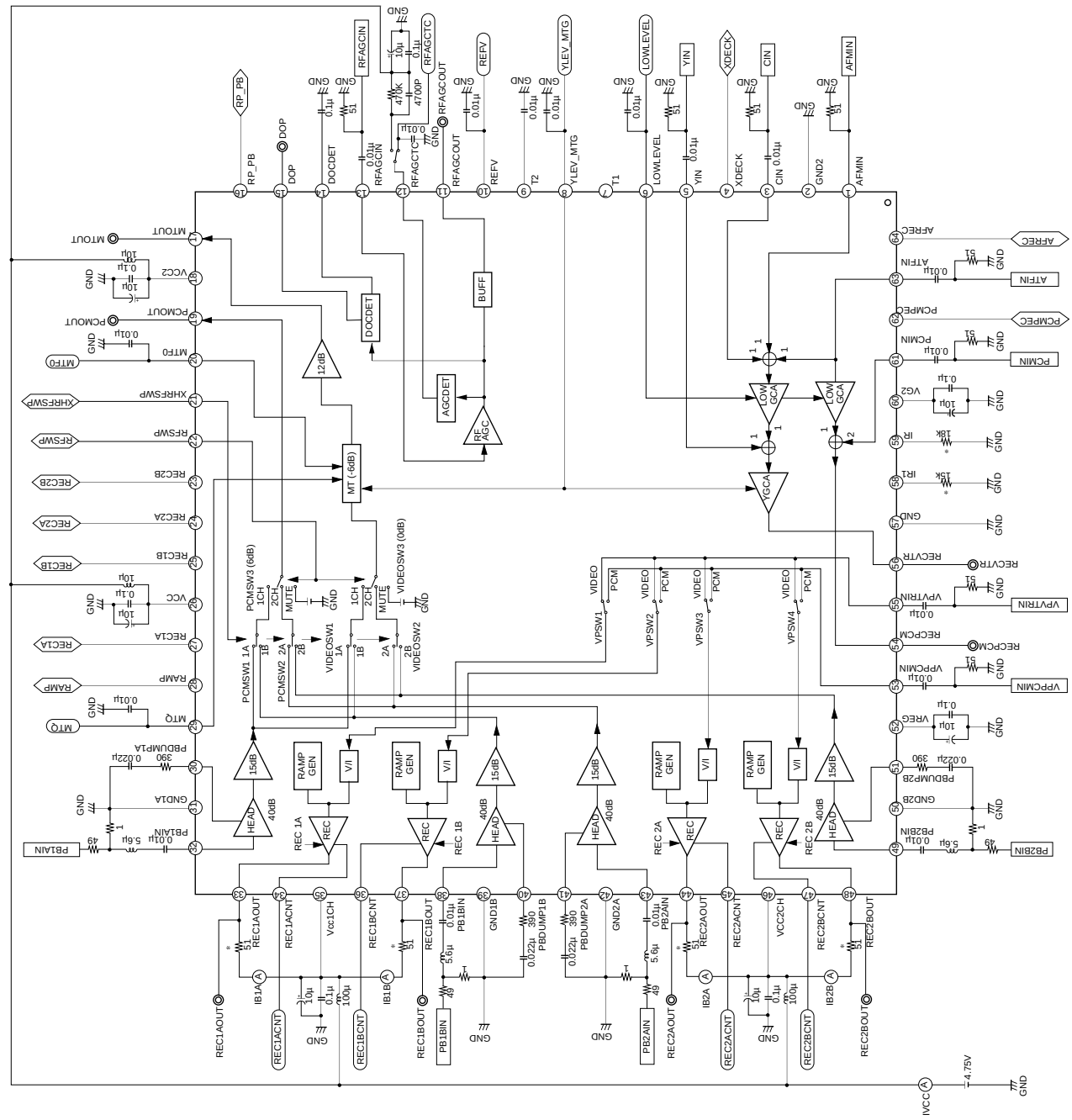
Mode	REC	PCM after-recording		
Operation	—	PCM after-recording	DECK PCM after-recording	
Pin 4 (XDECK)	—	H	O	L
Rising-edge inclination	32µA/µs	17µA/µs	32µA/µs	17µA/µs
Falling-edge inclination	32µA/µs	32µA/µs	32µA/µs	32µA/µs

Notes on Measurement

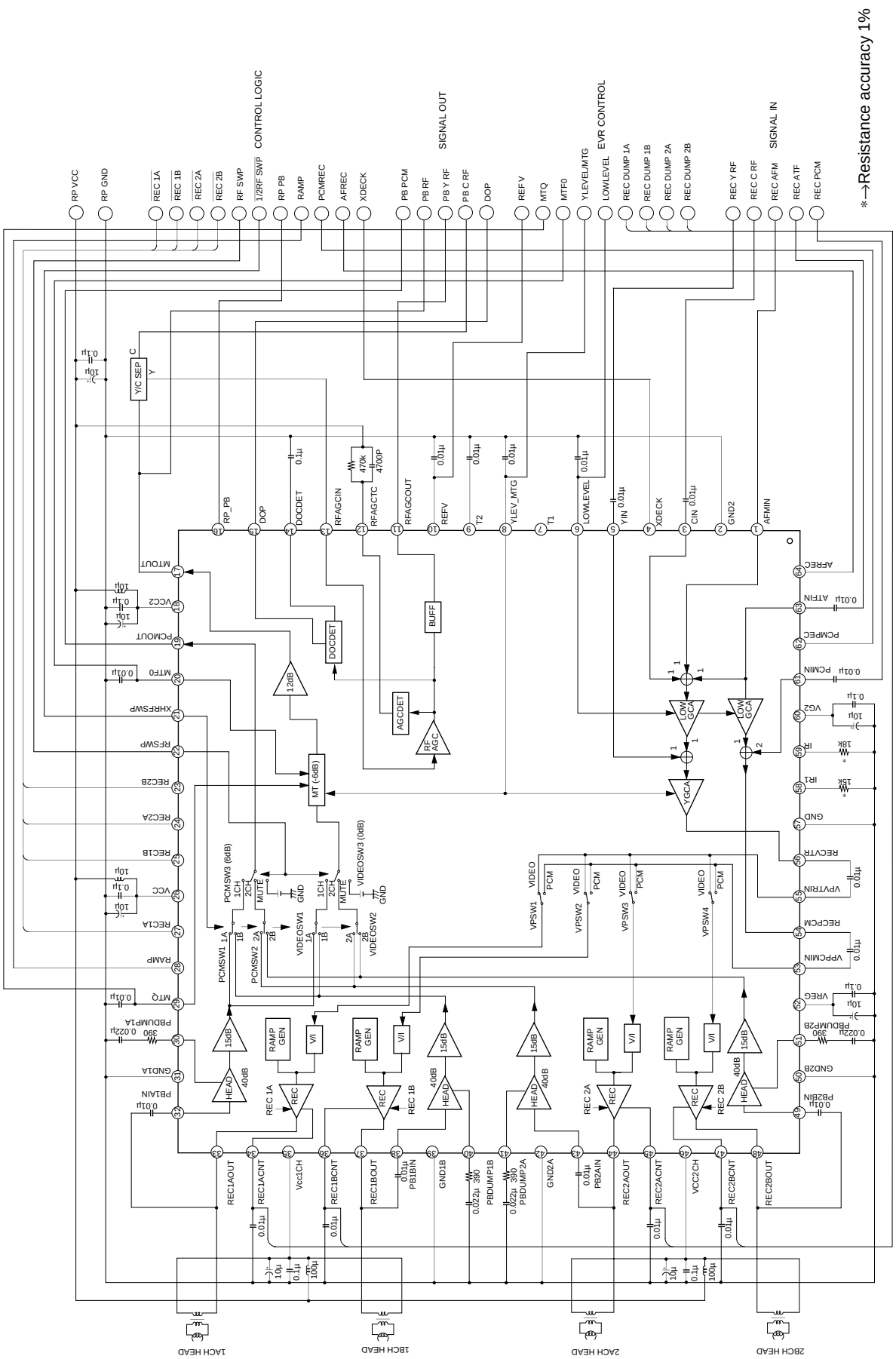
Start taking measurement after making the following adjustment:

Adjust the voltage input to Pin 8 (YLEV_MTG) so that the output level of Pin 56 (RECVTR) reaches 200 mVp-p under the same control logic condition (A) and input condition as those of measurement No. 5. The voltage adjusted here is called Vylev. The voltage input to Pin 8 (YLEV_MTG) is changed in measurement No. 5, 6, and 26. In the other measurement items, set the voltage back to Pin 8 (YLEV_MTG) = Vylev.

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Description of Operation

<Mix amplifier + recording level adjustment>

Y, chroma, AFM, ATF and PCM signals are input at specified levels so that they are mixed internally to achieve an appropriate current value at the head. The video path signal (Y + chroma + AFM + ATF) is output to Pin 56 (RECVTR) and the PCM path signal (PCM + ATF) to Pin 54 (RECPCM). The Y level is EVR-adjusted at Pin 8 (YLEV_MTG) and the low band (chroma, AFM, ATF) level at Pin 6 (LOWLEVEL). The low-band levels of the video path and the PCM path are interlocked in adjustment.

<SW + recording amplifier>

The video path signal and the PCM path signal, which underwent recording level adjustment, are switched at a correct timing, then converted to a current to drive the head.

A feedback dumping circuit is incorporated to inhibit head resonance, and the peaking amount can be adjusted by EVR at Pin 34 (REC1ACNT), Pin 36 (REC1BCNT), Pin 45 (REC2ACNT) and Pin 47 (REC2BCNT).

During recording, the output capacitance is about 12 pF including that of the head amplifier.

<Head amplifier>

The playback signal from the head is amplified with low noise and high gain. A feedback dumping circuit is incorporated to inhibit head resonance, and the peaking amount can be adjusted by external resistors connected to Pin 30 (PBDUMP1A), Pin 40 (PBDUMP1B), Pin 41 (PBDUMP2A) and Pin 51 (PBDUMP2B).

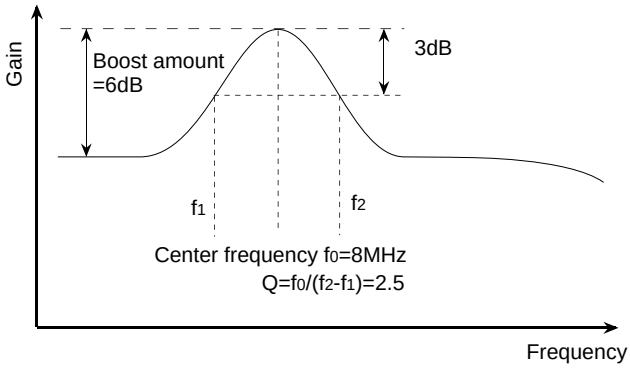
During playback, the input capacitance is about 20 pF including that of the recording amplifier.

<SW + middle tune>

This section switches the playback signals of 1A, 1B, 2A and 2B channels at the correct timing and outputs the playback video signal to Pin 17 (MTOUT) and the playback PCM signal to Pin 19 (PCMOUT). In the PCM after-recording mode, both playback video signal and playback PCM signal are muted during the PCM recording period.

The middle tune circuit corrects the frequency response of the playback video signal.

The center frequency can be adjusted by EVR at Pin 20 (MTF0), Q at Pin 26 (MTQ) and the boost amount at Pin 8 (YLEV_MTG).



The figure to the right shows the center condition that sets fo = 8 MHz, Q = 2.5 and the boost amount = 6 dB. Each control characteristic shown in "Example of Representative Characteristics" is obtained when two of their amount are fixed to the center condition.

<RFAGC>

This circuit inputs the playback Y signal separated from the playback video signal using an external circuit and outputs it at a constant level of 395 mVp-p. In the PCM after-recording mode, RFAGC gain is kept unchanged during PCM recording period.

<Dropout detection>

A dropout is detected in the playback Y signal, and a dropout pulse is output. The detection level is optimized using 224 mVp-p input as a reference. If necessary, the detection level can be adjusted by inputting a DC voltage to Pin 14 (DOCDET). To make this adjustment, input a voltage proportional to the output voltage of Pin 52 (VREG).

<Control logic block>

This IC exercises power-saving control of circuit blocks which are not in immediate need for operation. The IC also incorporates a logic circuit for controlling a number of SWs which change inputs and outputs at complicated timing.

The combinations of input and output in the basic operation are shown in the Control Logic Truth Table.

<Reference voltage in the IC>

VG2 2.45 V and VREG 4.15 V are generated as a reference voltages used in the IC.

VG2 cannot be used outside the IC. VREG cannot also be used outside the IC except for adjusting the dropout detection level at Pin 14 (DOCDET).

Notes on Operation

1. This IC is characterized by high-voltage gain (about 61 dB in the playback system). Be careful of the following when using the IC:

   1) Use reinforced power supply and ground lines. Decouple the power supply pin with a coil and a capacitor. Connect the decoupling capacitor as close to the pin as possible.

   2) Use of a regulator power supply is recommended.

   3) Connecting a capacitive load to the output may cause oscillation.

   4) Take particular care not to make capacitive coupling between the head amplifier input and the playback output. Also be careful not to make capacitive coupling between the recording input and the recording amplifier output.

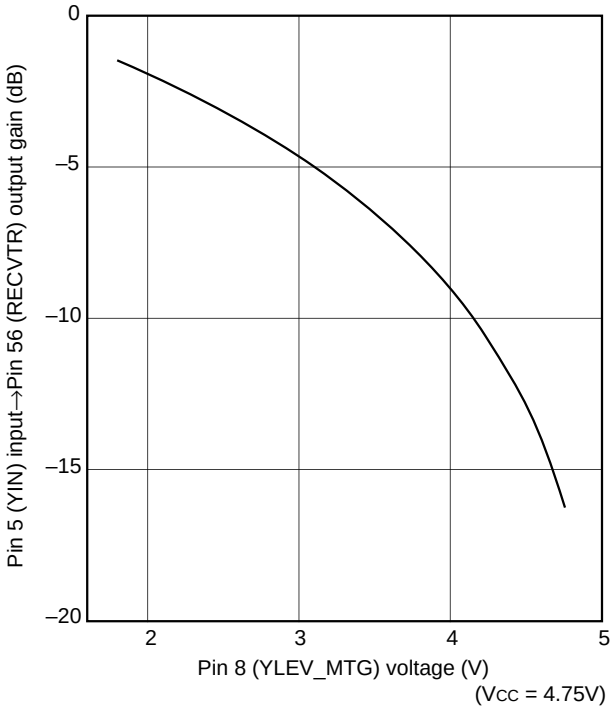
   5) Use of decoupling capacitors is recommended between the following DC voltage input pins and GND. When the control voltage source is at high impedance, aggravation of cross talk or oscillation is feared to occur.
      Pin 6 (LOWLEVEL), Pin 8 (YLEV_MTG), Pin 10 (REFV), Pin 12 (RFAGCTC) [not when time constant is connected], Pin 14 (DOCDET), Pin 20 (MTF0), Pin 29 (MTQ), Pin 34 (REC1ACNT), Pin 36 (REC1BCNT), Pin 45 (REC2ACT), Pin 47 (REC2BCNT)

   6) When a decoupling capacitor is necessary for other pins (not power supply pin), it is recommended to connect each decoupling capacitor as close to the pin as possible.

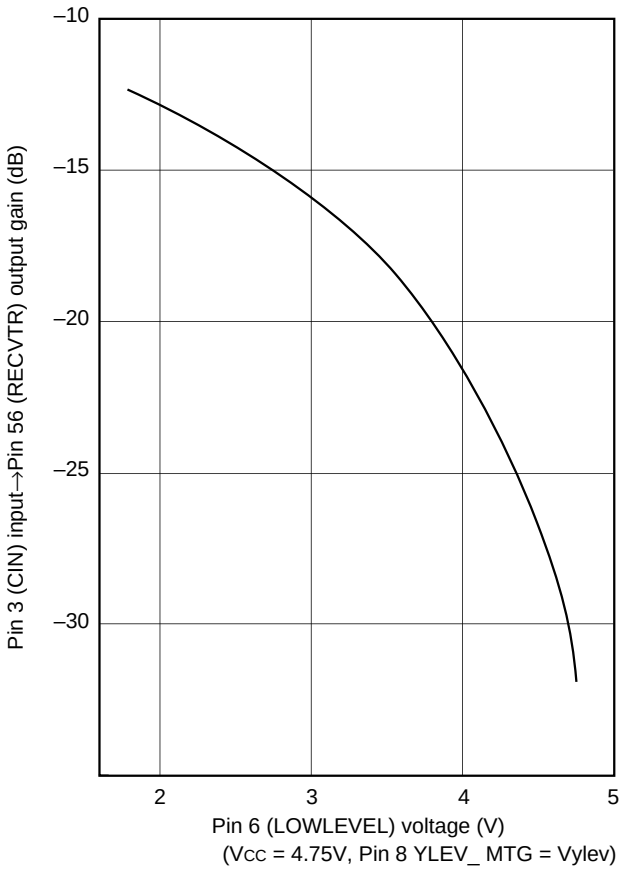
2. The voltage input to the EVR adjusting pin should be proportional to the supply voltage Vcc. Control the input voltage in the range from 1.8 V to 4.75 V when Vcc = 4.75 V.
   For EVR adjustment at Pin 12 (RFAGCTC), control the input voltage in the range from 2.5 V to 4.75 V.

3. During normal playback, Pin 16 (RP_PB) is set H, and Pin 64 (AFREC) is set L. At this time, be careful that taking the signal H at Pin 62 (PCMREC) holds RFAGC gain.

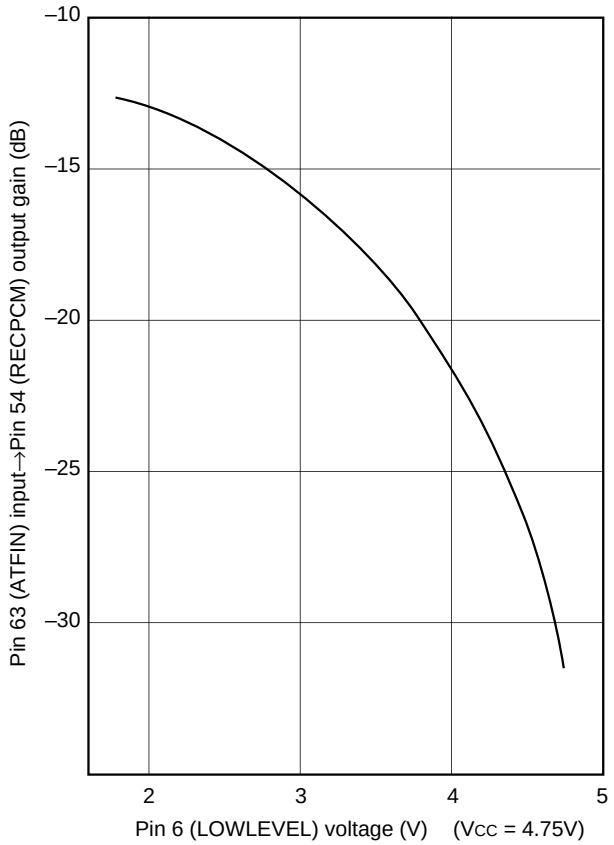
Y signal GCA gain control



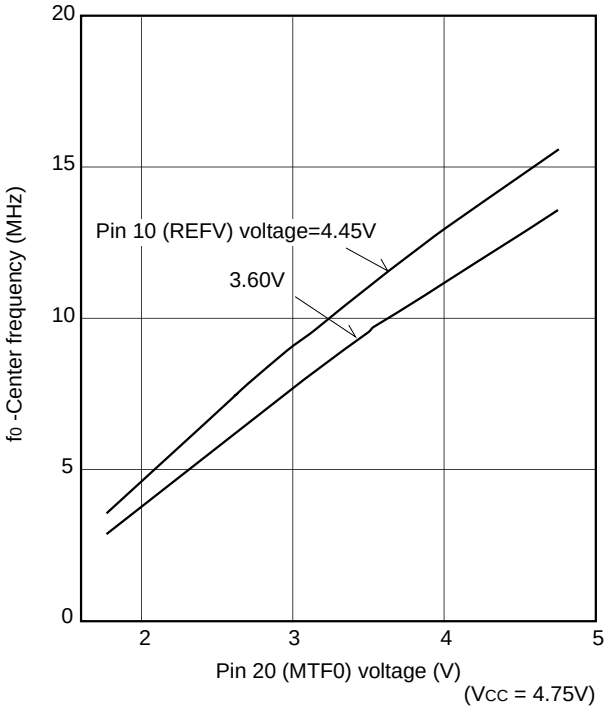
Low-band signal GCA (video, chroma path) gain control



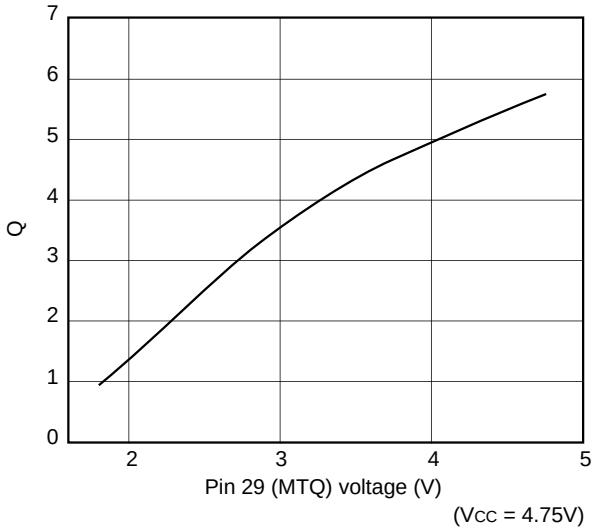
Low-band signal GCA (PCM, ATF path) gain control



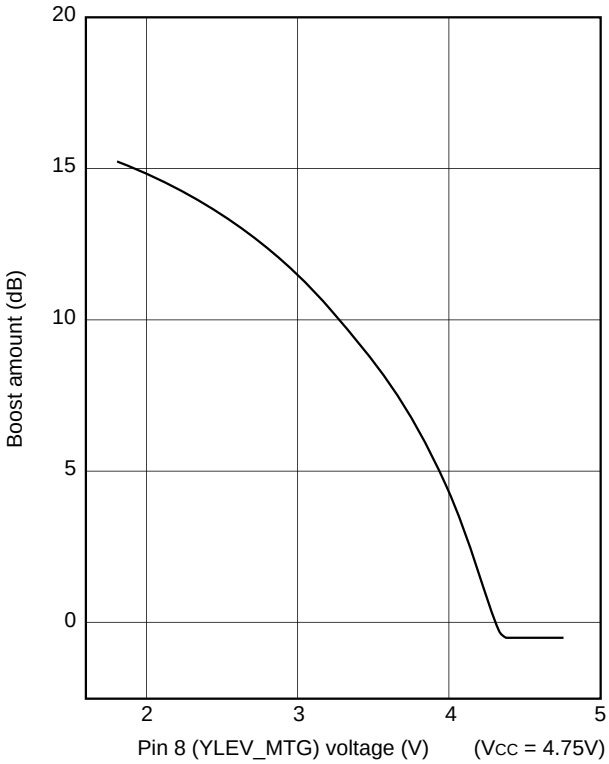
Middle tune fo control



Middle tune Q control

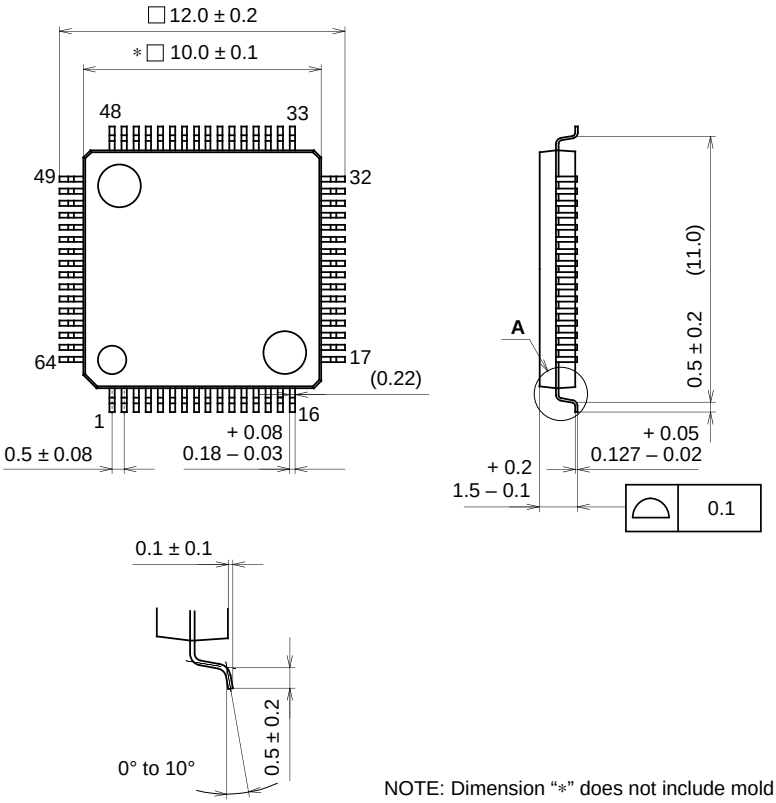


Middle tune boost amount control



Package Outline Unit : mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-64P-L01
EIAJ CODE	∗QFP064-P-1010-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g