SONY

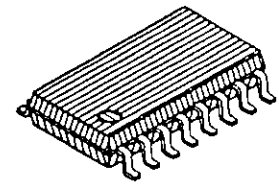
CXD2107M

Hi8 System Detection IC

Description

The CXD2107M is a Hi8 system detection IC that uses composite sync and RF signal input to determine whether the Hi8 system or the standard 8 mm system is being used.

16 pin SOP (Plastic)



Features

- TTL level-compatible at I/O level
- Single 5V power supply

Applications

Hi8 system detection

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C)

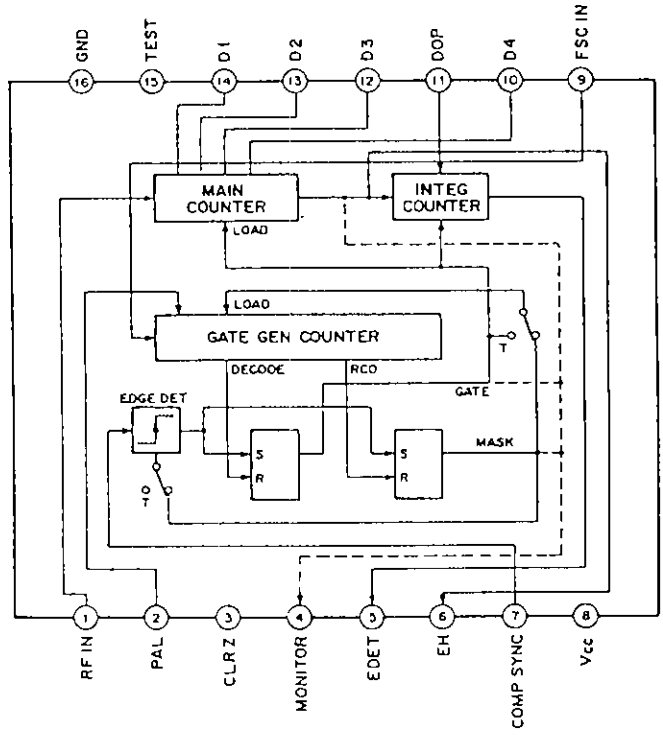
• Supply voltage	V_{DD}	Vss–0.5 to +7.0	V
• Input voltage	V_I	Vss–0.5 to V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

* Vss=0V

Recommended Operating Conditions

• Supply voltage	V_{DD}	+4.5 to +5.5	V
• Operating temperature	Topr	–20 to +75	°C

Block Diagram



E90116 - ST

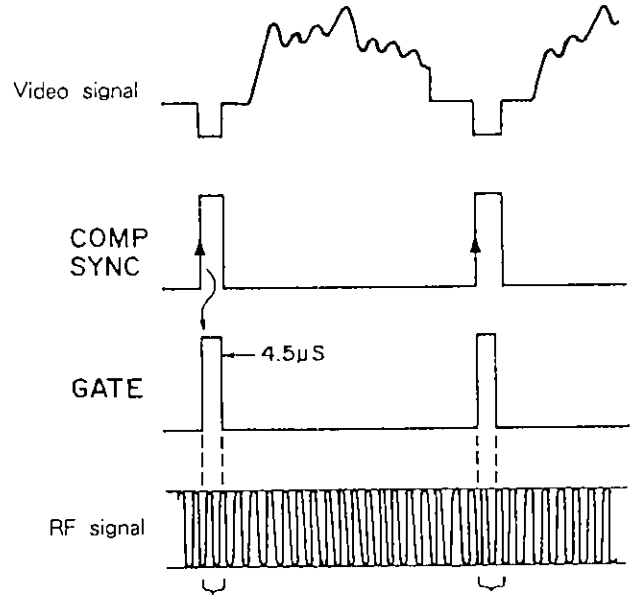
Description of Functions

This IC counts the number of pulses in the RF signal during the composite sync interval in order to discriminate between E (Hi8) mode and L (standard) mode.

Theoretical values (4.5 µs interval during composite sync)

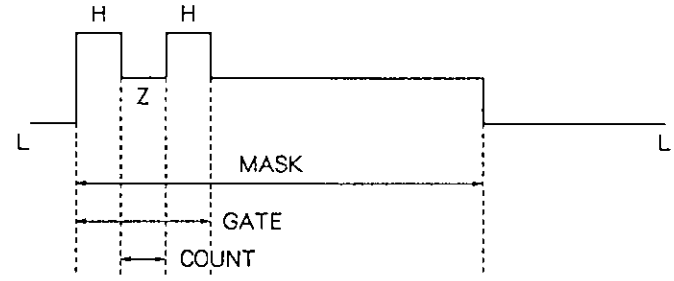
8mm (standard)	19
(Hi8)	26
VHS	15
S-VHS	24

An approximately 4.5 µs interval gate is created using the rising edge of COMP SYNC as a reference.
The count value can be changed according to the settings of D1 through D4 pins, and when the number of pulses in the RF signal exceeds the count value, the EH pin is judged to be high.
For example, by setting the count value between 19 and 26 for an 8 mm VCR, it is possible to discriminate between standard and Hi8.
In addition, for EDET, mode discrimination is made when either L mode or E mode continues for 16H. If the mode does not continue for 16H, the internal counter is reset and the count is restarted. In such instances, the previous mode is held.



E/L discrimination is made by counting the number of pulses in the RF signal corresponding to the Sync Tip portion.

Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>1</td><td>RFIN</td><td>I</td><td>PBY RF signal input.</td></tr>
<tr><td>2</td><td>PAL</td><td>I</td><td>PAL/NTSC switching. High: PAL; Low: NTSC</td></tr>
<tr><td>3</td><td>CLRZ</td><td>I</td><td>Internal counter clear. Normally high.</td></tr>
<tr><td>4</td><td>MONITOR</td><td>O
3STATE</td><td>Monitor of GATE pulse, MASK pulse and counter output pulse.
 
</td></tr>
<tr><td>5</td><td>EDET</td><td>O</td><td>E discrimination output. Output 16H continuous detection for EH output.
High: E mode; Low: L mode</td></tr>
<tr><td>6</td><td>EH</td><td>O</td><td>E discrimination output monitored in 1H units. High: E mode; Low: L mode</td></tr>
<tr><td>7</td><td>COMPSYNC</td><td>I</td><td>Composite sync input.</td></tr>
<tr><td>8</td><td>Vcc</td><td></td><td>Power supply (+5V)</td></tr>
<tr><td>9</td><td>FSCIN</td><td>I</td><td>Color subcarrier (fsc) input. Used as reference clock.
NTSC: 3.579545MHz; PAL: 4.433619MHz</td></tr>
<tr><td>11</td><td>DOP</td><td>I</td><td>Drop-out compensation pulse input. EDET output is maintained when high.</td></tr>
<tr><td>10</td><td>D4</td><td>I</td><td rowspan="4">MAIN COUNTER DATA setting.
<table>
<tr><td>D1</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>D2</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>D3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>D4</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>Count</td><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td></tr>
</table></td></tr>
<tr><td>12</td><td>D3</td><td>I</td></tr>
<tr><td>13</td><td>D2</td><td>I</td></tr>
<tr><td>14</td><td>D1</td><td>I</td></tr>
<tr><td>15</td><td>TEST</td><td>I</td><td>TEST control input. Composite sync input MASK is turned off when high.
Normally low.</td></tr>
<tr><td>16</td><td>GND</td><td></td><td>GND.</td></tr>
</table>

Electrical Characteristics

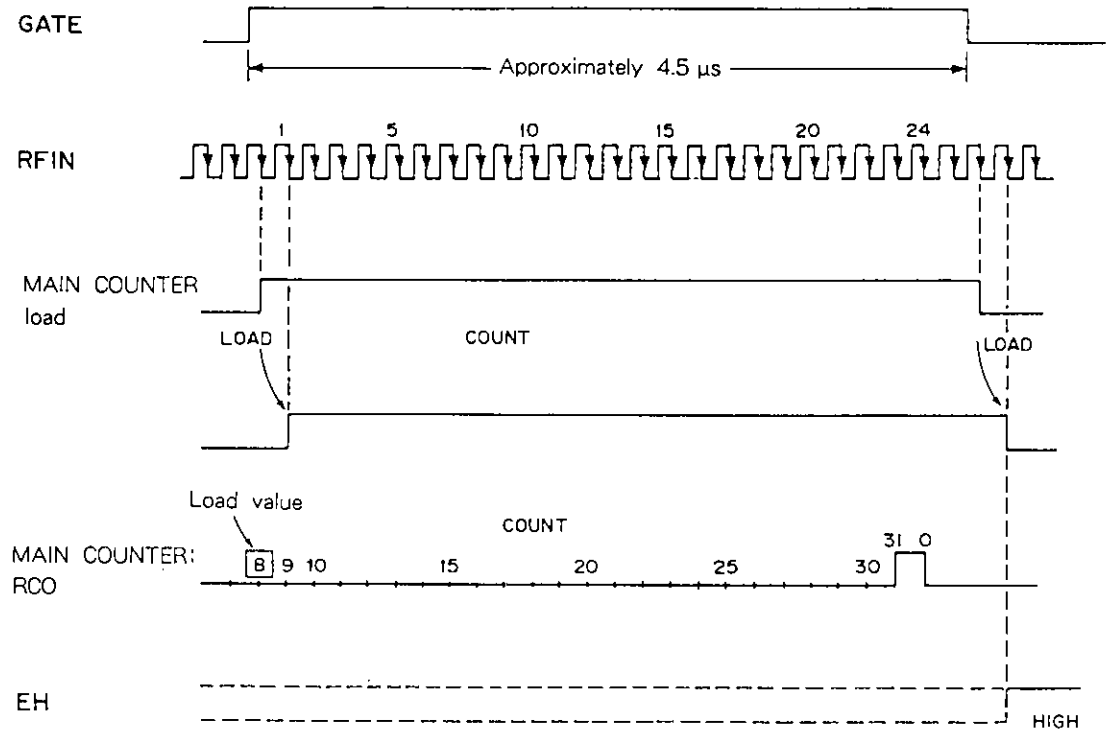
• DC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_{IHT}	TTL input cell	2.2			V
	V_{ILT}				0.8	V
Input amplitude	V_{IN}	RFIN and FSCIN pin *	0.3			Vp-p
Output voltage	V_{OH}	I_{OH}=–4mA	3.7			V
	V_{OL}	I_{OL}=4mA			0.4	V
Input leak current	I_{LI}		–10		10	µA
Output leak current	I_{OZ}		–40		40	µA

* Maximum input frequency: 10MHz

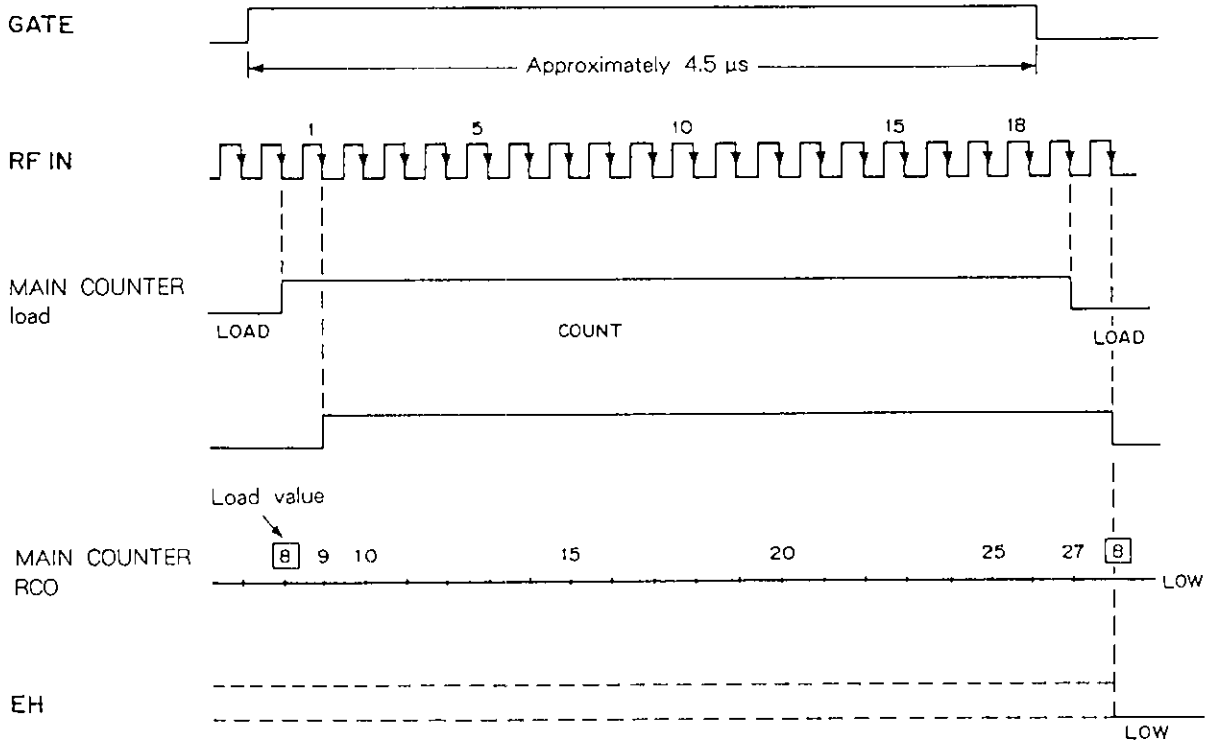
Timing Chart (1)



For Hi8 (In the example where MAIN COUNT is 24, D1 to 3 are low and D4 is high.)

* When Hi8 is being used, the MAIN COUNTER counts 24 pulses and EH is high.

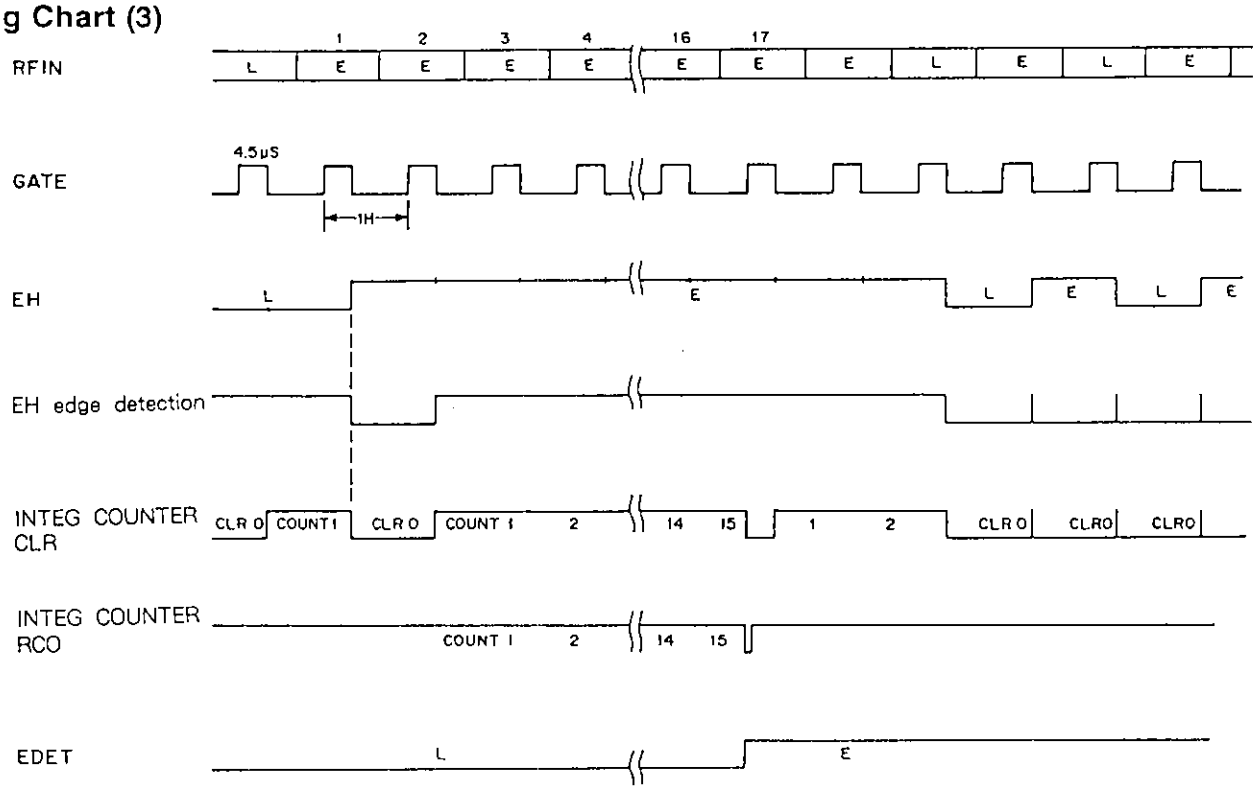
Timing Chart (2)



For standard (In the example where MAIN COUNT is 24, D1 to 3 are low and D4 is high.)

* When standard is being used, the MAIN COUNTER can not count 24 pulses and EH is low.

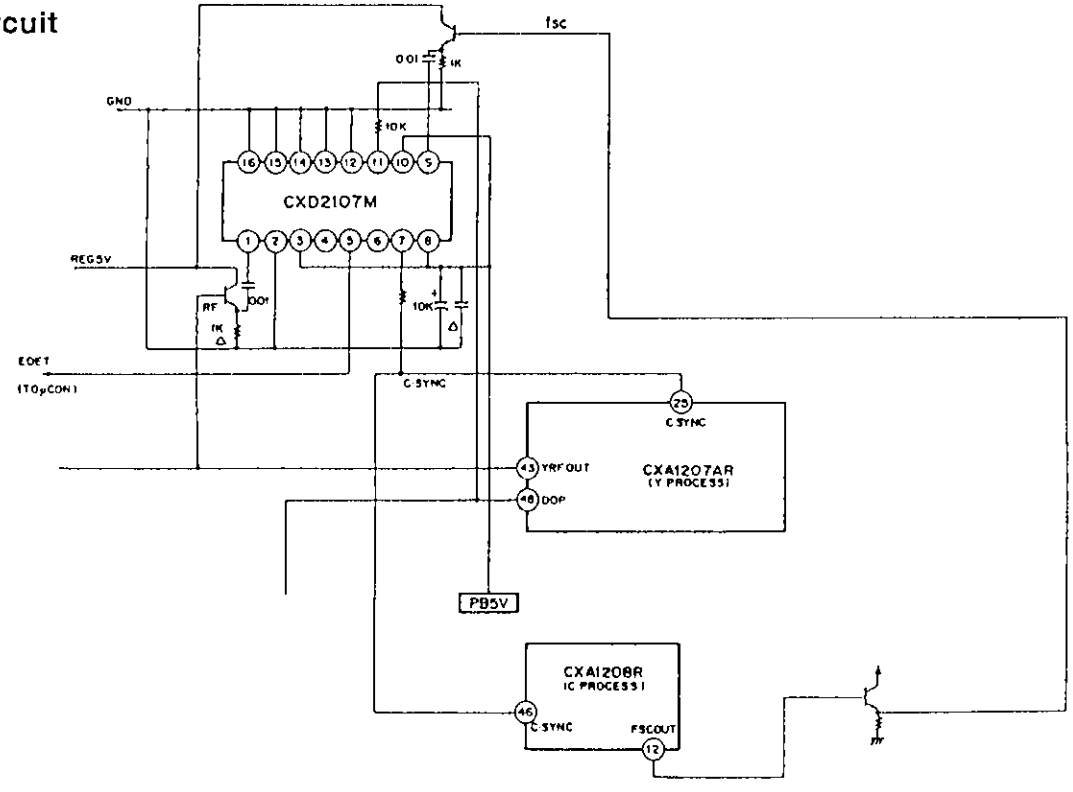
Timing Chart (3)



EDET output (16H continuous discrimination)

* If EH output is fixed at one level for 16H continuously, EDET is judged to be E or L. If the level is not fixed for 16H continuously, the previous judgment is maintained.

Application Circuit

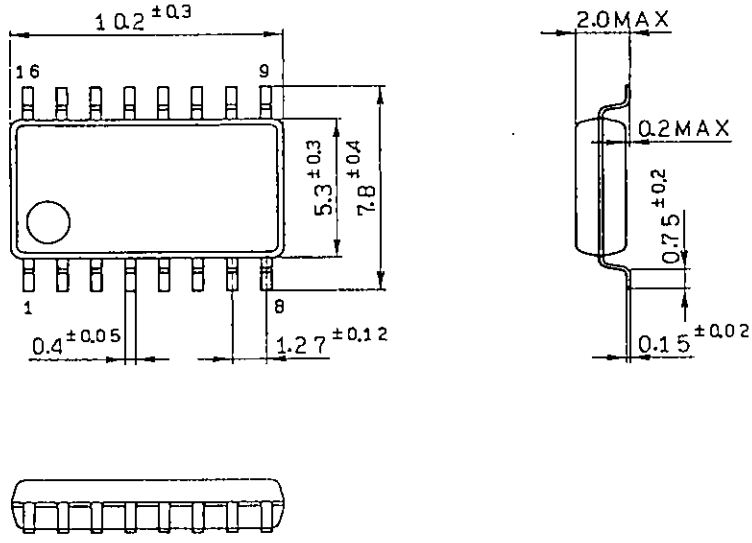


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit : mm

16pin SOP (Plastic) 300mil



SONY NAME	SOP-16P-L121
EIAJ NAME	*SOP016-P-0300-AX
JEDEC CODE	———