HI2555, CXD2555

September 1997

NOT RECOMMENDED FOR NEW DESIGNS

1-Bit, AD/DA Converter For Audio Application

Features

- **Two-Channel AD/DA Converters and Their Respective Digital Filters for Decimation and Oversampling Into a Single Chip**
- **Peripheral Analog Circuits for AD Converter Greatly Reduces External Elements**
- **Distortion (Typ)**
  - **ADC 0.01%**
  - **DAC . . . . . 0.008% (-3dB)**
- **S/N Ratio (Typ)**
  - **ADC 86dB**
  - **DAC 96dB**
- **Ripple in the Digital Filter Pass Band . . . . . ±0.05dB**
- **Attenuation in the Digital Filter Stop Band . . . . . .-45dB**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2555JCQ	-20 to 75	48 Ld MPQF	Q48.12x12-S
CXD2555Q	-20 to 75	48 Ld MPQF	Q48.12x12-S

Description

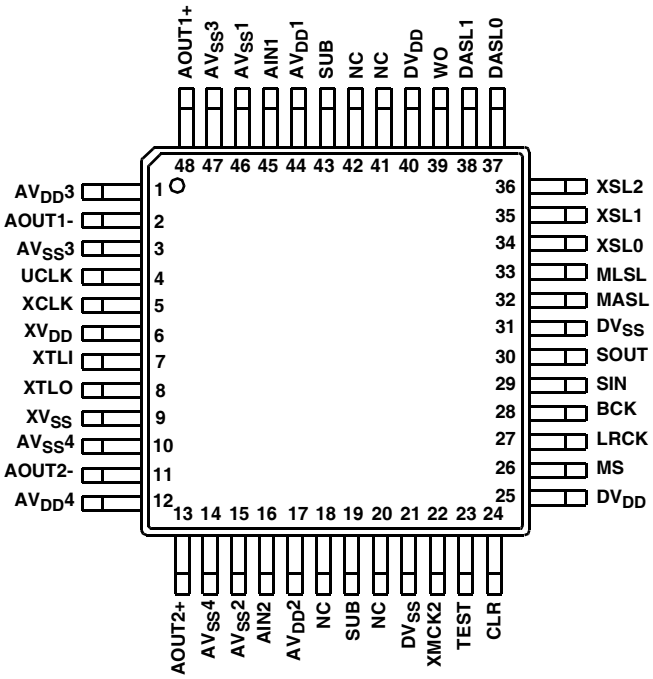
The HI2555, CXD2555 is a 1-bit stereo AD/DA converter featuring a 2nd-order DA system noise shaper. This LSI has also built-in digital filters and provides good cost performance.

Functions

- **Data Can Be Input/Output at Rate of 1 x f_S with a Built-In Digital Filter**
- **Simple Connection of Multiple HI2555, CXD2555s Enable Multi-Channel System**
- **The 32-Slot Serial Data Interface Enables Independent Selection of Data Frontward Packing/Rearward Packing and MSB First/LSB First**
- **The Master Clock is Applicable to Four Sources**
- **256f_S, 512f_S, 768f_S, and 1024f_S**
- **The Sampling Frequency May be Adjusted to Low f_S Frequencies Such as 16kHz or 8kHz, in Addition to Normal Ones of 48kHz, 44.1kHz, and 32Hz**
- **Various Frequency Divider Clocks Can Be Output for LSIs Chips Connected**

Pinout

HI2555, CXD2555 (48 LEAD MQFP)
TOP VIEW



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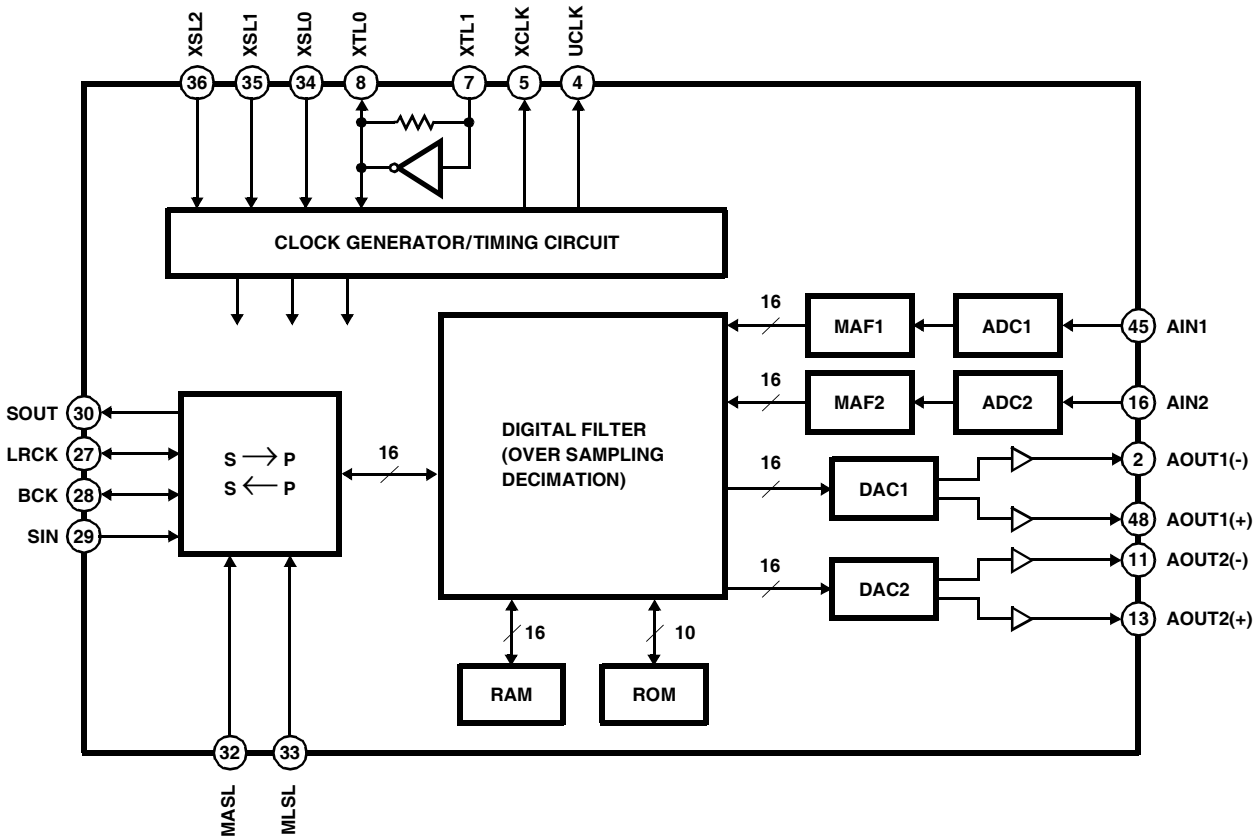
Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	AV_{DD} 3	-	Analog power supply for Channel-1 DA converter.
2	AOUT1(–)	O	Analog opposite-phase output of Channel-1 DA converter
3	AV_{SS} 3	-	Analog GND for Channel-1 DA converter.
4	UCLK	O	Outputs a 1/2 frequency divider of the clock input form the oscillator pin XTLI (Pin 7). User clock output for externally connected ICs.
5	XCLK	O	256 f_S clock output. this provides the master clock for ICs operating in the slave mode when multiple CXD255Qs are connected. (When XSL2 = Low)
6	XV_{DD}	-	Digital power supply for the master clock.
7	XTLI	I	Crystal oscillator circuit input. Connects the crystal oscillator selected by the crystal selection pins XSLO to 2 (Pins 34, 35, and 36). Used to input the master clock from external.
8	XTLO	O	Crystal oscillator circuit output. Connects the crystal oscillator selected by the crystal selection pins XSLO to 2 (Pins 34, 35, and 36).
9	XV_{SS}	-	Digital GND for the master clock.
10	AV_{SS} 4	-	Analog GND for Channel-2 DA converter.
11	AOUT2(-)	O	Analog opposite-phase output for Channel-2 DA converter.
12	AV_{DD} 4	-	Analog power supply for Channel-2 DA converter.
12	AOUT2 (+)	O	Analog in-phase output for Channel-2 DA converter.
14	AV_{SS} 4	-	Analog GND for Channel-2 DA converter.
15	AV_{SS} 2	-	Analog GND for Channel-2 AD converter.
16	AIN2	I	Analog input for Channel-2 AD converter.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	DESCRIPTION
17	AV_{DD} 2	-	Analog power supply for Channel-2 AD converter.
18	NC	-	
19	SUB	-	Connected to the IC internal circuit board (same electric potential as power supply). Connect to GND on the printed circuit board via a capacitor.
20	NC	-	
21	DV_{SS}	-	Digital GND.
22	XMCK2	O	IC measurement. Low is output normally.
23	TEST	I	Test pin. Normally fixed to Low. Equipped with a pull-down resistor.
24	CLR	I	System clear input. Normally High; cleared when Low. Equipped with a pull-up resistor.
25	DV_{DD}	-	Digital power supply.
26	MS	I	Master/slave mode switching input. Master mode when High; slave mode when Low. Equipped with a pull-up resistor.
27	LRCK	I/O	Serial I/O sampling frequency clock. Output i master mode (Pin 26 = High); input in slave mode (Pin 26 = Low). Transfers Channel-1 data when high, and Channel-2 data when Low.
28	BCK	I/O	Serial bit transfer clock (64 f_S) for serial input data SIN and serial output data SOUT. Output in master mode (Pin 26 = High); input in slave mode (Pin 26 = Low). Serial input data is retrieved at the rising edge; serial output data is transferred at the falling edge.
29	SIN	I	Two channels per sampling serial data input. Data format is represented by 2's complements, and consists of 32-bit slots.
30	SOUT	O	Two channels per sampling serial data input. Data format is represented by 2's complements, and consists of 32-bit slots.
31	DV_{SS}	-	Digital GND.
32	MASL	I	Selects whether 16-bit serial data is place din the first 16-bit or the second 16-bit slots of the serial I/O 32-bit slots. Forward packing when High; rearward packing when Low.
33	MLSL	I	Selects whether 16-bit serial data is input/output at LSB-first or MSB-first. MSB-first when High; LSB-first when Low.
34	XSL0	I	Crystal selection. Selects the clock frequency to be input from XTLI (Pin 7) using three bits, XSL 0 to 2.
35	XSL1	I	Crystal selection. Selects the clock frequency to be input from XTLI (Pin 7) using three bits, XSL 0 to 2.
36	XSL2	I	Crystal selection. Selects the clock frequency to be input from XTLI (Pin 7) using three bits, XSL 0 to 2.
37	DASL0	I	IC measurement. Normally fixed to High.
38	DASL1	I	IC measurement. Normally fixed to Low.
39	WO	I	Synchronization window open input. Window masked when High; window open when Low (forced synchronization). Equipped with a pull-up resistor.
40	DV_{DD}	-	Digital power supply
41	NC	-	
42	NC	-	
43	SUB	-	Connected to the IC internal circuit board (same electric potential as power supply). Connect to GND on the printed circuit board via a capacitor.
44	AV_{DD} 1	-	Analog power supply for Channel-1 AD converter.
45	AIN1	I	Analog input for Channel-1 AD converter.
46	AV_{SS} 1	-	Analog GND for Channel-1 AD converter.
47	AV_{SS} 3	-	Analog GND for Channel-1 DA converter.
48	AOUT1(+)	O	Analog in-phase output for Channel-1 DA converter.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) . . . . . V_{SS} -0.5V to 7V
Input Voltage (V_1) . . . . . V_{SS} -0.5V to V_{DD} +0.5V
Output Voltage (V_0) . . . . . V_{SS} -0.5V to V_{DD} +0.5V

Thermal Information

Operating Temperature (T_{OPR}) . . . . . -20^oC to 75^oC
Storage Temperature (T_{STG}) . . . . . -55^oC to 150^oC

Recommended Operating Conditions

ITEM	MIN	TYP	MAX
Supply Voltage (Note 1) (V_{DD})	+4.75	+5.0	+5.25V
Ambient Temperature (T_A)	-20^oC	-	75^oC
Sampling Frequency (Note 2) (f_S)	30kHz	-	50kHz

ITEM	MIN	TYP	MAX
Input Pin (C_{IN})	-	-	9pF
Output Pin (C_{OUT})	-	-	11pF
Bi-Directional Pin ($C_{I/O}$)	-	-	11pF
Measurement Conditions	$V_{DD} = V_I = 0V$, f = 1MHz		

NOTES:

1. The analog power supplies for AD converters (Pins 17 and 44) must be turned on simultaneously with or before other power supplies. turning on these power supplies after any other power supply may cause the device to fall into latch-up condition. This precaution, however, does not apply when turning off the power supplies.
2. Although the device can operate with low f_S frequencies such as f_S = 8kHz or 16kHz, its analog characteristics deteriorate to extent. When used at only these low frequencies, the CXD2570Q is recommended that is pin-compatible with the CXD2555Q.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications ($AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = 5.0V \pm 10\%$, $AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = -20^oC$ to 75^oC)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	APPLICABLE PIN
Input Voltage	V_{IHC}		0.7 V_{DD}	-	-	V	(Note 4)
	V_{ILC}		-	-	0.3 V_{DD}		
	V_{IN}	Analog Input	V_{SS}	-	V_{DD}	V	(Note 5)
Output Voltage	V_{OH1}	I_{OH} = -2mA	V_{DD} -0.5	-	0.4	V	(Note 6)
	V_{OL1}	I_{OL} = 4mA	0	-	0.4		
	V_{OH2}	I_{OH} = -4mA	V_{DD} -0.5	-	V_{DD}	V	(Note 7)
	V_{OL2}	I_{OL} = 4mA	0	-	0.4		
	V_{OH3}	I_{OH} = 12mA	$V_{DD}/2$	-	V	V	(Note 8)
	V_{OL3}	I_{OL} = 16mA	0	-	$V_{DD}/2$		
	V_{OH4}	I_{OH} = -2mA	V_{DD} -0.8	-	V_{DD}	V	(Note 9)
	V_{OL4}	I_{OL} = 4mA	0	-	0.4		
Input Leakage Current	I_{L11}		-10	-	10	μA	(Note 10)
	I_{L12}		-40	-	40	μA	(Note 11)
	I_{L13}		-20	-50	-120	μA	(Note 12)
	I_{L14}		20	50	120	μA	(Note 13)
Output Leakage Current	I_{LZ}		-40	-	40	μA	(Note 14)
Feedback Resistance	R_{FB}	$V_{IN} = V_{SS}$ or V_{DD}	250k	1M	2.5M	Ω	(Note 15)
Supply Current	I_{DD}	(Note 3)	-	57	75	mA	

NOTES:

3. This includes current consumption at load resistance (R_L = 3.9kΩ).
4. When all input pins except AIN1 and AIN2, and bi-directional pins (BCK, LRCK) are input.
5. AIN1 and AIN2.
6. XCLK, XMCK2, and SOUT.
7. AOUT1 (+), AOUT 1 (-), AOUT2 (+), AOUT2 (-), and UCLK.
8. XTLO.
9. When bi-directional pins (BCK, LRCK) are output.
10. All input pins except AIN1 and AIN2.
11. When bi-directional pins (BCK, LRCK) are input.
12. MS, WO, and CLR.
13. TEST.
14. SOUT, AOUT1 (+), AOUT1 (-), AOUT2 (+), AOUT2 (-), and UCLK.
15. Resistance between XTLO and XTLI.

AC Electrical Specifications

$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = 5.0V \pm 10\%$,
$AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = -20^oC$ to 75^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
SIN Setup Time	tsus		10	-	ns
SIN Hold Time	ths		15	-	ns
LRCK Setup Time	tsul	Slave Mode	10	-	ns
LRCK Hold Time	thl	Slave Mode	15	-	ns
LRCK Delay Time	tdl	Master Mode C_L = 130pF	-40	30	ns
SOUT Delay Time	tds	C_L = 60pF	9	65	ns
SOUT Data Reset Time	tzd		7	42	ns
SOUT Data Erase Time	tdz		6	40	ns
XTLI Pulse Width	twl	f_S = 48kHz, 256f_S (XSL0 = XSL1 = XSL2 = L)	40	60	ns

Analog Specifications

$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = 5.0V \pm 10\%$,
$AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = -20^oC$ to 75^oC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall Characteristics of ADC + DAC Connection: The following conditions apply unless otherwise specified: Input waveform = 1kHz sine wave, 1.4V_{RMS} (= 0dB) XTAI = 33.8688MHz (= 768f_S, f_S = 44.1kHz) CLR = MS = WO = Open (= 5V) SOUT and SIN directly coupled					
S/N	A-Weighting Filter	80	86	-	dB
THD + N	20kHz LPF	-	0.010	0.018	%
Dynamic Range	1kHz, - 60dB, 20kHz LPF	80	85	-	dB
Channel Separation	20kHz, 0dB	-	96	-	dB
Gain Difference Between Channels		-	0.1	-	dB
Gain	R_L = 3.9kΩ	-3	0	+3	dB
Input Level	R_{IN} = 0Ω	-	0.286	-	V_{RMS}
	R_{IN} = 4.7kΩ	-	1.4	-	V_{RMS}
DC Offset (ADC Output)		-	069F	-	Hex
ADC Input Impedance		-	1.2	-	kΩ

Analog Specifications

$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = 5.0V \pm 10\%$,
$AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = -20^oC$ to 75^oC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Specifications in Single Unit: The following conditions apply unless otherwise specified: Input data = 1kHz sine wave,full scale (= 0dB), XTAI = 33.8688MHz (= 768f_S, f_S = 44.1kHz), CLR = MS = WO = Open (= 5V), MS = GND					
S/N	A-Weighting Filter	92	96	-	dB
THD + N	20kHz LPF	-	0.008	0.012	%
Dynamic Range	1kHz, - 60dB, 20kHz LPF	85	89	-	dB
Channel Separation	20kHz, 0dB	-	100	-	dB
Gain Difference Between Channels		-	0.05	-	dB
Output Level	R_L = 3.9kΩ	1.80	1.93	2.10	V_{RMS}

Test Circuits

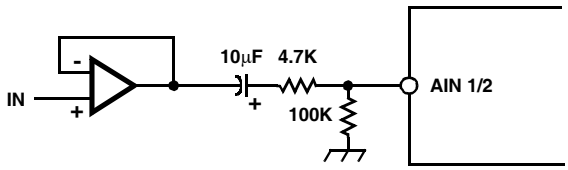


FIGURE 34. ADC INPUT SECTION

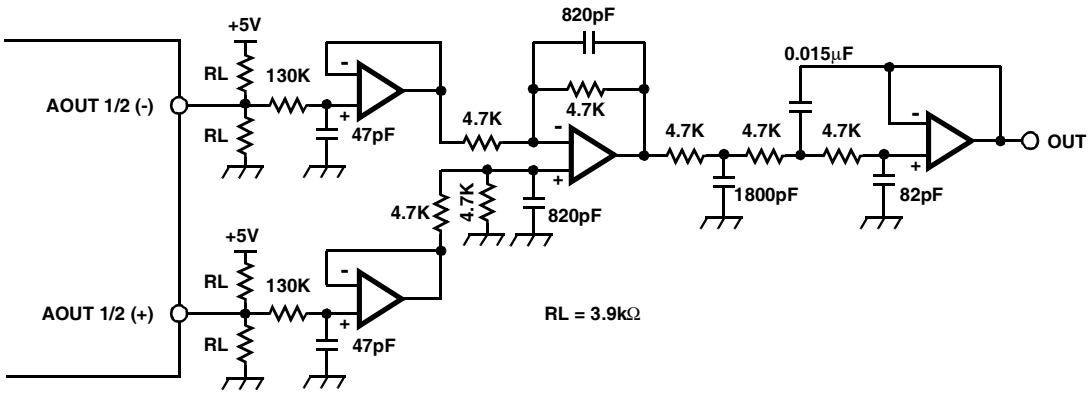


FIGURE 35. DAC OUTPUT SECTION

Timing Diagram

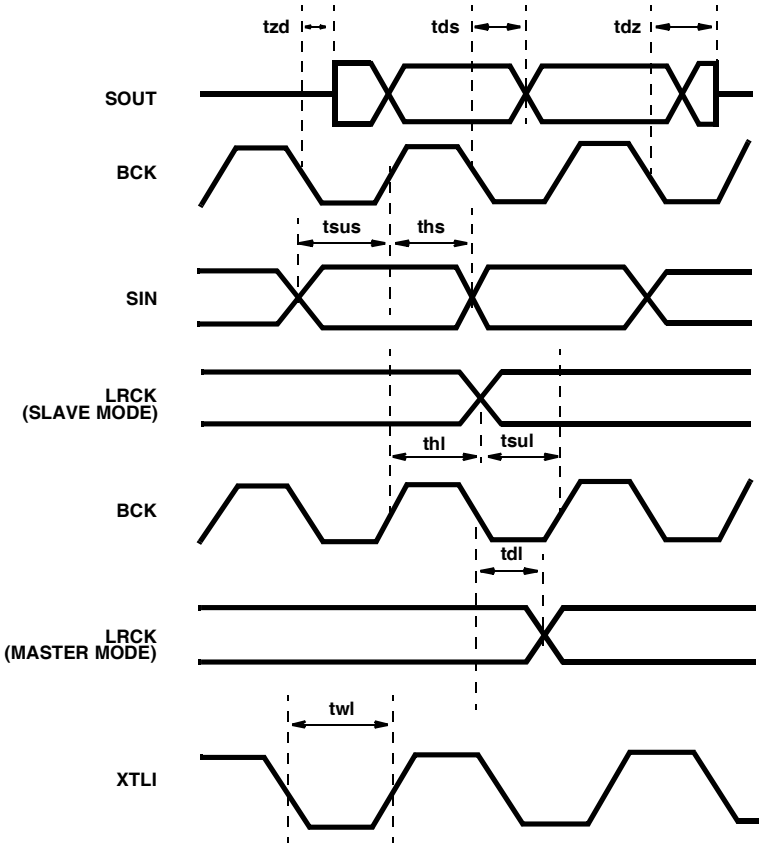


FIGURE 36.

Description of Functions

Serial Data Interface

(Related Pins) LRCK, BCK, SOUT, SIN, MASL, MLSL

The serial data format is common for both SIN (DA converter input) and SOUT (AD converter output), consisting of two channels per sampling serial data represented by 2's complement. Each channel is divided into 32-bit slots, of which 16 bits are handled as data.

MASL is used to select whether the 16 bits of valid data is placed in the first or the second half of the 32-bit slots.

TABLE 1.

MASL	
H	Forward Packing
L	Rearward Packing

Similarly, MLSL is used to select whether the serial data is arranged at LSB first or MSB first.

TABLE 2.

MLSL	
H	MSB first

TABLE 2.

MLSL	
L	LSB first

Master Mode/Slave Mode

(Related Pins) MS, LRCK, BCK

When using the XCS2555Q in multiple units or in a pair with DA converters such as the CXD2558M, one of these CXD2555Qs should be in the master mode to serve as the source of clocks LRCK and BCK. The other CXD2555Qs are used in the slave mode, with their clocks LRCK and BCK supplied by the master CXD2555Q.

TABLE 3.

MS	MODE	LRCK AND BCK I/O
H	Master Mode	Output
L	Slave Mode	Input

Crystal Oscillator Frequency Selection

(f_S = 32kHz to 48kHz)

(Related Pins) XTLI, XTLO, XSLO, XSL1, XSL2, UNCLK, XCLK

By setting a combination of XSLO and XSL1, with XSL2 fixed Low, the frequency of the external crystal oscillator connected to XTLI and XTLO can be selected. In this case, XCLK outputs a clock whose frequency is always 256 times f_S, and UCLK outputs a clock that is half the crystal oscillator frequency.

When supplying the master clock fro some other external source, not a crystal oscillator, use XTLI for this clock input and leave XTLO open.

TABLE 4.

XSL2	XSL1	XSL0	CRYSTAL OSCILLATOR FREQUENCY	XCLK	UCLK
L	L	L	$256f_S$	$256f_S$	$128f_S$
L	L	H	$512f_S$	$256f_S$	$256f_S$
L	H	L	$768f_S$	$256f_S$	$384f_S$
L	H	H	$1024f_S$	$256f_S$	$512f_S$

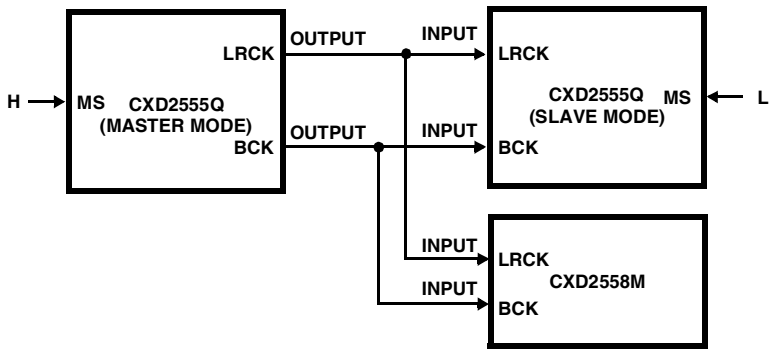


FIGURE 37. CONNECTION EXAMPLE

Crystal Oscillator Frequency Selection

(f_S = 8kHz to 24kHz)

(Related Pins) XTLI, XTLO, XSLO, XSL1, XSL2, UNCLK, XCLK

With XSL2 fixed High, the device can be operated with low-f_S frequencies which may be 1/2 or 1/4 the normal f_S frequency. In this case, the frequency of the crystal oscillator can be selected by setting a combination of XSL0 and XSL1 accordingly.

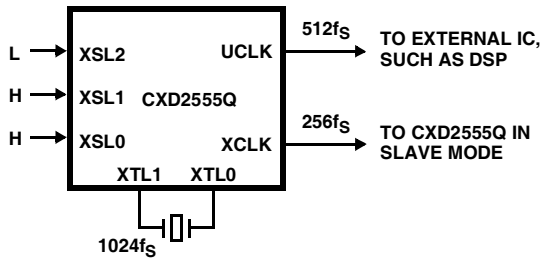


FIGURE 38. CONNECTION EXAMPLE

AD Converter Input Level

Given the constants shown in the Test Circuit on page 7, the AD converter input level V_{IN} (operational amplifier input IN) is such that $4V_{P-P}$ ($1.4V_{RMS}$) is equivalent to the full-scale output. Also, the large-amplitude inputs are possible by varying the AD converter input resistance value (R_{IN}). Use the equation shown below to calculate this resistance value. The AD converter generates full-scale outputs for inputs equal to or greater than the values thus obtained.

$R_{IN} = 420 \bullet V_{IN}$ [RMS] - 1200 [Ω]

Example: When input level = $1.4V_{RMS}$ ($4V_{P-P}$)

$R_{IN} = 4200 \bullet 1.4 - 1200 = 4680$
$\rightarrow 4700$ [Ω]

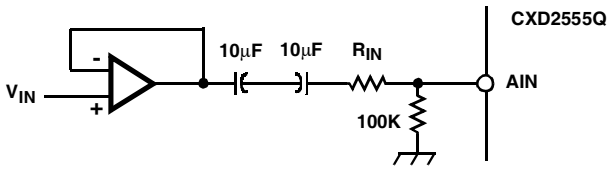


FIGURE 39.

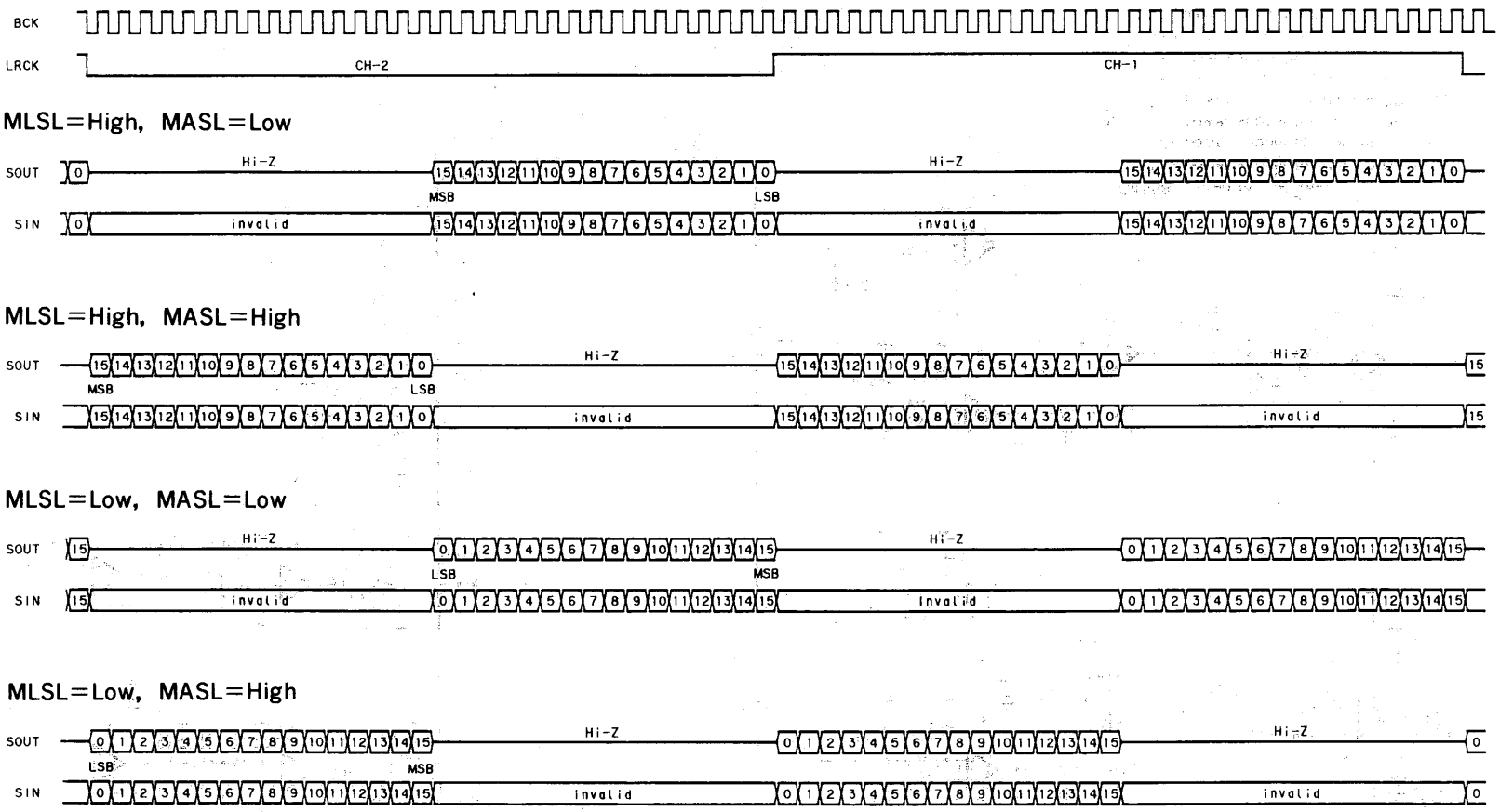
TABLE 5.

XSL2	XSL1	XSL0	CRYSTAL OSCILLATOR FREQUENCY (NOTE 16)	XCLK	UCLK	FREQUENCY DIVISION RATIO RELATIVE TO NORMAL f_S FREQUENCY	EXAMPLE OF 32kHz NORMAL FREQUENCY
H	L	L	$512f_S$	$512f_S$	$256f_S$	1/2	f_S = 16kHz
H	L	H	$1024f_S$	$1024f_S$	$512f_S$	1/4	f_S = 8kHz
H	H	L	$1024f_S$	$512f_S$	$512f_S$	1/2	f_S = 16kHz
H	H	H	$2048f_S$	$1024f_S$	$1024f_S$	1/4	f_S = 8kHz

NOTE:

16. When the normal frequency is assumed to be 32kHz, its derived frequency is 16kHz when divided by 2, or 8kHz when divided by 4. When divided in the same way, the low-f_S frequencies for 44.1kHz are 22.05kHz and 11.025kHz, and for 48kHz, they are 24kHz and 12kHz.

Serial Data Interface Timing



Application Circuit Master Mode (MS = High)