SONY

CXD2720Q

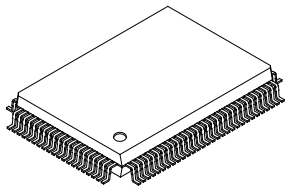
Single-Chip Digital Signal Processor for Karaoke

Description

The CXD2720Q is a digital signal processor LSI for Karaoke, suitable for use in LD/CD/CD-G/video CD and the like.

A large capacity DRAM and AD/DA converters are built in, and Karaoke functions such as key control, microphone echo and voice canceling are contained on a single chip.

100 pin QFP (Plastic)



Features

- 3-channel 1-bit AD converter and decimation filter
  S/N ratio: 88 dB
  THD + N: 0.016%
  Filter pass band ripple: less than ±0.5dB
  Filter stop band attenuation: less than –41dB
  (all characteristics are typical values)
- 2-channel 1-bit DA converter and oversampling filter
  S/N ratio: 98dB
  THD + N: 0.006%
  Filter pass band ripple: less than ±0.2dB
  Filter stop band attenuation: less than –41dB
  (all characteristics are typical values)
- In addition to analog input/output, 2-channel input/2-channel output of digital input/output are provided. The interface also supports a variety of formats.
- 128K-bit DRAM for key control and microphone echo processing

Functions

- Key controller pitch setting can be varied to a maximum of ±1 octave with a precision of 14 bits
- Microphone echo delay time can be varied to a maximum of 185ms (when Fs = 44.1kHz)
- Voice canceller supports settings other than center by the panpot volume
- Voice parametric equalizer
- Voice pitch shifter
- Mixing function to support sound multiplexing software
- Digital de-emphasis function

Structure

Silicon gate CMOS

Applications

Equipment having Karaoke function, such as LD/CD, compact music center, video games, etc.

Absolute Maximum Ratings

(Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 typ.)	V
• Operating temperature	Ta	–20 to +75	°C

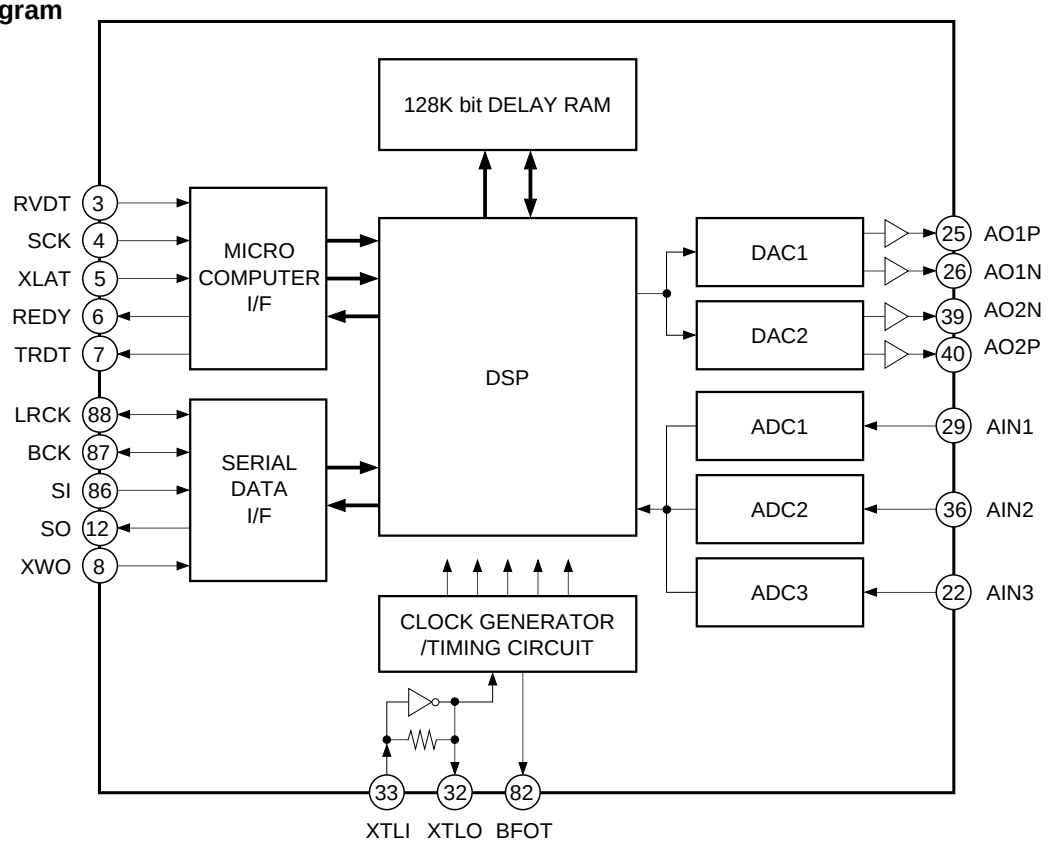
Input/Output Capacitance

• Input capacitance	C_{IN}	9 (max.)	pF
• Output capacitance	C_{OUT}	11 (max.)	pF
• Input/output capacitance	$C_{I/O}$	11(max.)	pF

* Measurement conditions: V_{DD} = V_I = 0V, F = 1MHz

E96426-ST

Block Diagram



Pin Configuration

Pin Description

Pin No.	Symbol	I/O	Description
1	AV_S0	—	DRAM digital GND.
2	$V_{SS}0$	—	Digital GND.
3	RVDT	I	Data input for microcomputer interface.
4	SCK	I	Shift clock input for microcomputer interface.
5	XLAT	I	Latch input for microcomputer interface.
6	REDY	O	Transmission enabling signal output for microcomputer interface. Transmission prohibited when Low.
7	TRDT	O	Serial data output for microcomputer interface.
8	XWO	I	Window open input for synchronization. Normally High.
9	XRST	I	System reset input. Resets when Low.
10	$V_{SS}1$	—	Digital GND.
11	$V_{DD}0$	—	Digital power supply.
12	SO	O	1-sampling 2-channel serial data output.
13	XS24	I	Serial data 24-/32-bit slot selection. 24-bit slot when Low. (valid for slave mode)
14	TST0	I	Test pin. Normally set Low.
15	TST1	I	Test pin. Normally set Low.
16	TST2	I	Test pin. Normally set Low.
17	TST3	I	Test pin. Normally set Low.
18	TST4	I	Test pin. Normally set Low.
19	TST5	I	Test pin. Normally set Low.
20	$V_{SS}2$	—	Digital GND.
21	AV_S3	—	CH3 AD converter GND.
22	AIN3	I	CH3 AD converter analog input (for microphone input).
23	AV_D3	—	CH3 AD converter power supply.
24	AV_D4	—	CH1 DA converter power supply.
25	AO1P	O	CH1 DA converter analog positive phase output.
26	AO1N	O	CH1 DA converter analog reversed phase output.
27	AV_S4	—	CH1 DA converter GND.
28	AV_S1	—	CH1 AD converter GND.
29	AIN1	I	CH1 AD converter analog input.
30	AV_D1	—	CH1 AD converter power supply.
31	XV_{DD}	—	Digital power supply for master clock.
32	XTLO	O	Crystal oscillator circuit output.
33	XTLI	I	Crystal oscillator circuit input.
34	XV_{SS}	—	Digital GND for master clock.
35	AV_S2	—	CH2 AD converter GND.

Pin No.	Symbol	I/O	Description
36	AIN2	I	CH2 AD converter analog input.
37	AV_D2	—	CH2 AD converter power supply.
38	AV_D5	—	CH2 DA converter power supply.
39	AO2N	O	CH2 DA converter analog reversed phase output.
40	AO2P	O	CH2 DA converter analog positive phase output.
41	AV_S5	—	CH2 DA converter GND.
42	$V_{SS}3$	—	Digital GND.
43	$V_{DD}1$	—	Digital power supply.
44 to 52	NC		Normally open.
53	$V_{SS}4$	—	Digital GND.
54 to 68	NC		Normally open.
69	$V_{SS}5$	—	Digital GND.
70	$V_{DD}2$	—	Digital power supply.
71 to 79	NC		Normally open.
80	$V_{SS}6$	—	Digital GND.
81	X768	I	Test input pin. Normally set Low.
82	BFOT	O	Clock, frequency-divider output (384fs).
83	INVI	I	Test pin. Normally set Low.
84	NC		Normally open.
85	NC		Normally open.
86	SI	I	1-sampling 2-channel serial data input.
87	BCK	I/O	Serial bit transmission clock for serial input/output data SI and SO.
88	LRCK	I/O	Sampling frequency clock for serial input/output data SI and SO.
89	XMST	I	BCK, LRCK master/slave mode switching input. Master mode when Low.
90	$V_{SS}7$	—	Digital GND.
91 to 98	NC		Normally open.
99	$V_{DD}3$	—	Digital power supply.
100	AV_D0	—	Digital power supply for DRAM.

DC Characteristics

(AV_D0 to 5 = XV_{DD} = $V_{DD}0$ to 3 = 5V ± 10%, AV_S0 to 5 = XV_{SS} = $V_{SS}0$ to 7 = 0V, Ta = –20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH}		0.7V_{DD}			V	*1, *4, *5
	Low level	V_{IL}				0.3V_{DD}	V	*1, *4, *5
Input voltage (2)	High level	V_{IH}		0.8V_{DD}			V	*3
	Low level	V_{IL}				0.2V_{DD}	V	*3
Input voltage (3)		V_{IN}	Analog input	V_{SS}		V_{DD}	V	*2
Output voltage (1)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*6, *7, *8
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*6, *7, *8, *9
Output voltage (2)	High level	V_{OH}	I_{OH} = –6.0mA	V_{DD} – 0.8			V	*10
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*10
Output voltage (3)	High level	V_{OH}	I_{OH} = –12.0mA	V_{DD}/2			V	*11
	Low level	V_{OL}	I_{OL} = 12.0mA			V_{DD}/2	V	*11
Input leak current (1)		I_I	V_{IH} = V_{DD}, V_{SS}	–10		10	µA	*1, *3, *5
Input leak current (2)		I_I	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*4
Output leak current		I_{OZ}	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*8, *9
Feedback resistance		R_{FB}		250k	1M	2.5M	Ω	Resistance between *5 and *11.
Current consumption		I_{DD}	fs = 44.1kHz		79	90	mA	

*1 RVDT, SCK, XLAT, XWO, XRST, XS24, TST0 to TST5, X768, SI, XMST

*2 AIN1, AIN2, AIN3

*3 INVI

*4 During input to bidirectional pins BCK, LRCK

*5 XTLI

*6 During output from bidirectional pins BCK, LRCK

*7 SO, BFOT

*8 TRDT

*9 REDY

*10 AO1P, AO1N, AO2N, AO2P

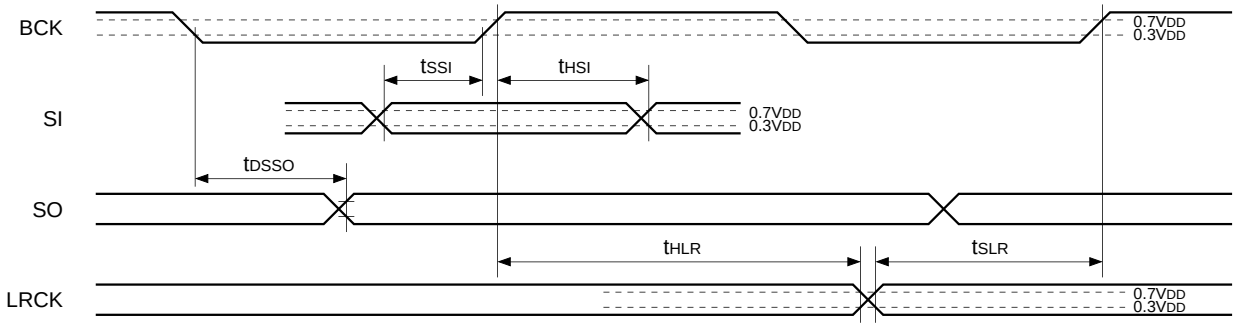
*11 XTLO

AC Characteristics

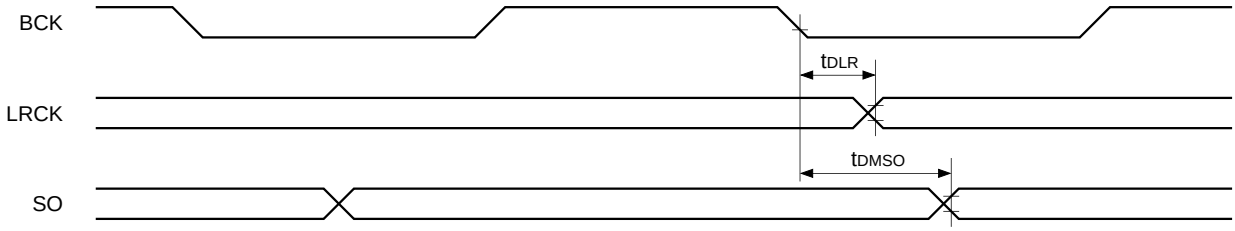
(AV_D0 to 5 = XV_{DD} = $V_{DD}0$ to 3 = 5V±10%, AV_S0 to 5 = XV_{SS} = $V_{SS}0$ to 7 = 0V, Ta = –20 to +75°C)

Serial Audio Interface Timing

[Slave mode]



[Master mode]

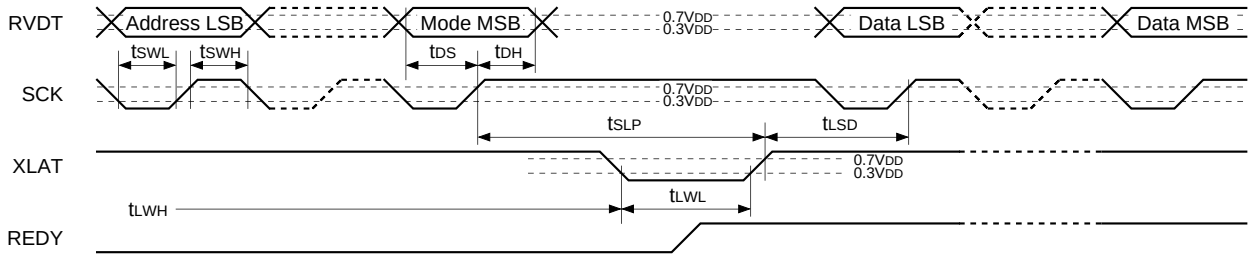


Item	Symbol	Conditions	Min.	Max.	Unit
SI setup time	t_{SSI}	Slave mode	20		ns
SI hold time	t_{HSI}	Slave mode	40		ns
SO delay time	t_{DSSO}	Slave mode, CL = 60pF		50	ns
LRCK setup time	t_{SLR}	Slave mode	20		ns
LRCK hold time	t_{HLR}	Slave mode	40		ns
LRCK delay time	t_{DLR}	Master mode, CL = 120pF		50	ns
SO delay time	t_{DMSO}	Master mode, CL = 60pF		100	ns

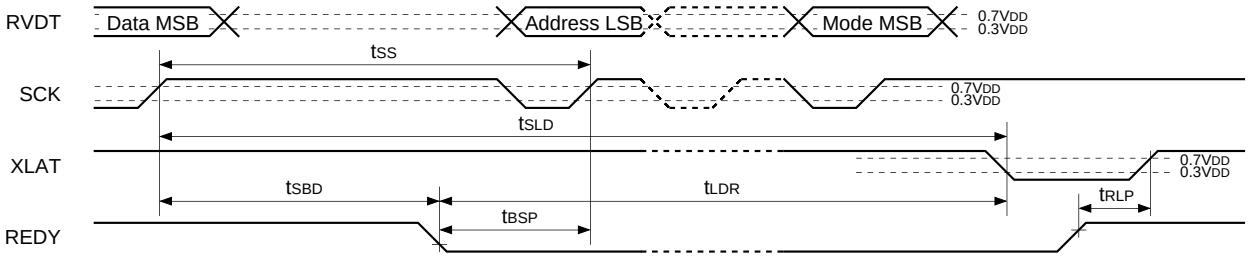
Microcomputer Interface Timing

[Write]

• Transmission timing for address section, transmission mode section, data section LSB

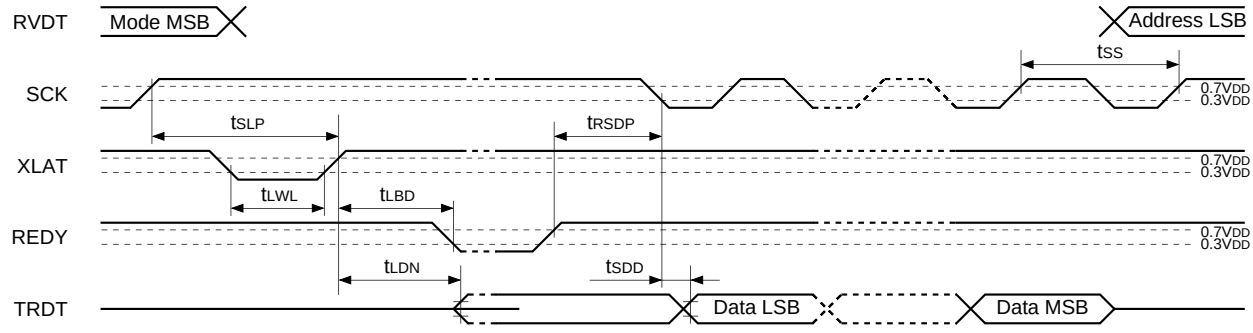


• Transmission timing from data section MSB to address section and transmission mode section



[Read]

• Transmission timing for address section and transmission mode section is the same as for write.



Item	Symbol	Min.	Max.	Unit
RVDT setup time relative to SCK rise	t_{DS}	20		ns
RVDT data hold time from SCK rise	t_{DH}	1t + 20		ns
SCK Low level width	t_{SWL}	1t + 20		ns
SCK High level width	t_{SWH}	1t + 20		ns
XLAT Low level width	t_{LWL}	1t + 20		ns
XLAT High level width	t_{LWH}	1t + 20		ns
SCK rise preceding time relative to XLAT rise	t_{SLP}	20		ns
SCK rise wait time relative to XLAT rise	t_{LSD}	3t + 20		ns
Delay time to REDY fall relative to XLAT rise.	t_{LBD}		3t + 50	ns
Delay time to REDY fall relative to SCK rise	t_{SBD}		4t + 50	ns
REDY fall preceding time relative to SCK rise	t_{BSP}	20		ns
REDY rise preceding time relative to XLAT rise	t_{RLP}	20		ns
REDY rise preceding time relative to SCK fall	t_{RSDP}	20		ns
XLAT fall wait time relative to SCK rise	t_{SLD}	3t + 20		ns
XLAT fall delay time relative to REDY fall	t_{LDR}	20		ns
Delay time from XLAT rise until TRDT data becomes active	t_{LDN}		3t + 80	ns
Delay time from SCK rise until TRDT data becomes high-impedance	t_{SDF}		3t + 80	ns
Delay time from SCK fall until TRDT data is verified	t_{SDD}		2t + 70	ns
CK rise wait time for next transmission	t_{SS}	2t + 40		ns

Note 1) t is the cycle of 1/2 the clock frequency applied to the XTLI pin. (384fs)

Note 2) REDY and TRDT pins are the values for CL = 60pF.

Analog Characteristics (AV_D0 to 5 = $V_{DD}0$ to 3 = XV_{DD} = 5.0V, AV_S0 to 5 = $V_{SS}0$ to 7 = XV_{SS} = 0.0V, Ta = 25°C, DSP: each function = OFF, gain = 1)

[1] ADC + DAC connection total characteristics

The measurement circuit in Figure 1-1 is used. Unless otherwise indicated, the measurement conditions are as given below.

- Input signal ...1.0Vrms, 1kHz
- fs.....44.1kHz
- Rin 0Ω

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	1.0Vrms, EIAJ (with "A" weighting filter)	80	88		dB
THD + N	1.0Vrms, EIAJ		0.016	0.03	%
	0.5Vrms, EIAJ		0.012		
Dynamic range	EIAJ		92		dB
Channel separation	Only ADC characteristics using DAC1, EIAJ		108		dB
Level difference between channels	Only ADC characteristics using DAC1		0.05		dB
Analog full-scale input level	Rin = 0Ω		1.26		Vrms
	Rin = 22kΩ		2.06		
ADC input impedance			34.6		kΩ
Analog current consumption			21		mA

*1 Analog input level which outputs digital full scale.
An optional analog input signal level Vin (Vrms) of 1.26Vrms or more can be set in digital full scale by the measurement circuit external resistor Rin.
The calculation formula for external resistor Rin is:

$$Rin = 27.5 \times Vin - 34.6\ [k\Omega] \quad \ldots\ldots(1)$$

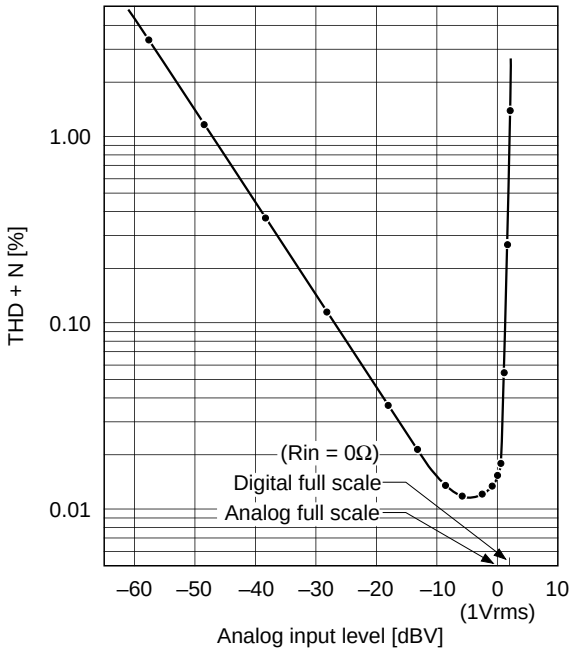
However, THD + N characteristics deteriorate for full-scale output as shown in Graph 1, so use of up to 80% (when Rin = 0Ω, 0.8 × 1.26 (Vrms) = 1.0 (Vrms) → "analog full scale") of the analog signal level is recommended for digital full-scale output.
In this case, the Rin calculation formula is the same as formula (1), except that Vin becomes 1.25 × Vin. Note that this change causes the output level after ADC + DAC to change.
Most of the above specifications are measurement values for analog full scale.

[2] DAC unit characteristics

Use the measurement circuit in Figure 1-2. Unless otherwise specified, the measurement conditions are as follows.

- Input signal ....0dB, 1kHz, 16 bit
- fs.....44.1kHz

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)		98		dB
THD + N	EIAJ (0dB)		0.006		%
	EIAJ (–1dB)		0.004		
Dynamic range	EIAJ (–60dB)		98		dB
Channel separation	EIAJ		120		dB
Level difference between channels	EIAJ		0.05		dB
Output level	EIAJ (Measure at OUT in Figure 1-2.)		2.0		Vrms



Graph 1.

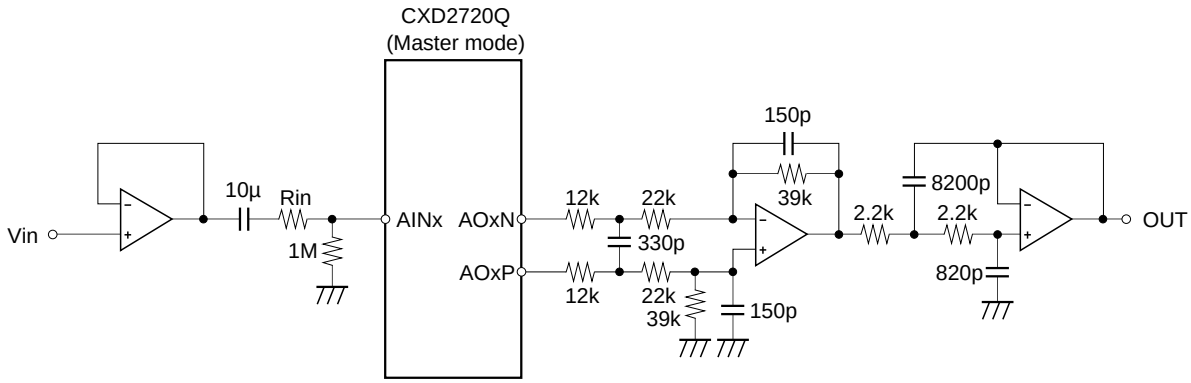


Figure 1-1. ADC + DAC Measurement Circuit Diagram

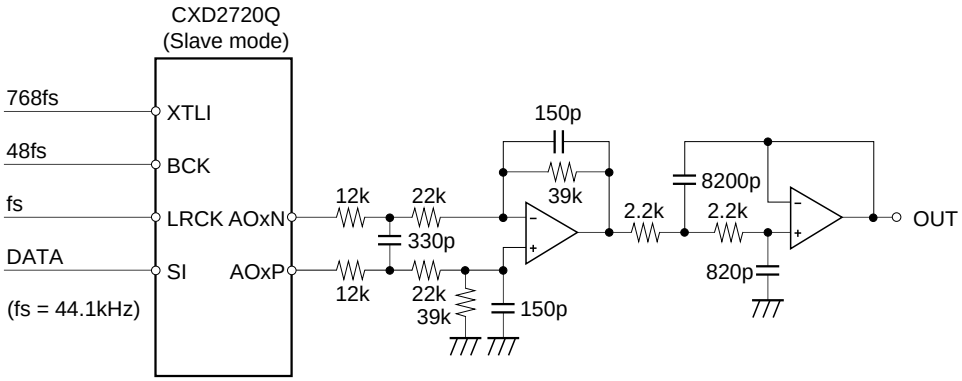


Figure 1-2. DAC Measurement Circuit Diagram

Description of Functions

1. Master/Slave Modes

[Relevant pins] XMST, LRCK, BCK

When connecting multiple CXD2720Qs, or when using as a pair with a D/A converter such as the CXD2558M, one of the CXD2720Q should be in master mode to supply LRCK and BCK.

The clock applied to LRCK and BCK in slave mode must be synchronized to either the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin

XMST	Mode	LRCK, BCK I/O
H	Slave mode	Input
L	Master mode	Output

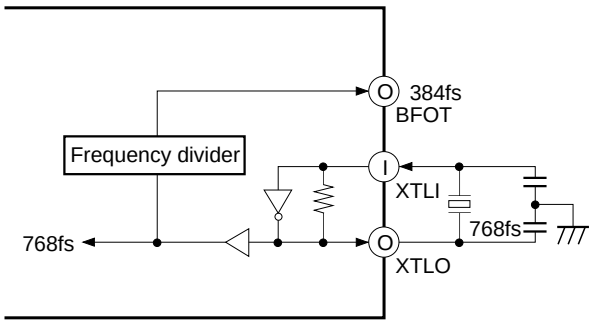
Table 1-1. LRCK, BCK Mode Setting

2. Master Clock System

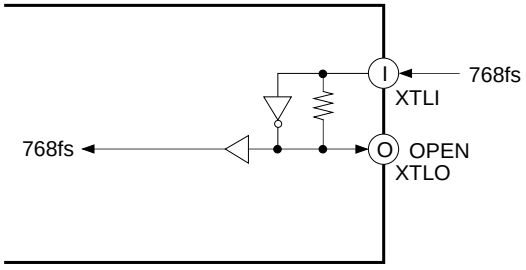
[Relevant pins] XTLI, XTLO, BFOT

768fs (fs = 44.1kHz) is assumed for the master clock system, and the connection is as shown below. (Please inquire with regard to use at other than fs = 44.1kHz.)

(1) Master



(2) Slave



3. Input/Output Synchronization Circuit

[Relevant pins] LRCK, XWO

During normal operation, synchronization is performed automatically to input LRCK (in slave mode), and phase is matched with serial input data, but if there is a lot of jitter on LRCK, or during power input, synchronization may be impossible. In this case, forced synchronization can be done by making the XWO pin Low for 2/Fs or more. Forced synchronization operation is done by the timing of the second LRCK rising edge after the XWO pin is made Low. When synchronization is completed, return the XWO pin to High.

4. Reset Circuit

[Relevant pins] XRST, XTLI, XTLO

This LSI must be reset after power is turned ON.

Reset is done by making the XRST pin Low for 1/Fs or more after supply voltage satisfies the recommended operating condition, and the crystal oscillator clock of the XTLI, XTLO pins or the external clock input from the XTLI pin is correctly applied.

5. Serial Audio Interface (SIF)

[Relevant pins] SI, SO, BCK, LRCK, XS24, XMST

Serial data is used for the external communication of the digital audio data.

The CXD2720Q has one system each for input and output, and each one inputs/outputs 2 channels of data at 1 sampling cycles. Either the 32-bit clock mode or 24-bit clock mode can be selected. In master mode, the 32 bit clock mode is fixed.

(1) Pin Configuration

The pins shown in the table below are assigned to SIF.

Pin name	I/O	Function
SI	I	Serial input; taken synchronized to BCK.
SO	O	Serial output; output synchronized to BCK.
BCK	I/O	BCK input/output; either 32-bit clock mode (64fs) or 24-bit clock mode (48fs). BCK output supports 32-bit clock mode only.
LRCK	I/O	LRCK input/output (1fs).
XS24	I	SI0 slot number (24/32) selection input. Low: 24-bit slot; High: 32-bit slot. Valid only in slave mode. Set High in master mode.
XMST	I	BCK, LRCK master mode/slave mode switching input. Low: master mode; High: slave mode.

Table 5-1. Pin Configuration

(2) Operation Modes

The LRCK/BCK mode and SI/SO system settings can be selected by the setup register settings as follows.

LRCK/BCK Mode Setting

Setup register	Function	Contents
SQ11	LRCK format	"0" : normal, "1" : IIS
SQ10	LRCK polarity selection	"0" : Lch "H", "1" : Lch "L"
SQ09	BCK polarity selection relative to LRCK edge	"0" : edge↓, "1" : edge↑

Table 5-2. LRCK/BCK Mode Setting

SI/O System Register Setting

SI system

Setup register	Function	Contents
SQ08	SI data list	"0" : MSB first, "1" : LSB first
SQ07	SI frontward/rearward truncation	"0" : Forward truncation, "1" : Rearward truncation
SQ06 SQ05	SI data word length SI data word length	SQ06 SQ05 0 0 : 16 bit 1 1 : 24 bit

Table 5-3. SI System Register Setting

SO system

Setup register	Function	Contents
SQ04	SO data list	"0" : MSB first, "1" : LSB first
SQ03	SO forward/rearward truncation	"0" : Forward truncation, "1" : Rearward truncation
SQ02 SQ01	SO data word length	SQ02 SQ01 0 0 : 16 bit 0 1 : 18 bit 1 0 : 20 bit 1 1 : 24 bit

Table 5-4. SO System Register Setting

(3) SIF Format

Serial I/F have one input/output system each, and except for slot number, the following formats can be set for input and output, independently, by setting the setup register. It can also be made to support IIS format, to enable connection to Philips and other devices. The timing charts for each data format are given on the following pages.

32-bit slot (XS24 = High)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08	Supplement
MSB first	24 bit	Forward truncation	1	1	0	0	Supports 20, 16 bits
MSB first	16 bit	Forward truncation	0	0	1	0	
LSB first	24 bit	Rearward truncation	1	1	1	1	Supports 20, 16 bits

Table 5-5. 32-bit Slot Serial IN

SI format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bit	Rearward truncation	0	0	1	0
MSB first	18 bit	Rearward truncation	1	0	1	0
MSB first	20 bit	Rearward truncation	0	1	1	0
MSB first	24 bit	Rearward truncation	1	1	1	0
MSB first	24 bit	Forward truncation	1	1	0	0
LSB first	24 bit	Rearward truncation	1	1	1	1

Table 5-6. 32-bit Slot Serial OUT

24-bit slot (XS24 = Low)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08	Supplement
MSB first	16 bit	Rearward truncation	0	0	1	0	
MSB first	24 bit		1	1	*	0	Supports 20, 16 bits for forward truncation
LSB first	24 bit		1	1	*	1	Supports 20, 16 bits for rearward truncation

Table 5-7. 24-bit Slot Serial IN

SI format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bit	Rearward truncation	0	0	1	0
MSB first	18 bit	Rearward truncation	1	0	1	0
MSB first	20 bit	Rearward truncation	0	1	1	0
MSB first	24 bit		1	1	*	0
LSB first	24 bit		1	1	*	1

Table 5-8. 24-bit Slot Serial OUT

Note 1) When performing 20-bit and 16-bit data input in serial IN 24-bit data format, fill the lower 4 and 8 bits with “0”, respectively.

Note 2) * means “don't care”.

Digital Audio Data Input Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

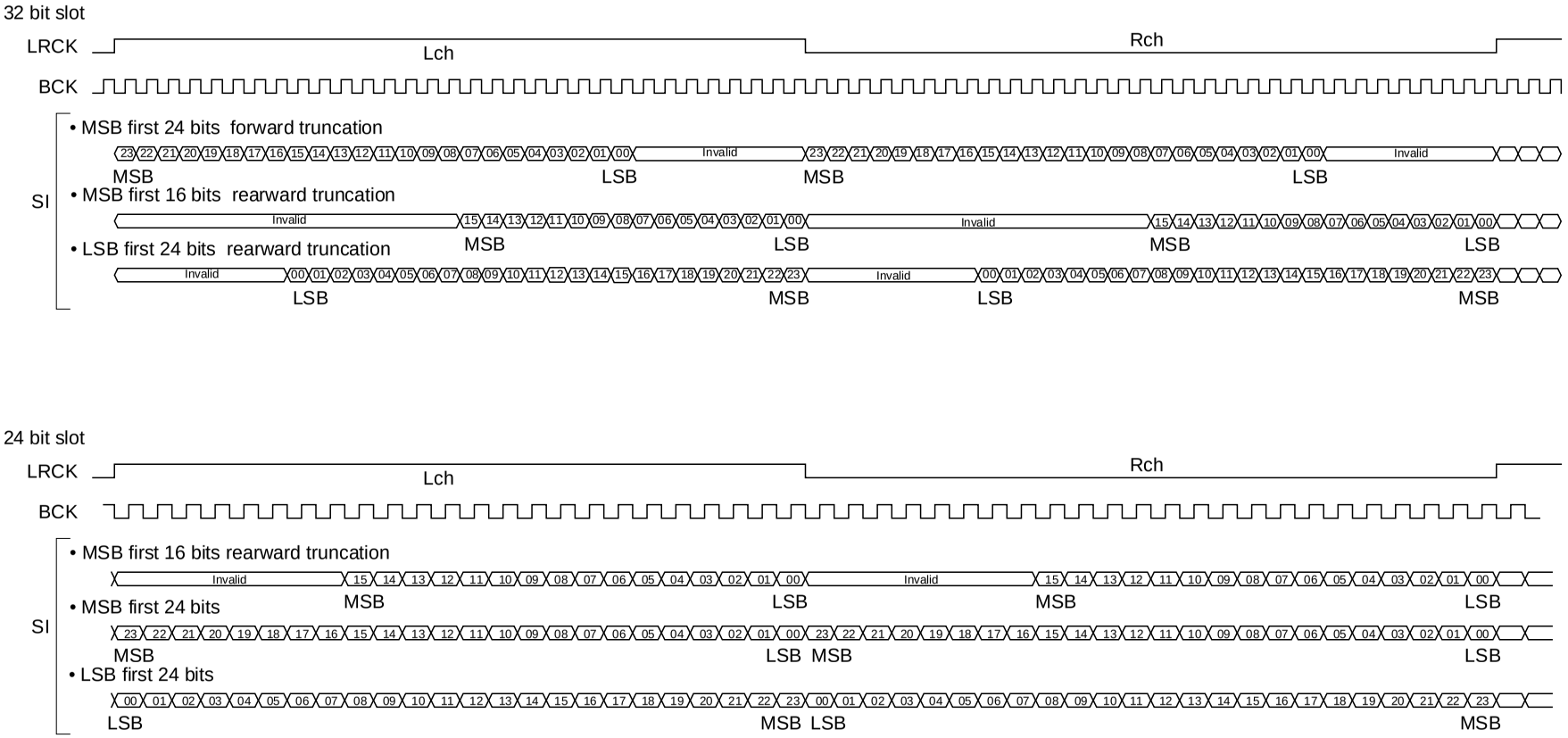


Figure 5-1.

Digital Audio Data Output Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

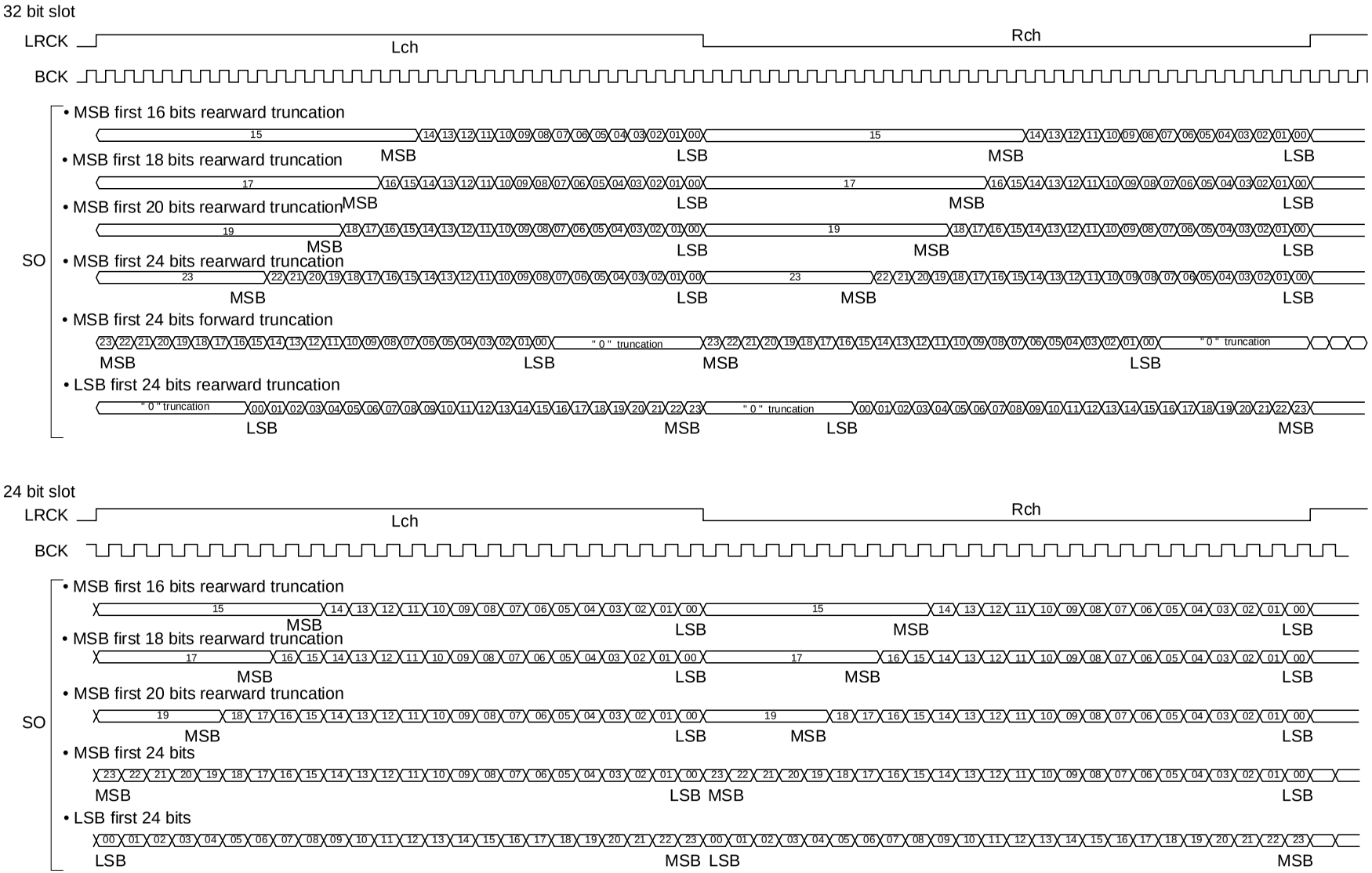


Figure 5-2.

6. Microcomputer Interface

[Relevant pins] RVDT, TRDT, SCK, XLAT, REDY

The CXD2720Q performs serial audio interface format setting, volume, coefficient settings of microphone echo delay amount and others by serial data from the microcomputer.

Further, bidirectional communication such as internal data read from the CXD2720Q to the microcomputer can be done at the rate of once in 1 LRCK.

(1) Pin Structure

The five external pins indicated in the table below are allocated for microcomputer interface.

Microcomputer interface begins operation when XLAT is received, so RVDT, TRDT, SCK and REDY are connected in common, and by controlling (wiring) only XLAT separately, multiple CXD2720Qs can be used.

Pin name	I/O	Function
RVDT	I	Serial data input from microcomputer.
TRDT	O	Serial data output to microcomputer. High impedance state unless this pin is set to internal data read state by the microcomputer. Therefore, it is preferable to perform pull-up or pull-down so that potential is not unstable when this pin is not active.
SCK	I	Shift clock for serial data. Input data from RVDT is taken according to SCK rise, and output data from TRDT is sent out according to SCK fall.
XLAT	I	Interprets the 8 bits of RVDT before this signal rises as transmission mode data, and the bits before that as address data.
REDY	O	Transmission prohibited while at Low level. Transmission enabled at High. This pin is an open drain, and must be pulled up externally.

Table 6-1. Microcomputer Interface External Pins

(2) Description of Communication Formats

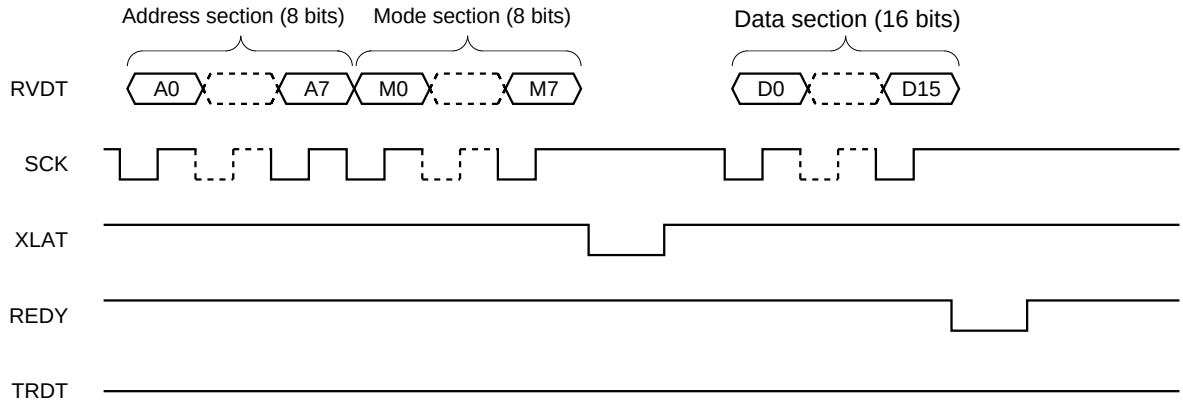
The data transmission timing between the microcomputer interface and coefficient RAM and setup register is called the SV cycle, and is generated once in 1LRCK.
The SV cycle is generated immediately preceding the signal processing program, so it has absolutely no effect on signal processing, and there is no risk of the sound being cut.

In read/write modes,

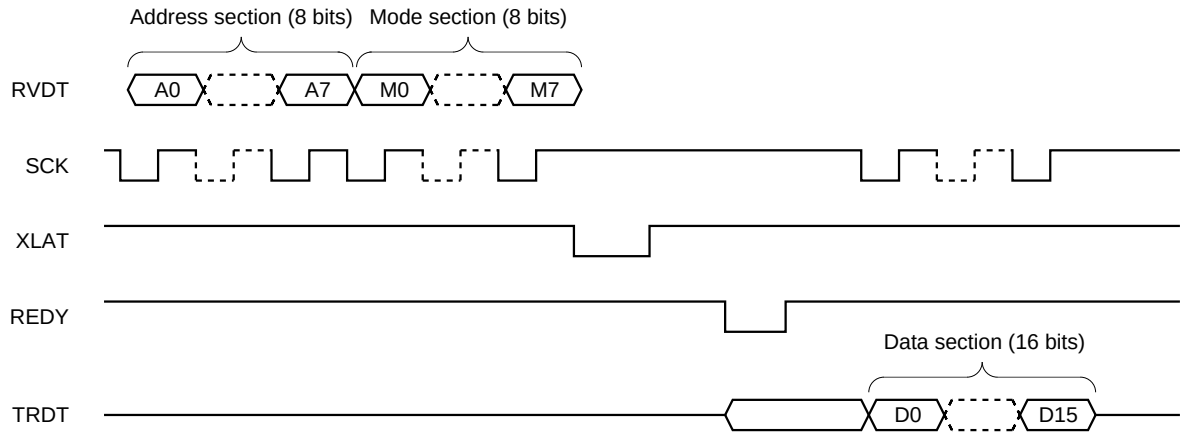
Address section + Mode section + Data section

act as one package of data to perform data transmission between the microcomputer and the CXD2720Q.

[Write] • For coefficient RAM



[Read] • For coefficient RAM



Note) For both read and write, the data section is 24 bits for the setup register.

Figure 6-1. Examples of Communication

(3) Data Structure

Data structure is classified in three types, as shown in the table below. All data communication is done with LSB first.

Name	Bit length	Contents	Remarks
A0 to A7	8	Address section	
M0 to M7	8	Transmission mode section	
D0 to D15/SQ00 to SQ23	16/24	Data section	Coefficient RAM is 16 bits; setup register is 24 bits

Table 6-2. Data Structure

(3)-1. Transmission Mode Section

The transmission mode section is 8 bits and has the following functions.

Bit	Name	Function	
M7	XVMT	SO Mute	0: ON (No sound) 1: OFF
M6		Reserve	
M5			
M4	VS1	Data type	VS1 VS0 0 0 Setup register 1 0 Coefficient RAM (K-RAM)
M3	VS0		
M2		Reserve	
M1			
M0	VRD	Send/Receive	0: Receive 1: Send **Note)** Polarity as seen from the CXD2720Q

Table 6-3. Transmission Mode Section

(3)-2. Address Section

The coefficient RAM has a 192-word structure, so the address section is 8 bits. The setup register has a 1-word structure, so the address section data may be optional.

(3)-3. Data Section

Sixteen SCK are required, as the coefficient RAM has a 16-bit structure (D0 to D15). The setup register has a 24-bit structure (SQ00 to SQ23), so twenty-four SCK are required.

(4) Details of Communication Methods

The definitions of signal timing required for control from the microcomputer are given below.

(4)-1. Write

First, address section data and mode section data are sent from the microcomputer, synchronized to SCK, to the RVDT pin.
The address section data is 8 bits both for the coefficient RAM and setup register, and the setup register transmits optional data for 1 word length. Address section data is sent with LSB first.
Mode section data is fixed at 8 bits regardless of content.

The phase relationship between SCK and RV data (data applied to the RVDT pin) has the following restrictions:

- RV data must be verified before SCK rise ($t_{DS} \geq 20$ns).
- RV data must be held for 1t + 20ns or more after SCK rise (t_{DH}).

SCK itself has the following restrictions:

- SCK Low level must be 1t+ 20ns or more (t_{SWL}).
- SCK High level must also be 1t + 20ns or more (t_{SWH}).

After raising SCK which corresponds to mode section final data, XLAT is raised ($t_{SLP} \geq 20$ns). XLAT Low level width must be maintained at 1t + 20ns or more (t_{LWL}). Further, fall timing restrictions are:

- for the preceding transmission, if REDY falls due to SCK, as for write, 3t + 20ns or more is required. (t_{SLD})
- for the preceding transmission, if REDY falls due to XLAT, as for read, 20ns or more is required. (t_{LDR})

Further, if preceding transmissions have been performed and REDY = Low, it is necessary to wait for REDY = High to raise XLAT.

The procedure until this point is the same for write and read.

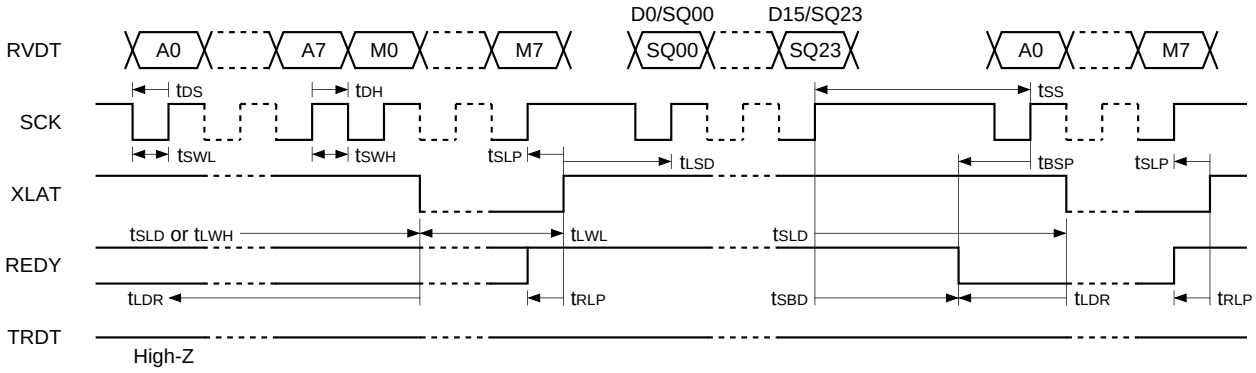


Figure 6-2. Write Timing

Data section write begins after XLAT rise, and here also transmission must be with LSB first, with t_{DS} and t_{DH} restrictions. In addition, after raising XLAT at the starting point for sending to the data section, wait for 3t + 20ns or more for the first SCK rise. (t_{LSD})

When 16 bits (coefficient RAM) or 24 bits (setup register) of this write is repeated, REDY = Low within 4t + 50ns, and the microcomputer is informed of waiting status for the SV cycle, which is the dedicated data rewrite cycle by microcomputer interface. (t_{SBD})
When REDY goes High again, the corresponding data is written.

The next communication restarts by using the REDY signal as follows.

- When REDY = Low, the SCK for the next transmission can rise ($t_{BSP} \geq$ 20ns).
- In the same way, when REDY = Low, the XLAT for the next transmission can fall ($t_{LDR} \geq$ 20ns).

REDY will fall due to this transmission, but it is prohibited for XLAT to rise for the next transmission before the REDY rises. Be sure to raise the next XLAT after REDY falls ($t_{RLP} \geq$ 20ns).

In order to restart the next transmission without using the REDY signal, the following conditions must be observed:

- There should be 2t + 40ns or more left between the SCK rise for the final data section and the SCK rise for the next transmission (t_{SS}).
- In the same way, the XLAT for the next transmission can fall after waiting 3t + 20ns or more after the final data section SCK rise (t_{SLD}).

The tss and t_{SLD} here are shorter times than $t_{SBD} \leq$ 4t + 50ns, so the restriction conditions are not much strict. However, even in this case the rise of XLAT for the next transmission must come after REDY rise ($t_{RLP} \geq$ 20ns).

Further, the restriction for XLAT fall at the starting point of this write from t_{SLD} can be:

- $t_{SLD} \geq$ 3t + 20ns if the preceding transmission was “write”.

(4)-2. Read

First, address section and mode section data are transmitted synchronized to SCK, and XLAT is raised matched with this; the procedure until this point is the same as for write, so the description is omitted here.

Read differs from write in that after XLAT rise, REDY falls within 3t + 50ns (t_{LBD}), and the microcomputer is informed of SV cycle waiting.
At this time, the TRDT pin changes from high-impedance state to active state ($t_{LDN} \leq 3t + 80ns$) simultaneously with REDY fall. When the read data is ready, the REDY pin changes from Low to High. When the data read out from the TRDT pin is made TR, and SCK falls ($t_{RSDP} \geq 20ns$) when the REDY pin goes High, the first TR data is defined within 2t + 70ns (t_{SDD}). The microcomputer reads this data at SCK rise. The TR data is read in order from the LSB with 16 bits for the coefficient RAM and 24 bits for the setup register by adding SCK, the corresponding data is all read, and then read is completed.

Next, the method for restarting transmission after read is completed is described.
As in Case 1, there is a method for sending address section and mode section data consecutively after reading all of the 16- or 24-bit data. There should be 2t + 40ns or more left between the SCK rise for the final data read and the next SCK rise (tss), and this is established by the conditions $t_{SWL} \geq 1t + 20ns$ and $t_{SWH} \geq 1t + 20ns$. Further, at this read REDY changes from High to Low, but it is prohibited for the XLAT for the next transmission to fall before this. If REDY = Low has been verified, XLAT can fall ($t_{LDR} \geq 20$ ns).
Also, while 16- or 24-bit data is being read from the TRDT pin, address and mode section data writing to the RVDT pin for the next transmission can be started.
In Case 3, the final section of read data and the final data in the mode section overlap, and this allows shifting to the next transmission processing in the shortest possible time after data read.
It is also possible to have data read and address and mode section write overlap partially, as shown by Case 2.

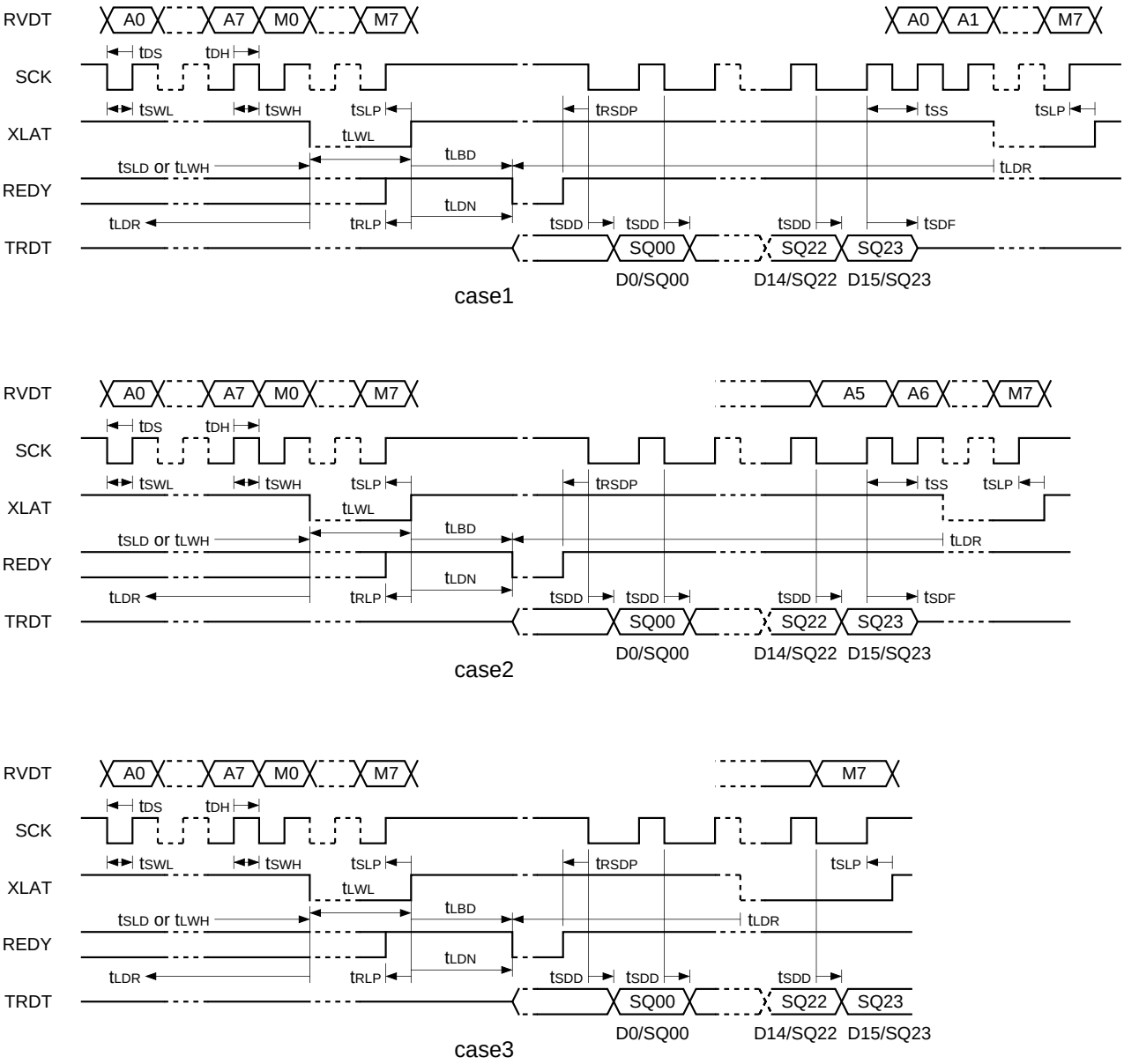


Figure 6-3. Read Timing

7. Setup Register

When the setup register is selected for microcomputer interface transmission mode, the following settings are possible for serial audio interface and DAC.

Data section bit	Control		When system reset is Low
SQ23 to 12	Reserve bit	Must be Low for setup register setting change	All Low
SQ11	LRCK format	0: normal 1: IIS	Normal
SQ10	LRCK polarity selection	0: Lch High 1: Lch Low	Lch High
SQ09	BCK polarity selection relative to LRCK edge	0: Falling edge 1: Rising edge	Falling edge
SQ08	SI data list	0: MSB first 1: LSB first (24-bit rearward truncation)	MSB first
SQ07	SI frontward/rearward truncation	0: Frontward truncation (valid only for MSB first/24 bits/32 slots) 1: Rearward truncation	Frontward truncation
SQ06, 05	SI data word length	SQ06 SQ05 0 0 : 16 bits 1 1 : 24 bits	16 bits
SQ04	SO data list	0: MSB first 1: LSB first	LSB first
SQ03	SO frontward/rearward truncation	0: Frontward truncation 1: Rearward truncation	Frontward truncation
SQ02, 01	SO data word length	SQ02 SQ01 0 0 : 16 bits 0 1 : 18 bits 1 0 : 20 bits 1 1 : 24 bits	16 bits
SQ00	DAC forced mute	0: ON 1: OFF	ON

Table 7-1.

8. Coefficient RAM Setting

When the coefficient RAM is selected in microcomputer interface transmission mode, the coefficient parameters such as each section's volumes and microphone echo delay amount can be set. Data settings other than those given following in Tables 8-1 and 8-2 are “don't care”.

(1) Fixed Values for System Initialization

When the system is initialized, the coefficient RAM must be set at the fixed values, shown below, due to internal operation.

Address	Fixed value
01H	68A9H
02H	5121H
03H	0000H
0DH	0000H
12H	8B2AH
13H	3BF7H
14H	38DFH
15H	4E77H
16H	2E90H
17H	0000H
19H	0000H
1AH	2000H
1BH	4000H
1DH	4000H
20H	0010H
21H	4000H
23H	4000H
24H	1600H
25H	2A00H
26H	3FF0H
27H	8000H
28H	0000H
2DH	0008H
30H	0000H
32H	0000H
41H	8000H
46H	0000H
50H	0008H
58H	0008H

Table 8-1.

* For Fs = 44.1kHz. Please inquire with regard to use at other than Fs = 44.1kHz, as the fixed values change.

(2) Setting Data

The relationships between the coefficient RAM and each function during DSP operation are as follows.

Address	Name	Function	Setting value
00H	Ki	SI data input level control	Refer to Table 12-1 for setting value
04H	Ke	De-emphasis ON/OFF	ON/AC19H; OFF/0000H
05H	KisLm	SI CH1 data → Lch mix	Refer to Table 12-1 for setting value
06H	KisRc	SI CH2 data → Lch mix	Refer to Table 12-1 for setting value
07H	KiaLm	ADC CH1 data → Lch mix	Refer to Table 12-1 for setting value
08H	KiaRc	ADC CH2 data → Lch mix	Refer to Table 12-1 for setting value
09H	KisRm	SI CH2 data → Rch mix	Refer to Table 12-1 for setting value
0AH	KisLc	SI CH1 data → Rch mix	Refer to Table 12-1 for setting value
0BH	KiaRm	ADC CH2 data → Rch mix	Refer to Table 12-1 for setting value
0CH	KiaLc	ADC CH1 data → Rch mix	Refer to Table 12-1 for setting value
0EH	DC1sw	DC cut1 ON/OFF for accompaniment	ON/4000H; OFF/0000H
0FH	DC1f0	DC cut1 cut-off frequency for accompaniment	Refer to Table 14-1 for setting value
10H	PL	Panpot volume for voice cancellation	Refer to Table 9-1 for setting value
11H	PR	Panpot volume for voice cancellation	Refer to Table 9-1 for setting value
18H	Kvc	Voice cancelling ON/OFF	ON/8000H; OFF/0000H
22H	nRpR	Pitch ratio for accompaniment	Refer to Table 10-1 for setting value
2EH	Ks	Key control ON/OFF for accompaniment	ON/8000H; OFF/0000H
31H	Kimc	Microphone input level control	Refer to Table 12-1 for setting value
33H	DC2f0	DC cut2 cut-off frequency for voice	Refer to Table 14-1 for setting value
34H	DC2sw	DC cut2 ON/OFF for voice	ON/4000H; OFF/0000H
35H	PEQa	PEQ coefficient for voice	Refer to Table 14-4 for setting value
36H	PEQb1	PEQ coefficient for voice	Refer to Table 14-4 for setting value
37H	PEQb2	PEQ coefficient for voice	Refer to Table 14-4 for setting value
38H	PEQg	PEQ coefficient for voice	Refer to Table 14-5 for setting value
39H	HC1a1	High cut1 for voice	Refer to Table 14-2 for setting value
3AH	HC1a0	High cut1 for voice	Refer to Table 14-2 for setting value
3BH	HC1b	High cut1 for voice	Refer to Table 14-2 for setting value
3CH	Kdry	Microphone input direct sound mix	Refer to Table 12-1 for setting value
3DH	Keff	Microphone input echo mix	Refer to Table 12-1 for setting value
3EH	KLm	Key control output Lch mix for accompaniment	Refer to Table 12-1 for setting value
3FH	KRm	Key control output Rch mix for accompaniment	Refer to Table 12-1 for setting value
40H	KLo	System volume Lch	Refer to Table 12-1 for setting value
42H	KRo	System volume Rch	Refer to Table 12-1 for setting value
44H	Tdo	Microphone echo delay amount	Refer to Table 11-1 for setting value
45H	Kre	Microphone echo read tap volume	Refer to Table 12-2 for setting value

Table 8-2 (1). Coefficient RAM Setting Data (1/2)

Address	Name	Function	Setting value
47H	Tre	Microphone echo read tap address	Refer to Table 11-1 for setting value
49H	Krd	Microphone echo input sound mix	Refer to Table 12-1 for setting value
4AH	Kfb	Microphone echo reverberation sound mix	Refer to Table 12-1 for setting value
4BH	HC2a1	Microphone echo high cut2	Refer to Table 14-3 for setting value
4CH	HC2a0	Microphone echo high cut2	Refer to Table 14-3 for setting value
4DH	HC2b	Microphone echo high cut2	Refer to Table 14-3 for setting value
53H	VnRpR	Voice pitch ratio	Refer to Table 10-1 for setting value
5AH	Krmc	Microphone input mix	Refer to Table 12-1 for setting value
5BH	Krmp	Voice pitch control output mix	Refer to Table 12-1 for setting value

Table 8-2. Coefficient RAM Setting Data (2/2)

* Refer to 13. DSP Signal Flow regarding the names.

9. Voice Canceller Settings

[Relevant pins] PL (address = 10H), PR (address = 11H), Kvc (address = 18H)

The vocal sound set at the center can be cancelled by setting Kvc = 8000H and PL, PR = 7000H.

Voice canceling at other than center setting can be done by the panpot volume.

Panpot volume value is PL for CH1, and PR for CH2, and at the center position they are both 0.857. When voice cancellation is OFF, set Kvc = 0000H and PL, PR = 0000H.

PL and PR setting values are hexadecimal notation with D15 as MSB and D0 as LSB.

PL	PR	Setting position	PL	PR	Setting position
7000H	7000H	center	7000H	7000H	center
7000H	6000H		6000H	7000H	
7000H	5000H		5000H	7000H	
7000H	4000H		4000H	7000H	
7000H	3000H		3000H	7000H	
7000H	2000H		2000H	7000H	
7000H	1000H		1000H	7000H	
7000H	0000H	CH2	0000H	7000H	CH1

Table 9-1. Settings for Voice Canceller Panpot Volume

10. Key Controller Setting

[Relevant coefficients] nRpR (address = 22H), Ks (address = 2EH), VnRpR (address = 53H), Krmp (address = 5BH)

(1) Key Controller Pitch Ratio

nRpR (D15,.....,D2) is a 2's complement format with a decimal point between D14 and D13, and sets the desired pitch ratio directly. (VnRpR has the same type of setting as nRpR.)

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The expression range for the pitch ratio is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$

but for practical use it is: $-0.5 \leq nRpR \leq 1.0$
or ±1 octave.

Use within a range of ± half an octave is recommended for quality of sound, although it depends on the aim and the source.
Also, the algorithm is such that allophones will not be generated even when nRpR setting value is changed.

(2) Notes on Key Controller OFF

The pitch does not change when nRpR and VnRpR are set to 0000H (OFF) when the key controller is OFF, but depending on the internal state during OFF, there is no guarantee that the input value will be output as is. During OFF, after setting nRpR and VnRpR to 0000H (OFF), set the pitch control section to through state with the following settings.

Accompaniment controller OFF: Ks = 0000H (OFF)

Voice key controller OFF: sKrmp = 0000H (OFF)

(3) Examples of Key Controller Setting

Examples of pitch ratio setting are illustrated below.
nRpR setting values are hexadecimal notation with D15 as MSB and D2 as LSB for a total of 14 bits.
(D1 and D0 can be optional data.)

CENT	nPpR	CENT	nPpR
0	0000H	0	0000H
+50	01E0H	–50	FE2EH
+100	03CEH	–100	FC69H
+150	05CAH	–150	FAB1H
+200	07D6H	–200	F905H
+250	09F1H	–250	F765H
+300	0C1BH	–300	F5D2H
+350	0E56H	–350	F44AH
+400	10A2H	–400	F2CCH
+450	12FFH	–450	F15AH
+500	156EH	–500	EFF3H
+550	17EEH	–550	EE95H
+600	1A82H	–600	ED42H
+650	1D29H	–650	EBF8H
+700	1FE4H	–700	EAB8H
+750	22B3H	–750	E980H
+800	2597H	–800	E852H
+850	2892H	–850	E72CH
+900	2BA2H	–900	E60EH
+950	2EC9H	–950	E4F9H
+1000	3208H	–1000	E3ECH
+1050	3560H	–1050	E2E6H
+1100	38D0H	–1100	E1E8H
+1150	3C5BH	–1150	E0F1H
+1200	4000H	–1200	E000H

Table 10-1. Pitch Ratio Setting Examples

The numeric representation format for pitch ratio here is:

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The numeric representation range is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$
Also, the relationship formula with music word cent value C is:

$$nRpR = 2^{\frac{C}{1200}} - 1,\ C = 1200 \log^2 [nRpR + 1]\ [cent]$$

The semitone at average ratio is 100 [cent].

11. Microphone Echo Delay Amount Setting

[Relevant coefficients] Tdo (address = 44H), Tre (address = 47H)

Microphone echo delay amount can be varied by setting coefficient Tdo (12 bits from D14 to D3) values. The relationships between the coefficient and the delay amount are shown in Table 11-1.

Coefficient Tre (12 bits from D14 to D3) is microphone input echo initial delay time.
Set in the range of 0008H to Tdo.

Setting value Tdo		Delay (fs = 44.1kHz)	
0008H 0010H 0018H 7ff0H 7ff8H 0000H	4096step	0.045ms 185.76ms	0.045 ms/step setting possible

Table 11-1. Microphone Echo Delay Amount Setting

* When Fs = 44.1kHz. Please inquire with regard to use at other than Fs = 44.1kHz, as the delay amount changes.

12. Input/Output Level Settings

[Relevant coefficients] Ki (address = 00H), KisLm (address = 05H), KisRc (address = 06H), KiaLm (address = 07H), KiaRc (address = 08H), KisRm (address = 09H), KisLc (address = 0AH), KiaRm (address = 0BH), KiaLc (address = 0CH), Kimc (address = 31H), Kdry (address = 3CH), Keff (address = 3DH), KLm (address = 3EH), KRm (address = 3FH), KLo (address = 40H), KRo (address = 42H), Kre (address = 45H), Krd (address = 49H), Kfb (address = 4AH), Krmc (address = 5AH), Krmp (address = 5BH)

The input/output levels and volumes are 2's complement format with a decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.
The coefficient and level relationships are as follows.

D15 to D0	Level
8000H ↓ FFFFH 0000H	0dB ↓ –90.31dB – ∞

Table 12-1. Input/Output Level Settings (other than Kre)

D15 to D0	Level
8000H ↓ FFFFH 0000H	+12.04dB ↓ –78.27dB – ∞

Table 12-2. Input/Output Level Settings (Kre)

The input/output levels for 8001H to FFFEH are determined by the following formulas.

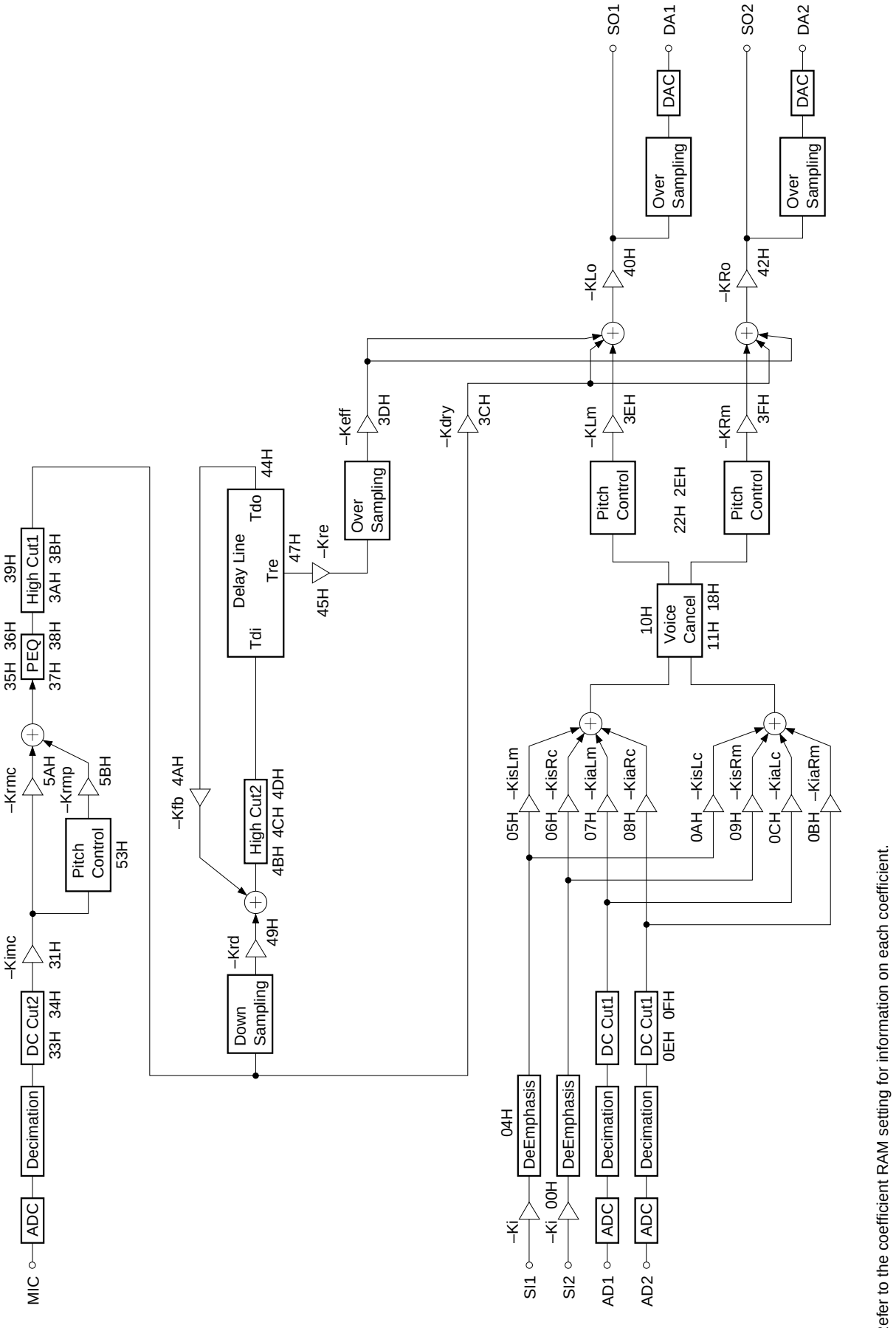
$$(\text{Coefficient value}) = [\,(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}] \times (-1) \quad \text{for other than Kre}$$

$$(\text{Coefficient value}) = [\,(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}] \times (-4) \quad \text{for Kre}$$

Input/output level = 20 log [coefficient value] dB

* D15 to D0 are negative values, but the calculation is (–1) × (D15 to D0).

13. DSP Signal Flow



* Refer to the coefficient RAM setting for information on each coefficient.

14. Filter Coefficient Table

[Relevant coefficient] DC1f0 (address = 0FH), DC2f0 (address = 33H), HC1b (address = 3BH), HC1a1 (address = 39H), HC1a0 (address = 3AH), HC2b (address = 4DH), HC2a1 (address = 4BH), HC2a0 (address = 4CH), PEQa (address = 35H), PEQb1 (address = 36H), PEQb2 (address = 37H), PEQg (address = 38H)

The cut-off frequencies and PEQ gain, Q, and center frequency settings for each signal flow filter are shown in Tables 13-1 to 13-5.

Note that if the above setting values are changed during DSP operation, the output level becomes unstable for several 1/fs.

Tables 14-1 to 14-5 and digital de-emphasis are given for fs = 44.1kHz. Please inquire with regard to using an fs other than this value.

(1) DC Cut1 for Accompaniment/ DC Cut2 for Voice

Cut-off frequency (Hz)	DC1f0 DC2f0	Cut-off frequency (Hz)	DC1f0 DC2f0	Cut-off frequency (Hz)	DC1f0 DC2f0	Cut-off frequency (Hz)	DC1f0 DC2f0
20	7FA2	270	7B2B	520	76D9	770	72AC
30	7F74	280	7AFE	530	76AE	780	7282
40	7F45	290	7AD1	540	7683	790	7258
50	7F17	300	7AA4	550	7657	800	722E
60	7EE9	310	7A77	560	762C	810	7204
70	7EBA	320	7A4B	570	7601	820	71DB
80	7E8C	330	7A1E	580	75D6	830	71B1
90	7E5E	340	79F1	590	75AB	840	7187
100	7E30	350	79C5	600	7580	850	715D
110	7E02	360	7998	610	7555	860	7134
120	7DD4	370	796C	620	752A	870	710A
130	7DA6	380	7940	630	74FF	880	70E1
140	7D78	390	7914	640	74D4	890	70B7
150	7D4B	400	78E7	650	74A9	900	708E
160	7D1D	410	78BB	660	747E	910	7064
170	7CEF	420	788F	670	7454	920	703B
180	7CC2	430	7863	680	7429	930	7012
190	7C94	440	7837	690	73FF	940	6FE9
200	7C67	450	780B	700	73D4	950	6FBF
210	7C39	460	77DF	710	73AA	960	6F96
220	7C0C	470	77B4	720	737F	970	6F6D
230	7BDF	480	7788	730	7355	980	6F44
240	7BB2	490	775C	740	732B	990	6F1B
250	7B85	500	7731	750	7301	1000	6EF2
260	7B58	510	7705	760	72D6		

Table 14-1.

(2) High Cut1 for Voice

Cut-off frequency (Hz)	HC1b	HC1a1	HC1a0	Cut-off frequency (Hz)	HC1b	HC1a1	HC1a0
1000	6EF2	0886	F77A	5600	3416	25F4	DA0C
1100	6D5C	0951	F6AF	5700	3306	267C	D984
1200	6BCB	0A1A	F5E6	5800	31F9	2703	D8FD
1300	6A3E	0AE0	F520	5900	30EC	2789	D877
1400	68B6	0BA4	F45C	6000	2FE2	280E	D7F2
1500	6733	0C66	F39A	6100	2ED8	2893	D76D
1600	65B4	0D25	F2DB	6200	2DD0	2917	D6E9
1700	6439	0DE3	F21D	6300	2CCA	299A	D666
1800	62C3	0E9E	F162	6400	2BC4	2A1D	D5E3
1900	6150	0F57	F0A9	6500	2AC0	2A9F	D561
2000	5FE2	100E	EFF2	6600	29BD	2B21	D4DF
2100	5E77	10C4	EF3C	6700	28BC	2BA1	D45F
2200	5D11	1177	EE89	6800	27BB	2C22	D3DE
2300	5BAE	1228	EDD8	6900	26BC	2CA1	D35F
2400	5A4E	12D8	ED28	7000	25BD	2D21	D2DF
2500	58F2	1386	EC7A	7100	24C0	2D9F	D261
2600	579A	1432	EBCE	7200	23C4	2E1D	D1E3
2700	5645	14DD	EB23	7300	22C9	2E9B	D165
2800	54F3	1586	EA7A	7400	21CF	2F18	D0E8
2900	53A4	162D	E9D3	7500	20D5	2F95	D06B
3000	5259	16D3	E92D	7600	1FDD	3011	CFEF
3100	5110	1777	E889	7700	1EE6	308C	CF74
3200	4FCB	181A	E7E6	7800	1DEF	3108	CEF8
3300	4E88	18BB	E745	7900	1CF9	3183	CE7D
3400	4D48	195B	E6A5	8000	1C04	31FD	CE03
3500	4C0B	19FA	E606	8100	1B10	3277	CD89
3600	4AD0	1A97	E569	8200	1A1C	32F1	CD0F
3700	4998	1B33	E4CD	8300	192A	336A	CC96
3800	4863	IBCE	E432	8400	1838	33E3	CC1D
3900	4730	1C67	E399	8500	1746	345C	CBA4
4000	4600	1CFF	E301	8600	1655	34D5	CB2B
4100	44D2	1D96	E26A	8700	1565	354D	CAB3
4200	43A6	1E2C	E1D4	8800	1475	35C5	CA3B
4300	427C	1EC1	E13F	8900	1386	363C	C9C4
4400	4155	1F55	E0AB	9000	1298	36B3	C94D
4500	4030	1FE7	E019	9100	11A9	372B	C8D5
4600	3F0D	2079	DF87	9200	10BC	37A1	C85F
4700	3DEC	2109	DEF7	9300	0FCF	3818	C7E8
4800	3CCD	2199	DE67	9400	0EE2	388E	C772
4900	3BAF	2228	DDD8	9500	0DF5	3905	C6FB
5000	3A94	22B5	DD4B	9600	0D09	397B	C685
5100	397B	2342	DCBE	9700	0C1E	39F0	C610
5200	3863	23CE	DC32	9800	0B32	3A66	C59A
5300	374D	2459	DBA7	9900	0A47	3ADC	C524
5400	3639	24E3	DB1D	10000	095C	3B51	C4AF
5500	3527	256C	DA94	OFF	0000	0000	8000

Table 14-2.

(3) High Cut2 for Microphone Echo

Cut-off frequency (Hz)	HC2b	HC2a1	HC2a0	Cut-off frequency (Hz)	HC2b	HC2a1	HC2a0
1000	5FE2	100E	EFF2	5600	FE68	40CC	BF34
1100	5D11	1177	EE89	5700	FC95	41B5	BE4B
1200	5A4E	12D8	ED28	5800	FAC2	429F	BD61
1300	579A	1432	EBCE	5900	F8EE	4389	BC77
1400	54F3	1586	EA7A	6000	F719	4473	BB8D
1500	5259	16D3	E92D	6100	F543	455E	BAA2
1600	4FCB	181A	E7E6	6200	F36C	464A	B9B6
1700	4D48	195B	E6A5	6300	F194	4736	B8CA
1800	4AD0	1A97	E569	6400	EFBB	4822	B7DE
1900	4863	1BCE	E432	6500	EDE0	4910	B6F0
2000	4600	1CFF	E301	6600	EC02	49FF	B601
2100	43A6	1E2C	E1D4	6700	EA23	4AEE	B512
2200	4155	1F55	E0AB	6800	E841	4BDF	B421
2300	3F0D	2079	DF87	6900	E65D	4CD1	B32F
2400	3CCD	2199	DE67	7000	E476	4DC5	B23B
2500	3A94	22B5	DD4B	7100	E28C	4EBA	B146
2600	3863	23CE	DC32	7200	E09F	4FB0	B050
2700	3639	24E3	DB1D	7300	DEAE	50A9	AF57
2800	3416	25F4	DA0C	7400	DCBA	51A3	AE5D
2900	31F9	2703	D8FD	7500	DAC1	529F	AD61
3000	2FE2	280E	D7F2	7600	D8C5	539D	AC63
3100	2DD0	2917	D6E9	7700	D6C4	549E	AB62
3200	2BC4	2A1D	D5E3	7800	D4BE	55A1	AA5F
3300	29BD	2B21	D4DF	7900	D2B3	56A6	A95A
3400	27BB	2C22	D3DE	8000	D0A3	57AE	A852
3500	25BD	2D21	D2DF	8100	CE8E	58B9	A747
3600	23C4	2E1D	D1E3	8200	CC72	59C7	A639
3700	21CF	2F18	D0E8	8300	CA50	5AD8	A528
3800	1FDD	3011	CFEF	8400	C828	5BEC	A414
3900	1DEF	3108	CEF8	8500	C5F9	5D03	A2FD
4000	1C04	31FD	CE03	8600	C3C2	5E1F	A1E1
4100	1A1C	32F1	CD0F	8700	C184	5F3E	A0C2
4200	1838	33E3	CC1D	8800	BF3E	6061	9F9F
4300	1655	34D5	CB2B	8900	BCEF	6188	9E78
4400	1475	35C5	CA3B	9000	BA98	62B4	9D4C
4500	1298	36B3	C94D	9100	B837	63E4	9C1C
4600	10BC	37A1	C85F	9200	B5CC	651A	9AE6
4700	0EE2	388E	C772	9300	B357	6654	99AC
4800	0D09	397B	C685	9400	B0D7	6794	986C
4900	0B32	3A66	C59A	9500	AE4C	68DA	9726
5000	095C	3B51	C4AF	9600	ABB5	6A25	95DB
5100	0788	3C3B	C3C5	9700	A911	6B77	9489
5200	05B3	3D26	C2DA	9800	A660	6CD0	9330
5300	03E0	3E0F	C1F1	9900	A3A1	6E2F	91D1
5400	020D	3EF9	C107	10000	A0D4	6F96	906A
5500	003A	3FE2	C01E	OFF	0000	0000	8000

Table 14-3.

(4) PEQ for Voice

Center frequency (Hz)	PEQa	PEQb1	PEQb2
250.0	023D	7DAE	847B
280.6	0282	7D64	8505
315.0	02CF	7D10	859F
353.6	0325	7CB2	864B
396.9	0385	7C47	870B
445. 4	03F0	7BCF	87E1
500. 0	0467	7B48	88CF
561.2	04EC	7AAE	89D9
630.0	0580	7A01	8B01
707.1	0624	793D	8C4A
793.7	06DB	785E	8DB7
890.9	07A6	7762	8F4D
1000. 0	0886	7643	910E
1122.5	097E	74FD	92FE
1259.9	0A91	738B	9524
1414.2	0BC0	71E5	9781
1587.4	0D0D	7004	9A1C
1781.8	0E7C	6DE0	9CFA
2000.0	100E	6B6D	A01E
2244.9	11C7	68A1	A38F
2519.8	13A8	656E	A752
2828.4	15B5	61C6	AB6C
3174.8	17F1	5D97	AFE4
3563.6	1A5E	58CF	B4BE
4000.0	1CFF	535A	BA00
4489.8	1FD8	4D24	BFB2
5039.7	22ED	4617	C5DC
5656.9	2642	3E23	CC85
6349.6	29DB	353B	D3B8
7127.2	2DC1	2B5C	DB84
8000.0	31FD	2097	E3FC

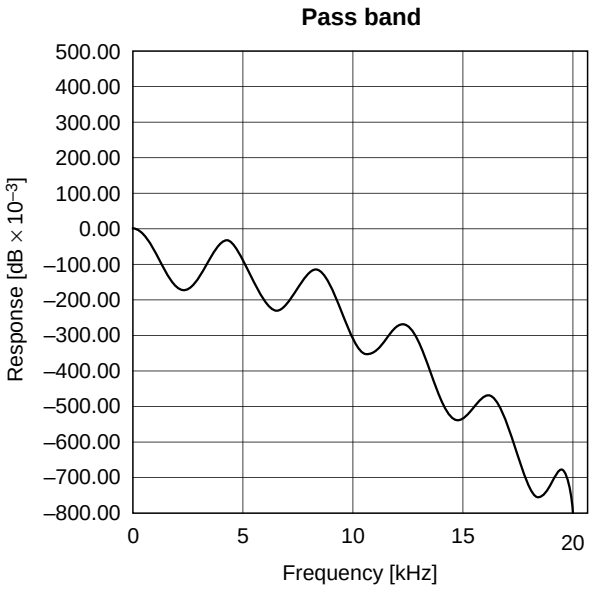
Table 14-4.

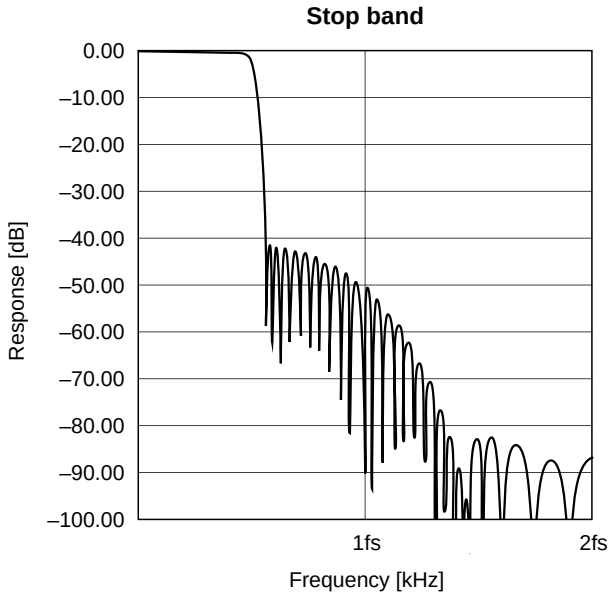
Gain (dB)	PEQg
0.0	0000
0.5	01E5
1.0	03E7
1.5	0608
2.0	0849
2.5	0AAC
3.0	0D33
3.5	0FE1
4.0	12B7
4.5	15B8
5.0	18E7
5.5	1C46
6.0	1FD9
6.5	23A1
7.0	27A3
7.5	2BE2
8.0	3061
8.5	3524
9.0	3A30
9.5	3F88
10.0	4531
10.5	4B30
11.0	518A
11.5	5844
12.0	5F64

Table 14-5.

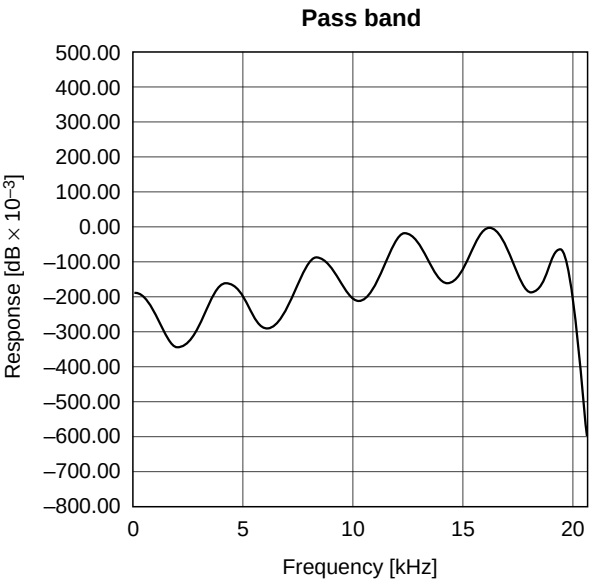
Filter Characteristics

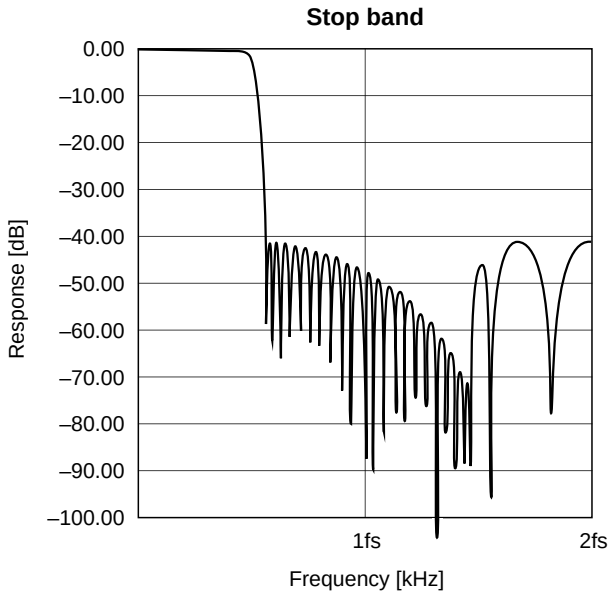
ADC Filter Characteristics (43rd + 15th FIR)



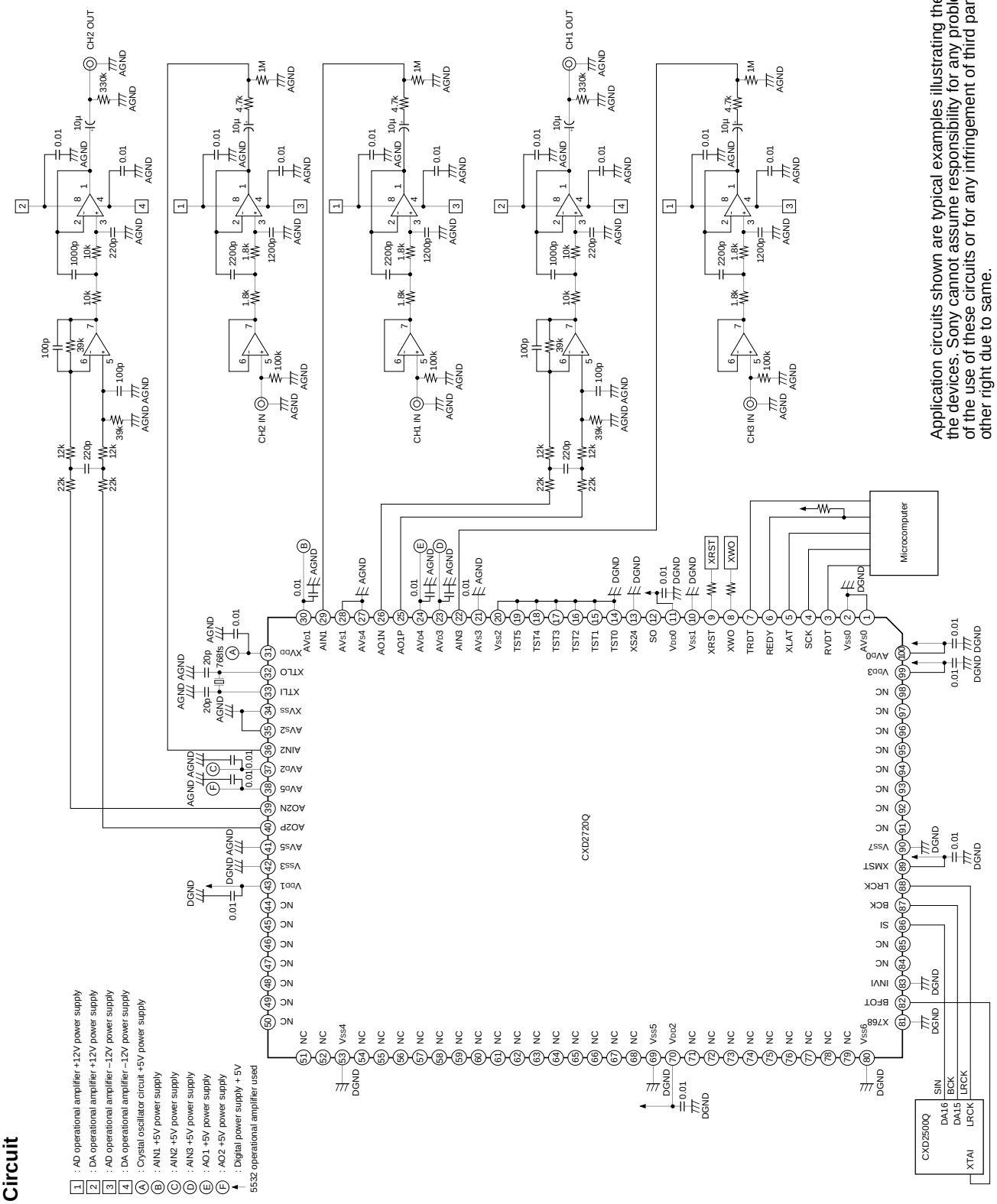


DAC Filter Characteristics (43rd + 7th FIR)





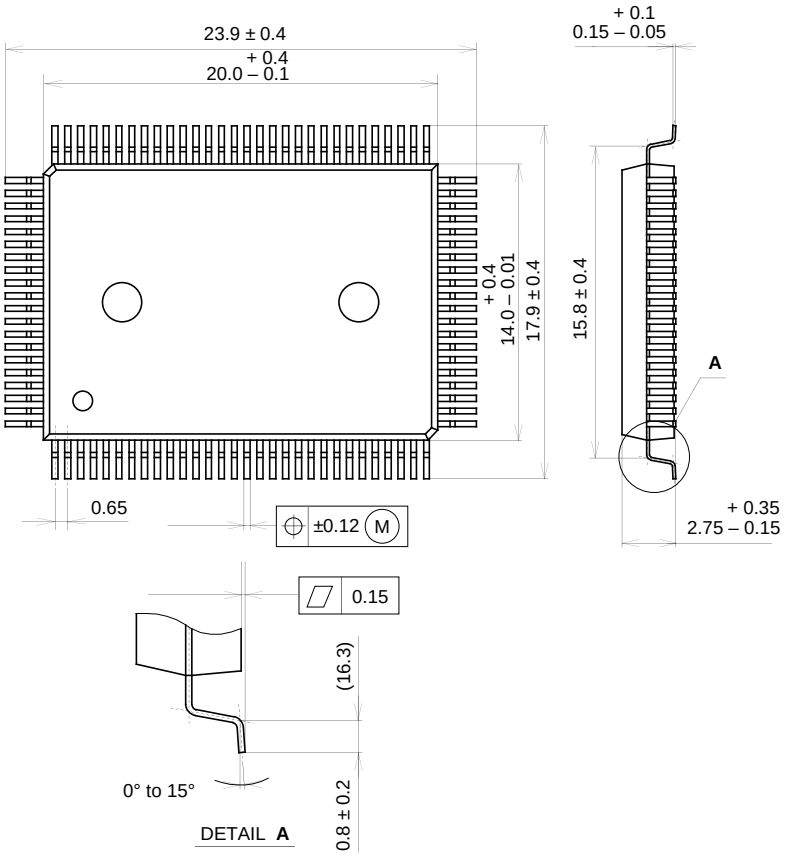
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g