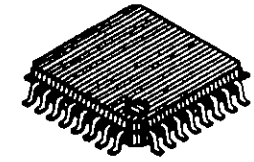
SONY®

CXD2917Q

Digital Audio Data Modulation and Transmission

For the availability of this product, please contact the sales office.

32pin QFP (Plastic)



Description

The CXD2917Q is a digital audio data transmission LSI for consumer use.

Features

- A variety of digital audio equipment can be connected because the channel status data can be set in parallel from the input pins,.
- Four different frequencies (128 Fs, 192 Fs, 256 Fs, or 384 Fs) can be selected for the master clock.
- Switchable dual inputs are provided for both the digital audio data and for the C2 channel status data.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD} Note 1	V_{SS}	−0.5	to		0.7	V
• Input voltage	V_I Note 1	V_{SS}	−0.5	to	V_{DD}	+0.5	V
• Output voltage	V_O Note 1	V_{SS}	−0.5	to	V_{DD}	+0.5	V
• Operating temperature	T_{opr}		−20	to		+75	°C
• Storage temperature	T_{stg}		−55	to		+150	°C

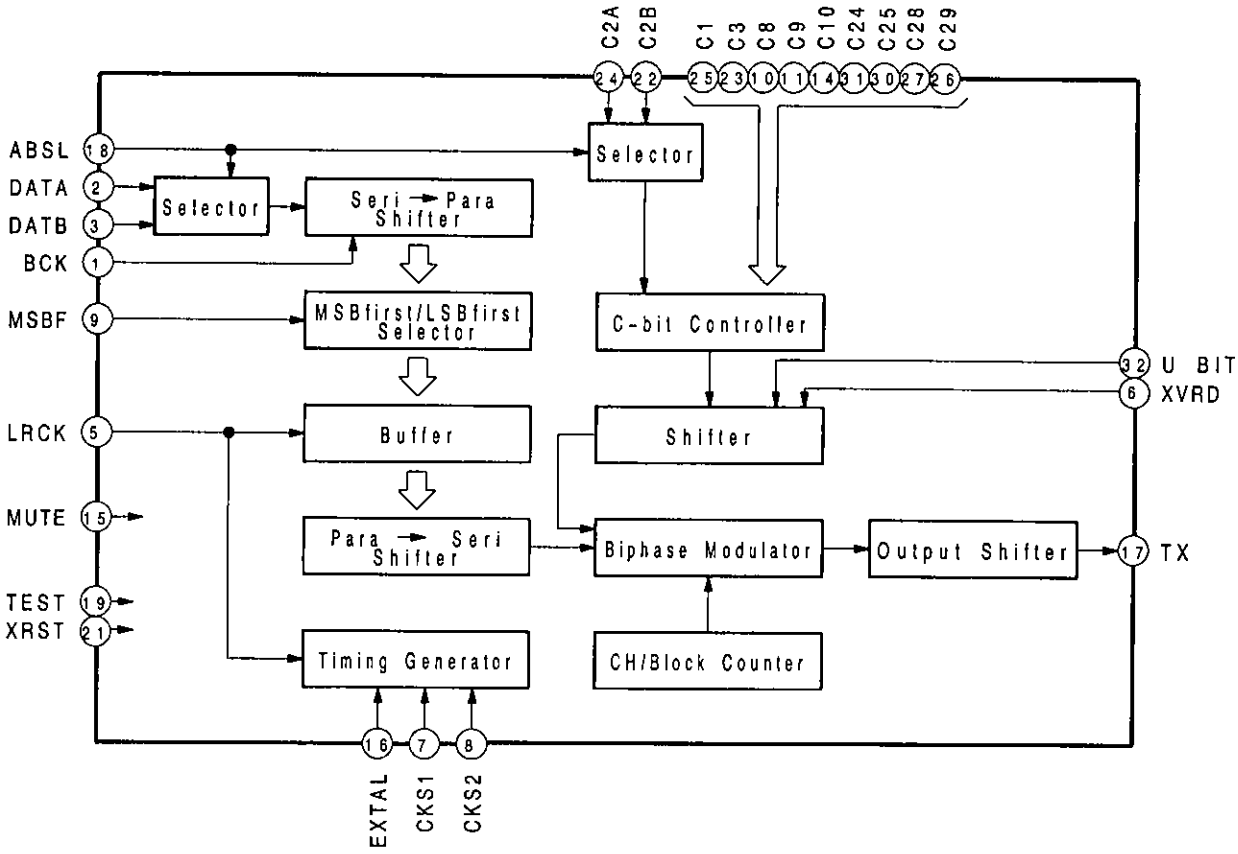
*Note 1 Vss=0 V

Recommended Operating Conditions

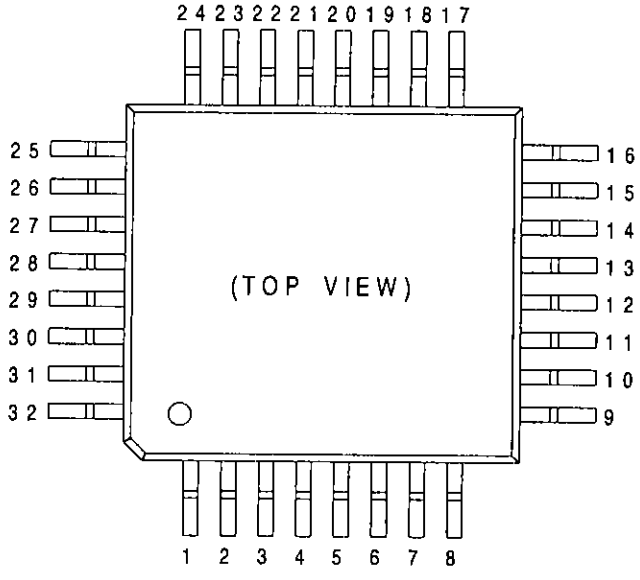
• Operating voltage	V_{DD}	4.5	to	5.5	V (5.0 V typ.)
• Operating temperature	T_{opr}	−20	to	+75	°C

E92613-YA

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	BCK	I	Bit clock input. Data is retrieved at rising edge.
2	DATA	I	Digital audio data input 1 (NR2).
3	DATB	I	Digital audio data input 2 (NR2).
4	Vss	–	GND
5	LRCK	I	LR clock input. High: left channel; Low: right channel
6	XVRD	I	Validity flag input. High when interpolation processing is performed on the data.
7	CKS1	I	Frequency selection input 1 for clock input to EXTAL. 192 Fs, 384 Fs/$\overline{128\ Fs, 256\ Fs}$.
8	CKS2	I	Frequency selection input 2 for clock input to EXTAL. 256 Fs, 384 Fs/$\overline{128\ Fs, 192\ Fs}$.
9	MSBF	I	MSB first/$\overline{\text{LSB first}}$ selection input for data.
10	C8	I	Preset input for channel status data bit 8.
11	C9	I	Preset input for channel status data bit 9.
12	Vss	–	GND
13	VDD	–	+5 V
14	C10	I	Preset input for channel status data bit 10.
15	MUTE	I	Mute input. High: Only audio data on TX will be all "0".
16	EXTAL	I	Clock input. The frequency is selected from 128 Fs, 192 Fs, or 384 Fs by CKS1 (Pin 6) and CKS2 (Pin 8).
17	TX	O	Transmission data output converted to digital audio interface format.
18	ABSL	I	Selection input for DATA (Pin 2)/$\overline{\text{DATB (Pin 3)}}$ and C2A (Pin 24)/$\overline{\text{C2B (Pin 22)}}$.
19	TEST	I	Test mode setting input. Fixed low for normal use.
20	Vss	–	GND
21	XRST	I	Reset input. Fixed high for operation.
22	C2B	I	Preset input 2 for channel status data bit 2.
23	C3	I	Preset input for channel status data bit 3.
24	C2A	I	Preset input 1 for channel status data bit 2.
25	C1	I	Preset input for channel status data bit 1.
26	C29	I	Preset input for channel status data bit 29.
27	C28	I	Preset input for channel status data bit 28.
28	Vss	–	GND
29	VDD	–	+5 V
30	C25	I	Preset input for channel status data bit 25.
31	C24	I	Preset input for channel status data bit 24.
32	UBIT	I	User data input.

Electrical Characteristics

DC characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, Topr = –20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			15		mA
		I_{DSS}	at stand still $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$			0.1	
Output voltage	High level	V_{OH}	I_{OH}=–0.4 mA	4.0		V_{DD}	V
	Low level	V_{OL}	I_{OL}=2.0 mA	V_{SS}		0.4	V
Input voltage	High level	V_{IH}		2.4			V
	Low level	V_{IL}				0.8	V
Input leak current		I_{LI}	V_I=0V to V_{DD}	–10		10	µA

I/O capacitances

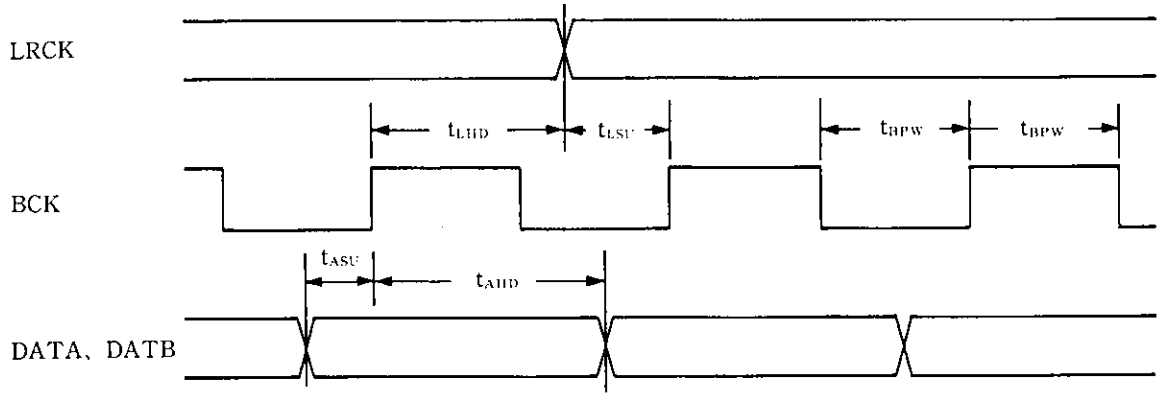
(Ta = 25°C)

V_{DD} = V_I = 0V, fM = 1MHz

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IX}			9	pF.
Output pin	C_{OUT}			9	pF.

AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Setup time of LRCK for BCK	t_{LSU}	50			ns
Hold time of LRCK for BCK	t_{LHD}	50			ns
Setup time of DATA/DATB for BCK	t_{ASU}	50			ns
Hold time of DATA/DATB for BCK	t_{AHD}	50			ns
BCK pulse width	t_{BPW}	100			ns
EXTAL frequency	f_{EXT}			18.5	MHz



Description of Functions

Digital audio data input

Two digital audio data input formats, MSB first/16-bit mode and LSB first/24-bit mode, are provided and can be selected through the MSBF input (Pin 9). (See Fig. 2.)

1) MSB first/16-bit mode (MSBF = high)
   BCK: 16 clocks/words or more
   DATA, DATB: MSB first, 16 bits rearward packing
2) LSB first/24-bit mode (MSBF = low)
   BCK: 24 clocks/words or more
   DATA, DATB: LSB first, 16 bits rearward packing

Validity flag and user data

The validity flag and user data are retrieved at the last BCK of each word of digital audio data so that the value corresponding to each word should be input to XVRD (Pin 6) and UBIT (Pin 32) respectively as shown in Fig. 2.

Channel status data

Bits 0, 6 and 7 of the channel status data are fixed to "0", corresponding to mode 0 for consumer use.

Among bits 0 to 191, this IC can set the following 10 bits: 1, 2, 3, 8, 9, 10, 24, 25 and 29. Set these bits in parallel from the input pins.

These bits can be used to set the following items:

a. Digital data/audio data
b. Emphasis on/off
c. Digital copy enable/disable
d. Category codes (up to 8 kinds)
e. Sampling frequency: 44.1 kHz/48 kHz/32 kHz
f. Clock accuracy: level I/II/III

Dual input selection

This IC is equipped with dual inputs for digital audio data input (DATA/DATB) and channel status data bit 2 (C2A/C2B). These inputs can be switched through the ABSL input pin (Pin 18).

The ABSL input is sampled once through LRCK (Pin 5) in the IC so that the digital audio data is never switched within a single sample.

This function is useful, for example, when inputting the TV main and additional stereo sound signals along with the copy disable signal for dual inputs of satellite broadcast tuner.

Mute function

By setting the MUTE input (Pin 15) high, the audio data on the TX output (Pin 17) can be set to all "0" while keeping the channel status data, user data and others unchanged. Mute is applied in units of one LRCK cycle since the MUTE input is also sampled in the IC through LRCK.

EXTAL (Pin 16) frequency

The clock input to EXTAL can be selected from among four frequencies using CKS1 (Pin 7) and CKS2 (Pin 8) as shown in the table below.

CKS1	CKS2	EXTAL frequency
0	0	128Fs
1	0	192Fs
0	1	256Fs
1	1	384Fs

Table 1. Clock frequency input to EXTAL

However, when inputting 192 Fs to EXTAL, note that the TX output may generate jitters, depending on the clock duty. (See Fig. 1.)

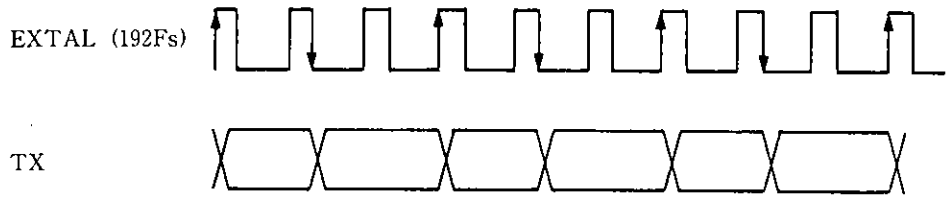


Fig. 1. TX when inputting 192 Fs clock to EXTAL

Input Timing Chart

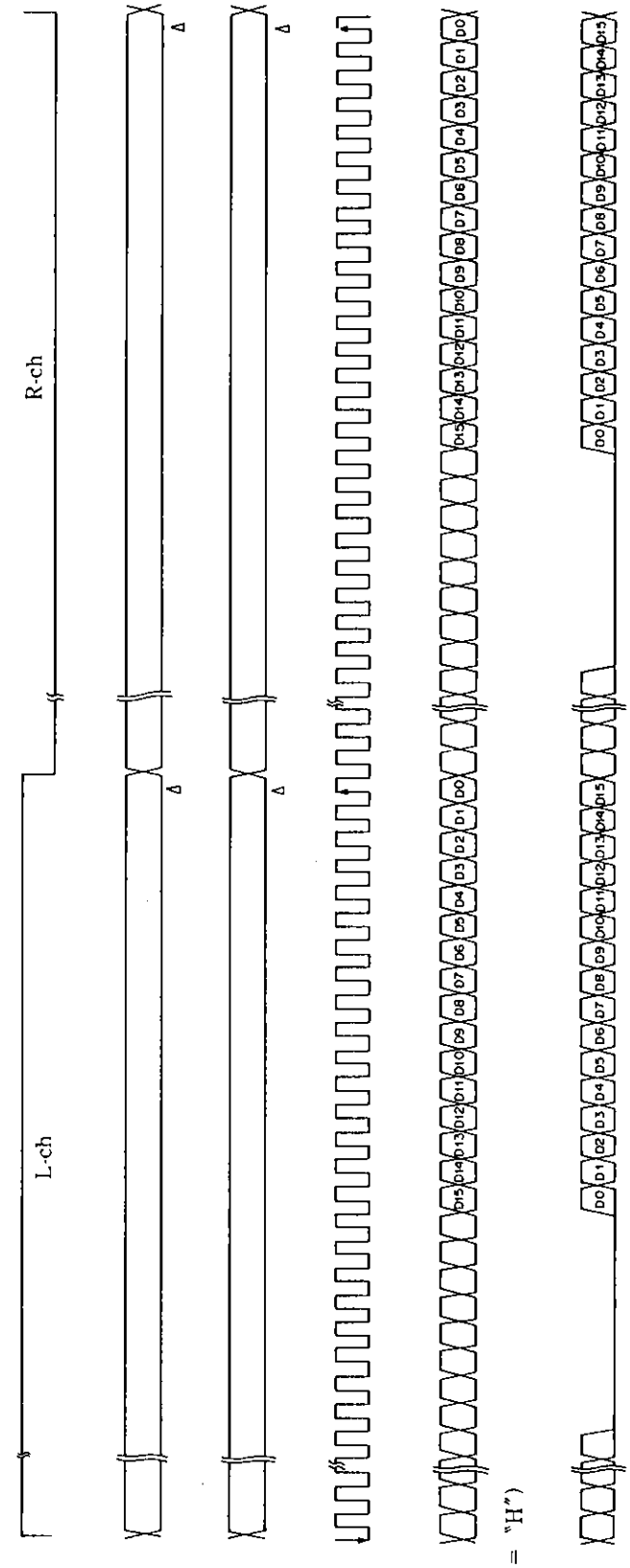
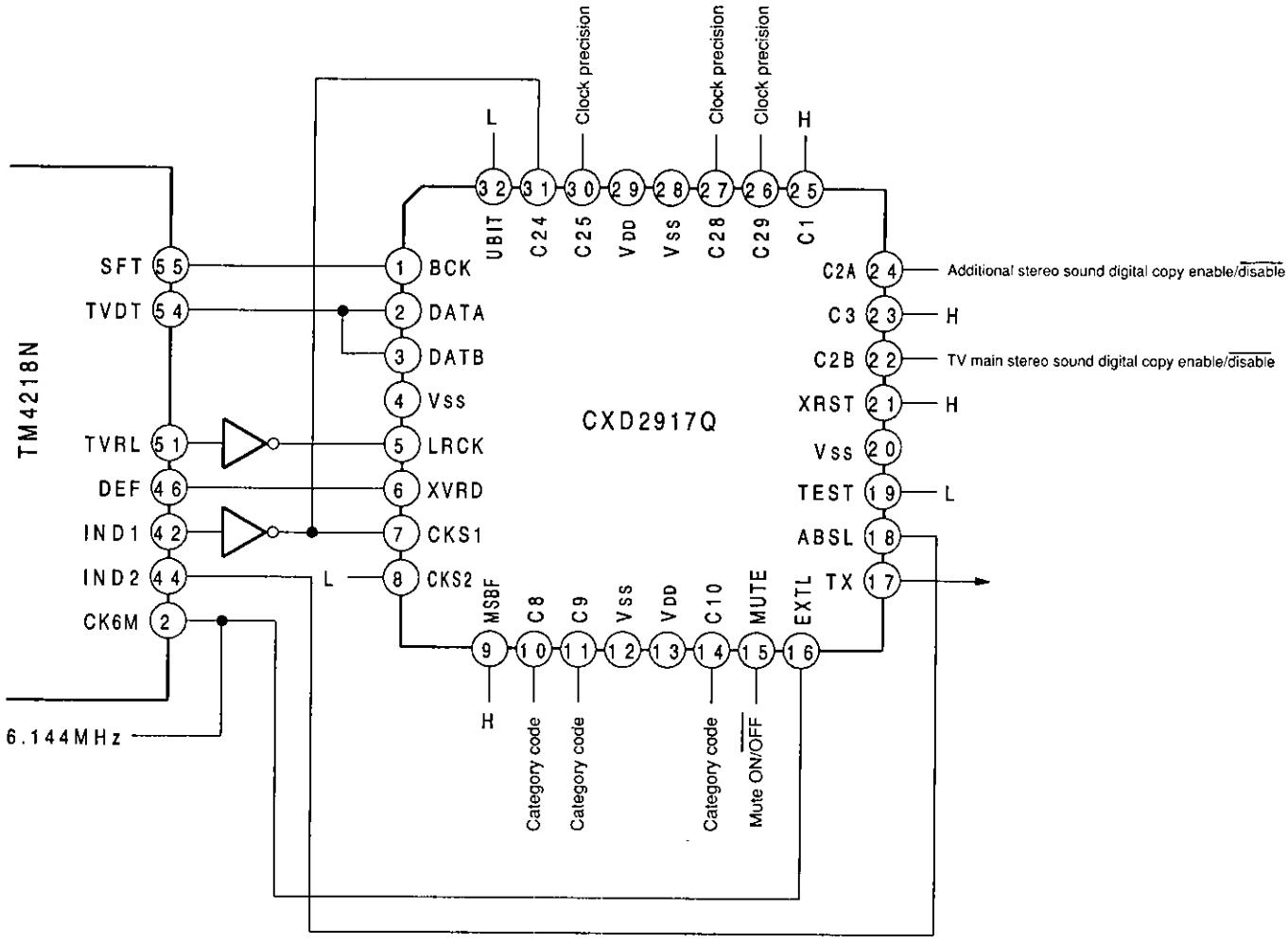


Fig. 2. Input timing chart

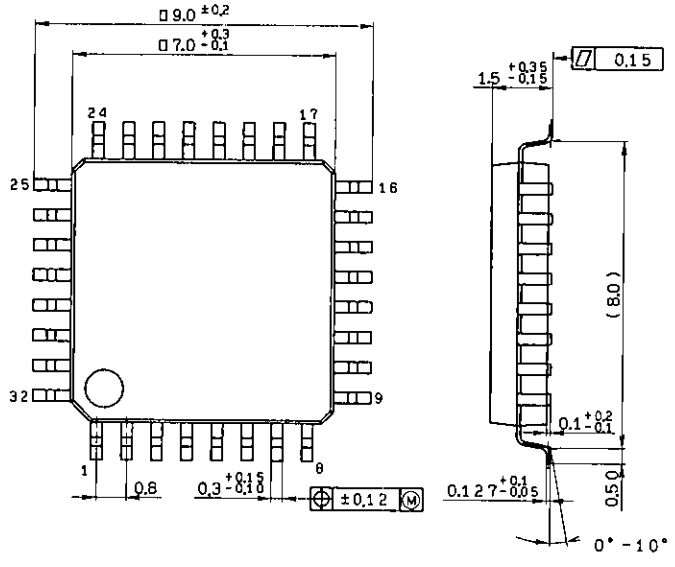
Application Circuit



Example of connection with the audio signal processing IC for B.S. tuner TM4218N (TOSHIBA CORPORATION.)

Package Outline Unit: mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———