SONY

CXK5B81020J/TM -12

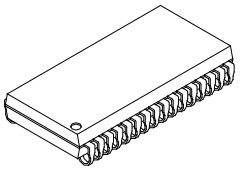
131072-word × 8-bit High Speed Bi-CMOS Static RAM

For the availability of this product, please contact the sales office.

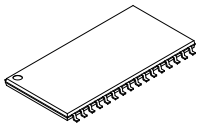
Description

CXK5B81020J/TM is a high speed 1M bit Bi-CMOS static RAM organized as 131072 words by 8 bits. Operating on a single 3.3V supply this asynchronous IC is suitable for use in high speed and low power applications.

CXK5B81020J
32 pin SOJ (Plastic)



CXK5B81020TM
32 pin TSOP (Plastic)



Features

- Single 3.3V power supply: 3.3V ± 0.3V
- Fast access time 12ns (Max.)
- Low standby current: 10mA (Max.)
- Low power operation 864mW (Max.)
- Package line-up

  Dual Vcc/Vss

  CXK5B81020J 400mil 32pin SOJ package

  CXK5B81020TM 400mil 32pin TSOP package

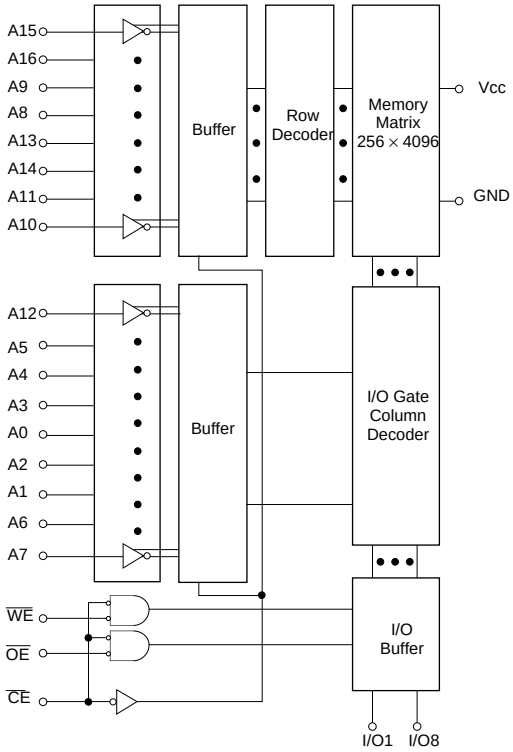
Function

131072 word × 8-bit static RAM

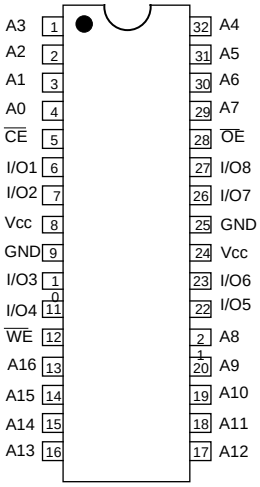
Structure

Silicon gate Bi-CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+3.3V power supply
GND	Ground
NC	No connection

E93707B58-PP

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		–0.5*1 to +4.6	V
Input voltage	V_{IN}		–0.5*1 to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		–0.5*1 to V_{CC} + 0.5	V
Allowable power dissipaiton	P_D		1.5*2	W
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +150	°C
Soldering temperature • time	Tsolder	J	260 • 10	°C • sec
		TM	235 • 10	°C • sec

*1 Vcc, V_{IN}, $V_{I/O}$ = –2.0V Min. for pulse width less than 5ns.

*2 Air flow ≥ 1m/s.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	L	H	Read	Data out	I_{CC}
L	×	L	Write	Data in	I_{CC}
L	H	H	Output disable	High Z	I_{CC}

×: "H" or "L"

Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*	—	0.8	V

* V_{IL} = –2.0V Min. for pulse width less than 5ns.

Electrical Characteristics

DC Characteristics

(Vcc = 3.3V ± 0.3V, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.*	Max	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	–10	—	+10	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}	–10	—	+10	µA
Average operating current	I_{CC}	Cycle: Min. Duty = 100% I_{OUT} = 0mA $\overline{CE}$ = V_{IL} V_{IN} = V_{IH} or V_{IL}	—	—	240	mA
Standby current	I_{SB1}	$\overline{CE}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	—	—	10	mA
	I_{SB2}	Cycle: Min. Duty = 100% $\overline{CE}$ = V_{IH} V_{IN} = V_{IH} or V_{IL}	—	—	100	mA
Output high voltage	V_{OH}	I_{OH} = –2.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.0mA	—	—	0.4	V

* Vcc = 3.3V, Ta = 25°C

I/O Capacitance

(Ta = 25°C, f = 1MHz)

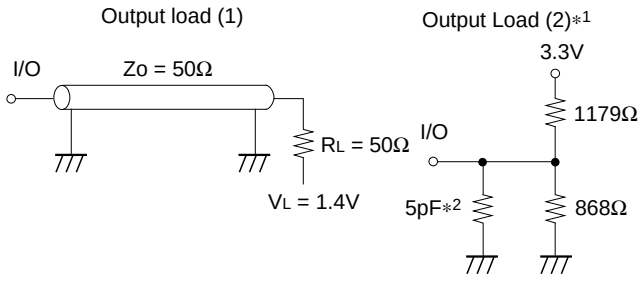
Item	Symbol	Conditions	Min.	Typ.	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	5	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test condition** (Vcc = 3.3V ± 0.3V, Ta = 0 to +75°C)

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0.0V
Input rise time	tr = 2ns
Input fall time	tf = 2ns
Input and output reference level	1.4V
Output load conditions	Fig. 1



*1. t_{LZ}, t_{OLZ}, t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}
*2. Including scope and jig capacitances

Fig. 1

• **Read cycle**

Item	Symbol	-12		Unit
		Min.	Max.	
Read cycle time	t_{RC}	12	—	ns
Address access time	t_{AA}	—	12	ns
Chip enable access time	t_{CO}	—	12	ns
Output enable to output valid	t_{OE}	—	6	ns
Output data hold time	t_{OH}	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	6	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	6	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1 1-(2).
This parameter is sampled and is not 100% tested.

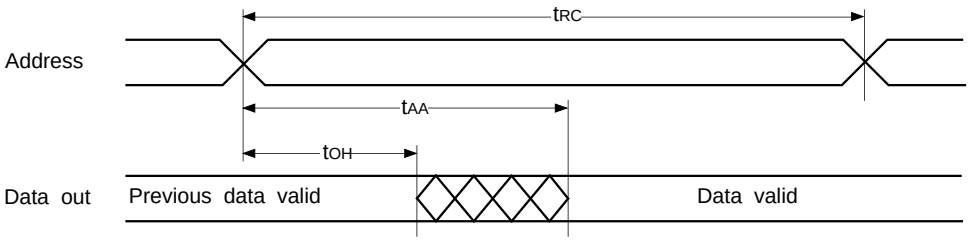
• **Write cycle**

Item	Symbol	-12		Unit
		Min.	Max.	
Write cycle time	t_{WC}	12	—	ns
Address valid to end of write	t_{AW}	10	—	ns
Chip enable to end of write	t_{CW}	10	—	ns
Data valid to end of write	t_{DW}	8	—	ns
Data hold from end of write	t_{DH}	0	—	ns
Write pulse width	t_{WP}	10	—	ns
Address set up time	t_{AS}	0	—	ns
Write recovery time	t_{WR}	0	—	ns
Output active from lend of write	t_{OW}*	4	—	ns
Write to output in high Z	t_{WHZ}*	0	6	ns

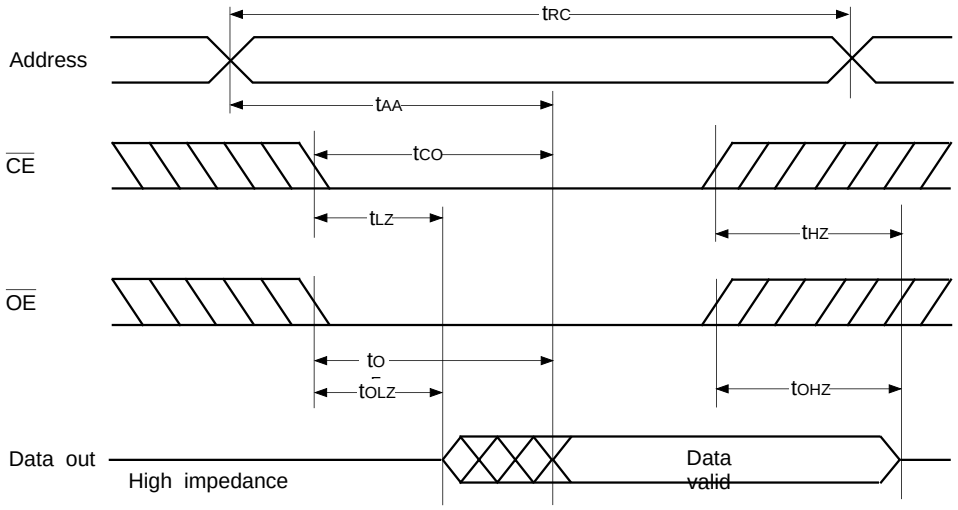
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

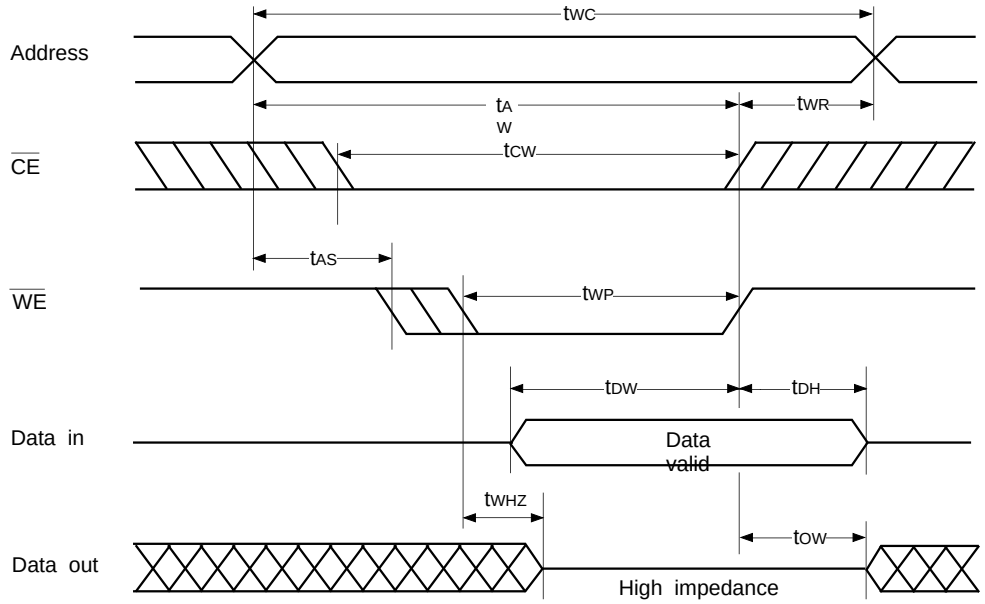
• Read cycle (1) : $\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}



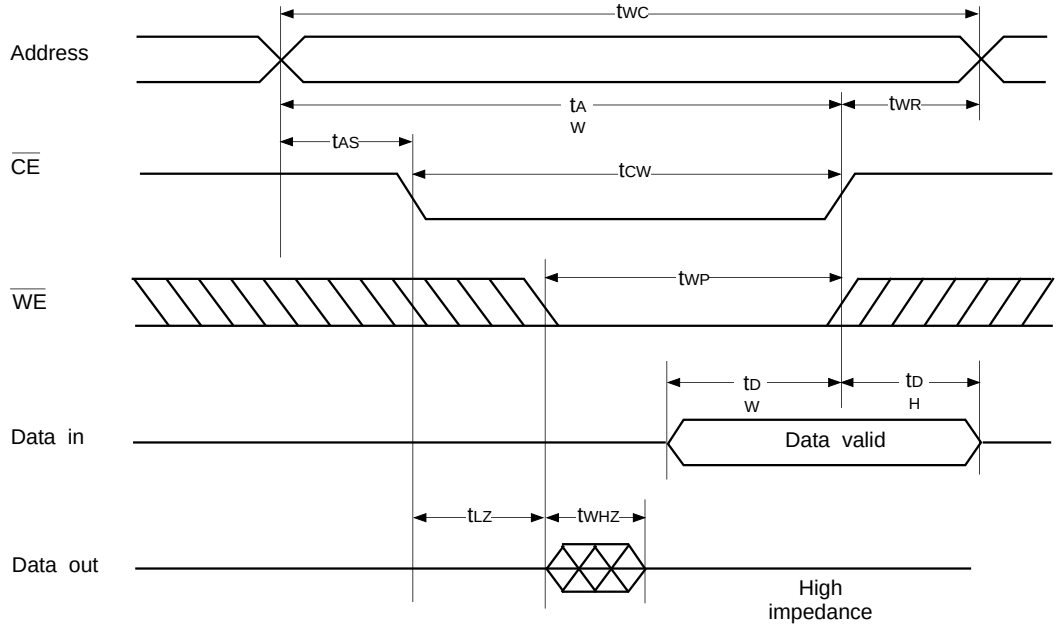
• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



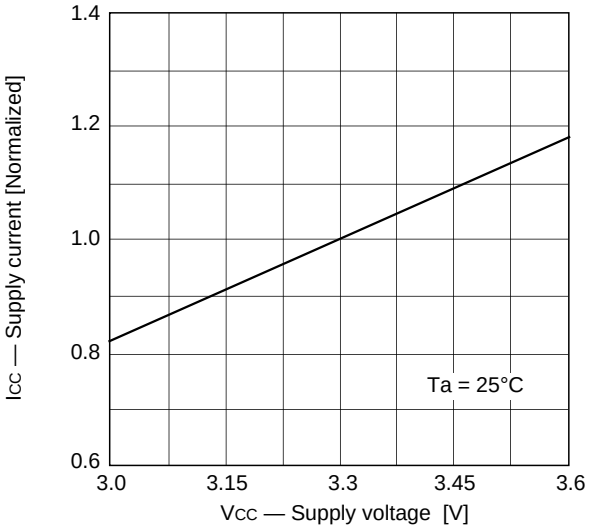
• Write cycle (2) : $\overline{CE}$ control



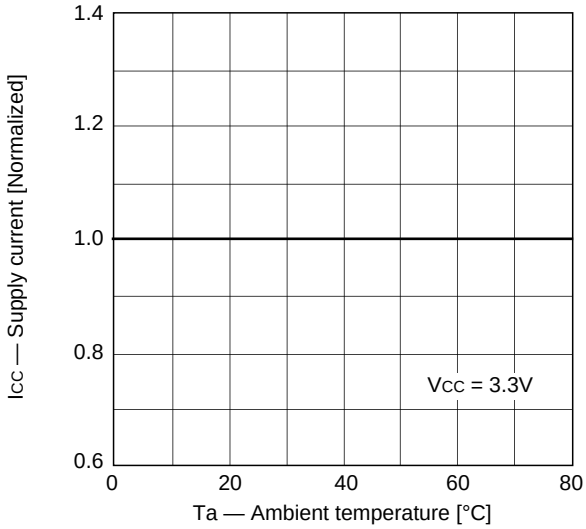
* Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Example of Representative Characteristics

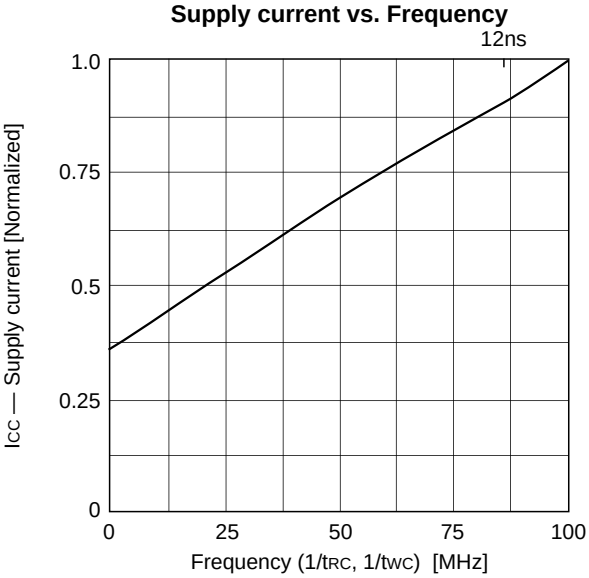
Supply current vs. Supply voltage



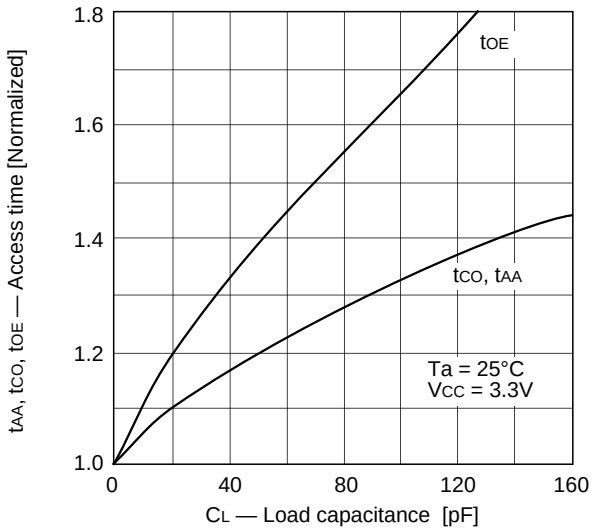
Supply current vs. Ambient temperature



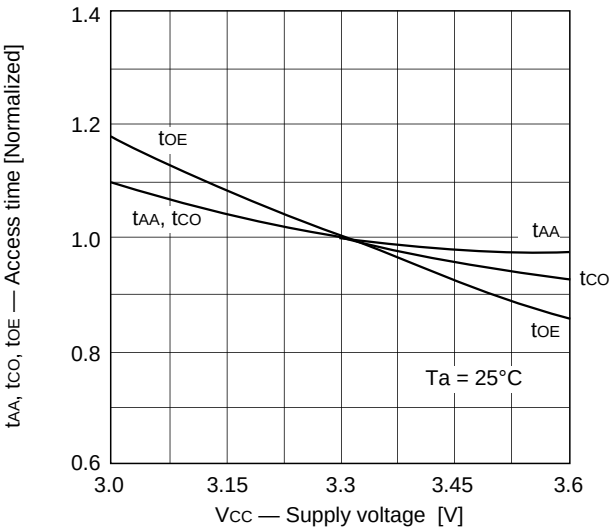
Supply current vs. Frequency



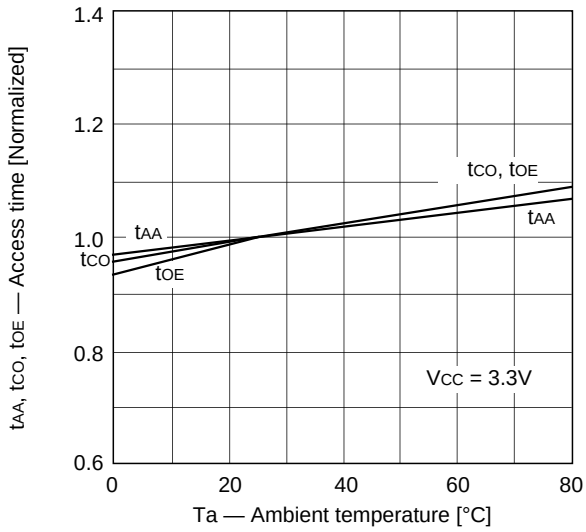
Access time vs. Load capacitance



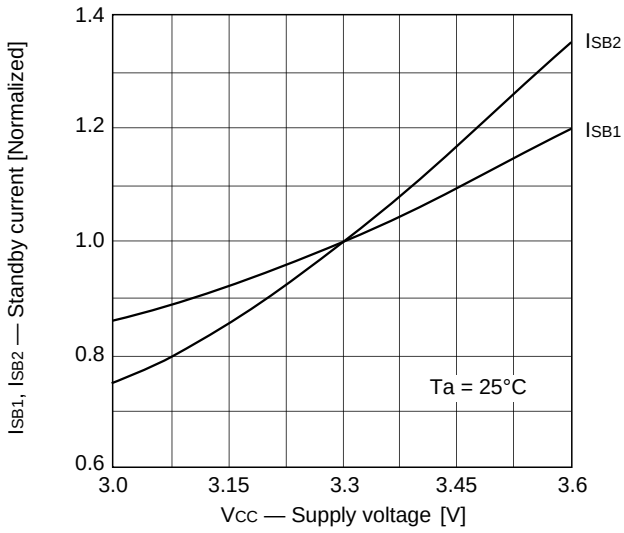
Access time vs. Supply voltage



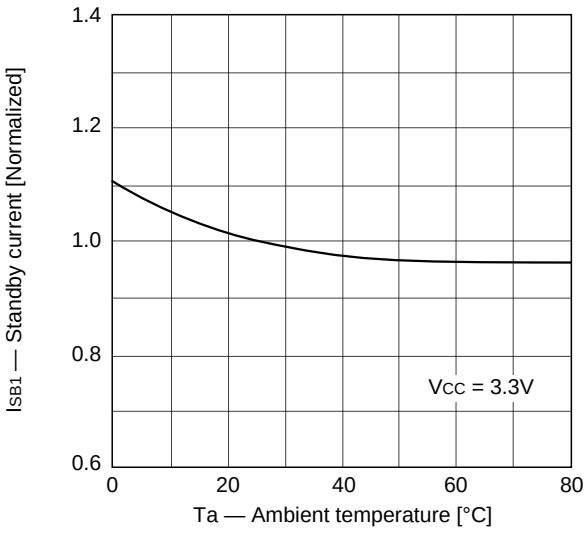
Access time vs. Load capacitance



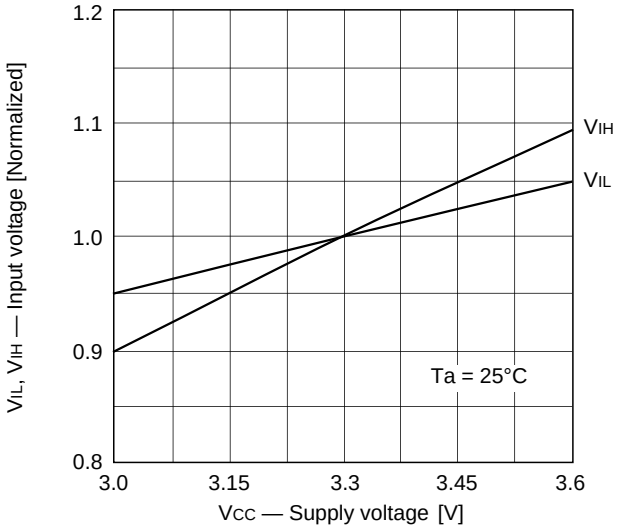
Standby current vs. Supply voltage



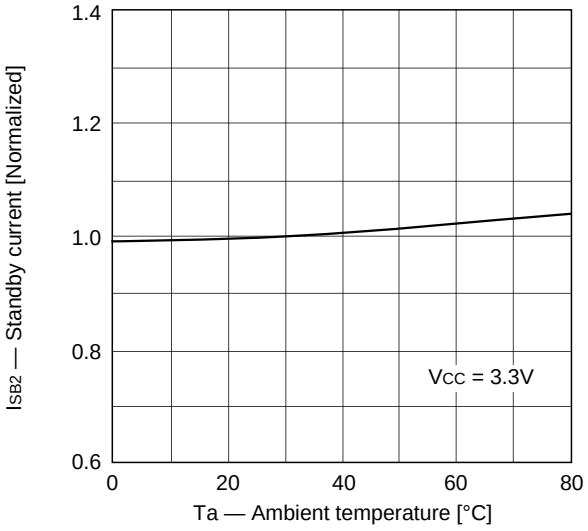
Standby current vs. Ambient temperature



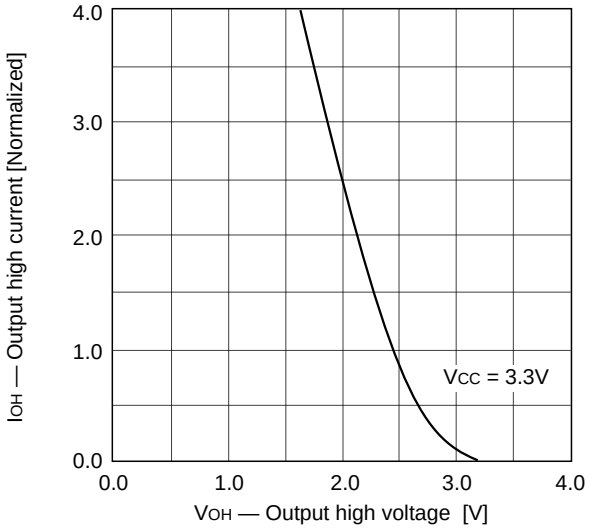
Input voltage level vs. Supply voltage



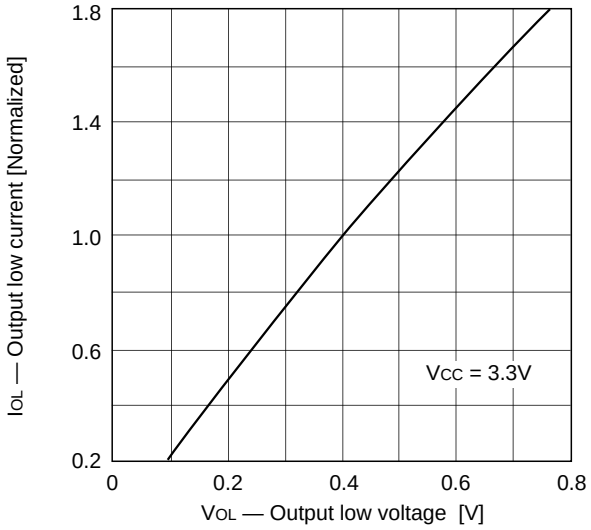
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



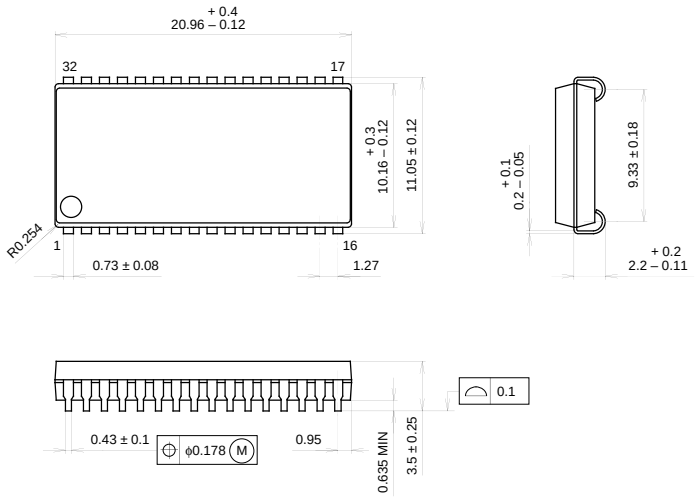
Output low current vs. Output low voltage



Package Outline Unit: mm

CXK5B81020J

32PIN SOJ (PLASTIC) 400mil



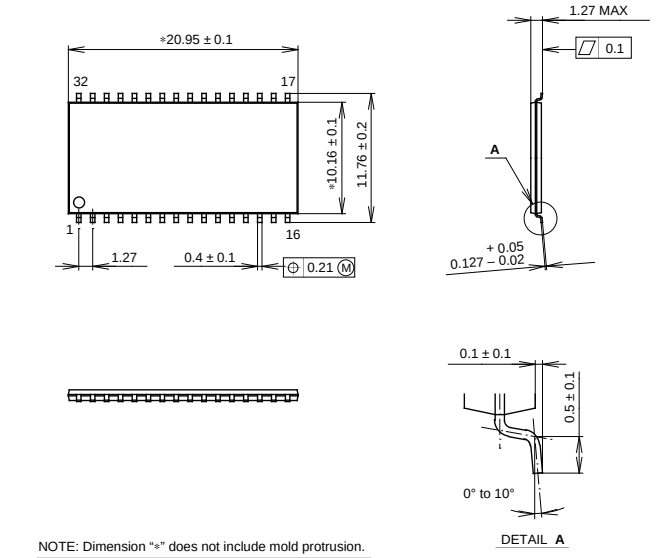
PACKAGE STRUCTURE

SONY CODE	SOJ-32P-01
EIAJ CODE	*SOJ032-P-0400-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE WEIGHT	1.3g

CXK5B81020TM

32PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -32P-L01
EIAJ CODE	TSOP (II) 032-P-0400-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————