

32768-word × 8-bit High Speed CMOS Static RAM Preliminary

Description

The CXK5T8257BTM/BYM/BM is 262,144 bits high speed CMOS static RAM organized as 32768-words by 8 bits.

Special feature are low power consumption and high speed.

The CXK5T8257BTM/BYM/BM is a suitable RAM for portable equipment with battery back up.

Features

- Extended operating temperature range: -25 to +85°C
- Wide supply voltage range operation: 2.7 to 3.6V
- Fast access time: (Access time)

3.0V operation	-10LLX	100ns (Max.)
	-12LLX	120ns (Max.)
3.3V operation	-10LLX	85ns (Max.)
	-12LLX	100ns (Max.)
- Low standby current: 7.0µA (Max.)
- Low power data retention: 2.0V (Min.)
- Available in many packages

CXK5T8257BTM/BYM

8mm × 13.4mm 28 pin TSOP Package

CXK5T8257BM

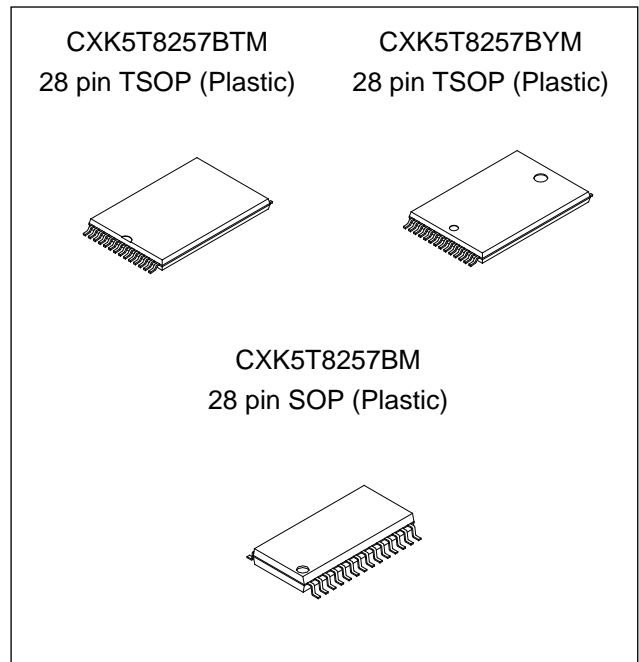
450mil 28 pin SOP Package

Function

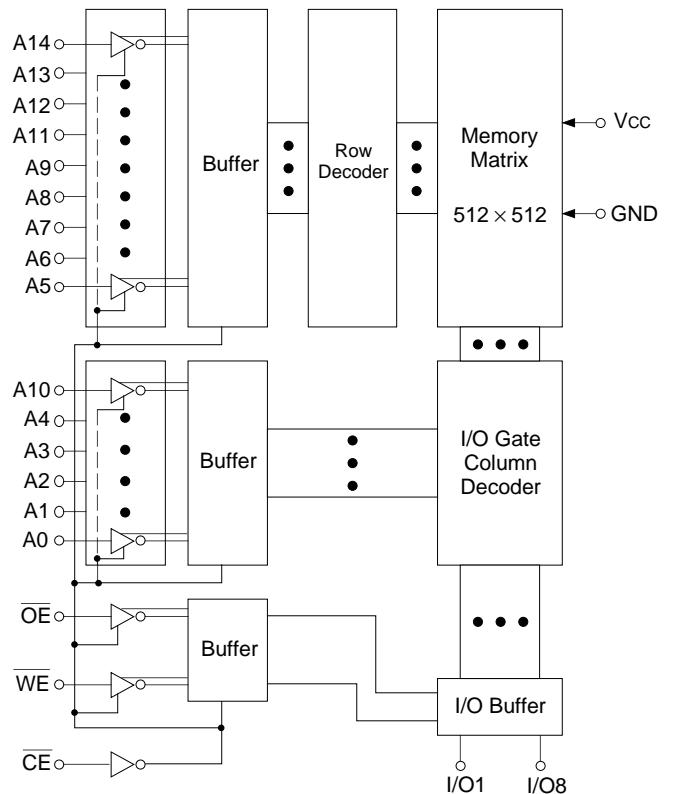
32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

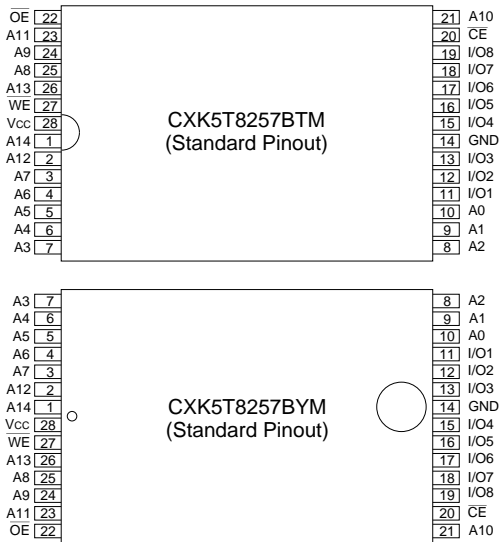


Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +4.6	V
Input voltage	V _{IN}	-0.5*1 to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5*1 to V _{CC} + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature · time	T _{solder}	235 · 10	°C · s

*1 V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	×	L	Write	Data in	I _{CC1} , I _{CC2}

x: "H" or "L"

DC Recommended Operating Conditions

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Vcc = 2.7 to 3.6V			Vcc = 3.3V ± 0.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	2.7	3.3	3.6	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.4	—	Vcc + 0.3	2.2	—	Vcc + 0.3	
Input low voltage	V _{IL}	-0.3*1	—	0.4	-0.3*1	—	0.6	

*1 V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• **DC characteristics**

(Vcc = 2.7 to 3.6V, GND = 0V, Ta = -25 to +85°C)

Item	Symbol	Test Conditions	Min.	Typ.*2	Max.	Unit	
Input leakage current	I _{LI}	V _{IN} = GND to Vcc	-0.5	—	0.5	μA	
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ OE = V _{IH} or $\overline{WE} = V_{IL}$ V _{I/O} = GND to Vcc	-0.5	—	0.5		
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$ V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA	—	0.9	2	mA	
Average operating current	I _{CC2}	Min. cycle duty = 100%, I _{OUT} = 0mA					
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	-25 to +85°C	—	—	7.0	μA
			-25 to +70°C	—	—	3.5	
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.06	0.7	mA	
Output high voltage	V _{OH}	I _{OH} = -2mA	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.0mA	—	—	0.4		

*2 Vcc = 3.3V, Ta = 25°C

*3 I_{CC2} = 21mA for 3.3V operation (Vcc = 3.3V ± 0.3V)

*4 I_{CC3} = 40mA for 3.3V operation (Vcc = 3.3V ± 0.3V)

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

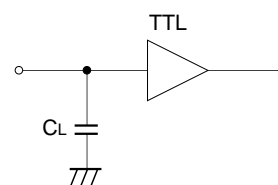
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions**

(Ta = -25 to +85°C)

Item	Conditions		
	V _{CC} = 2.7 to 3.6V	V _{CC} = 3.3V ± 0.3V	
Input pulse high level	V _{IH} = 2.4V	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.4V	V _{IL} = 0.6V	
Input rise time	t _r = 5ns	t _r = 5ns	
Input fall time	t _f = 5ns	t _f = 5ns	
Input and output reference level	1.4V	1.4V	
Output load conditions	-10LLX	C _L *1 = 100pF, 1TTL	C _L *1 = 30pF, 1TTL
	-12LLX	C _L *1 = 100pF, 1TTL	C _L *1 = 100pF, 1TTL



*1 C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	V _{CC} = 2.7 to 3.6V				V _{CC} = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	85	—	100	—	ns
Address access time	t _{AA}	—	100	—	120	—	85	—	100	
Chip enable access time (\overline{CE})	t _{CO}	—	100	—	120	—	85	—	100	
Chip enable to output valid	t _{OE}	—	50	—	60	—	50	—	50	
Chip hold from address change	t _{OH}	20	—	20	—	20	—	20	—	
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	10	—	10	—	
Output enable to output in low Z (\overline{OE})	t _{OLZ}	10	—	10	—	10	—	10	—	
Chip disable to output in high Z (\overline{CE})	t _{HZ} *1	—	35	—	40	—	35	—	35	
Output disable to output in high Z (\overline{OE})	t _{OHZ} *1	—	35	—	35	—	35	—	35	

*1 t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

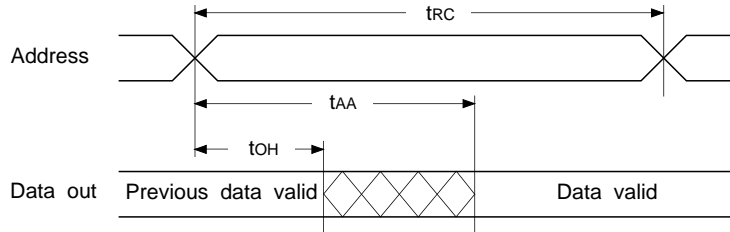
• Write cycle

Item	Symbol	V _{CC} = 2.7 to 3.6V				V _{CC} = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	85	—	100	—	ns
Address valid to end of write	t _{AW}	80	—	100	—	80	—	80	—	
Chip enable to end of write	t _{CW}	80	—	100	—	80	—	80	—	
Data to write time overlap	t _{DW}	35	—	50	—	35	—	35	—	
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	
Write pulse width	t _{WP}	60	—	70	—	60	—	60	—	
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	0	—	
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	
Write to output in high Z	t _{WHZ} *2	—	35	—	40	—	35	—	35	

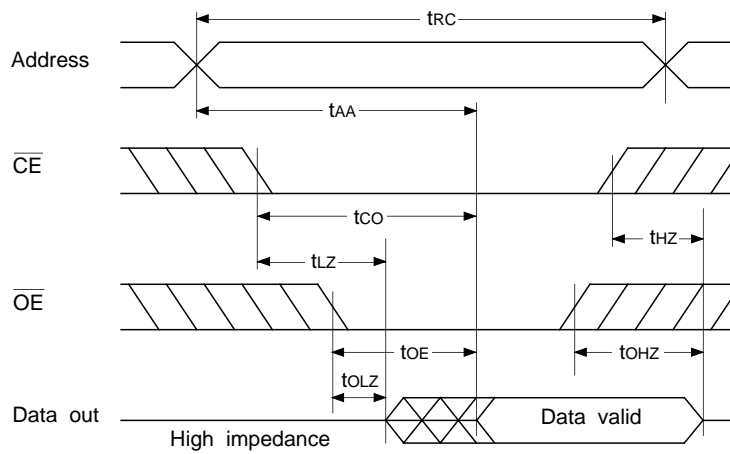
*2 t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing waveform

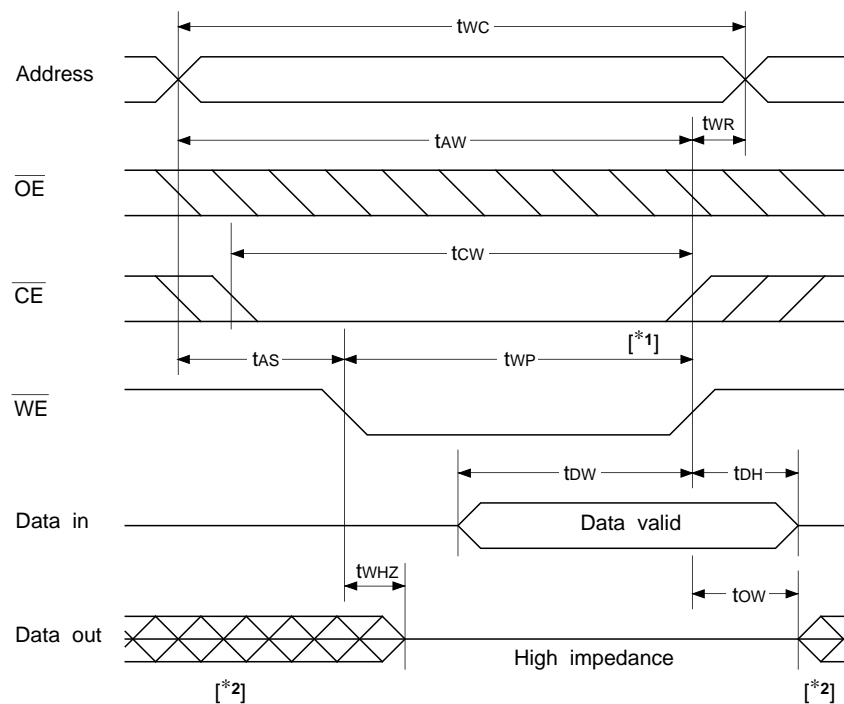
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$



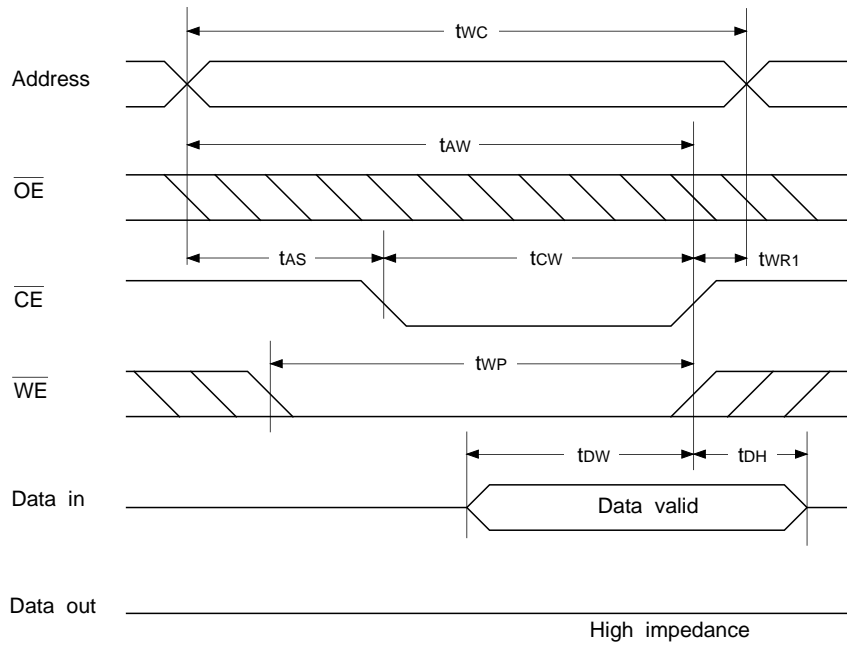
- Read cycle (2): $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2): \overline{CE} control

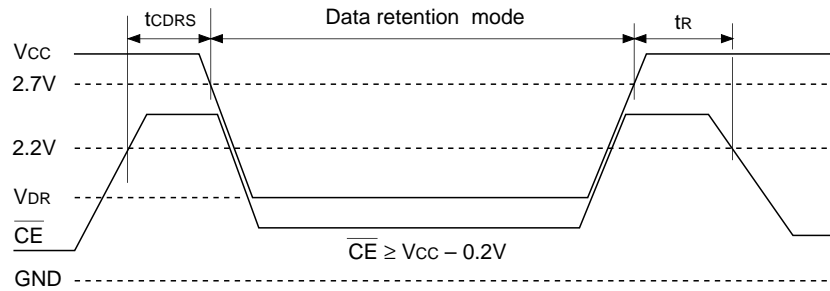


*1 Write is executed when both \overline{CE} and \overline{WE} are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is output condition.

Data Retention Waveform

- Low supply voltage data retention waveform



Data Retention Characteristics

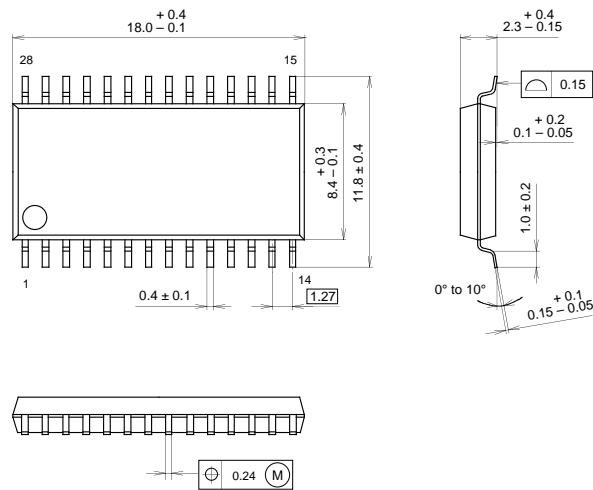
(Ta = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2	—	3.6	V	
Data retention current	I _{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	-25 to +85°C	—	—	6	μA
			-25 to +70°C	—	—	3	
			+25°C	—	0.1	—	
	I _{CCDR2}	$V_{CC} = 2.0 \text{ to } 3.6V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.12*1	7.0		
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t _R		5	—	—	ms	

*1 V_{CC} = 3.3V, Ta = 25°C

CXK5T8257BM

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L05
EIAJ CODE	+SOP028-P-0450
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g