

CXK5V16100TM -85LLX/10LLX

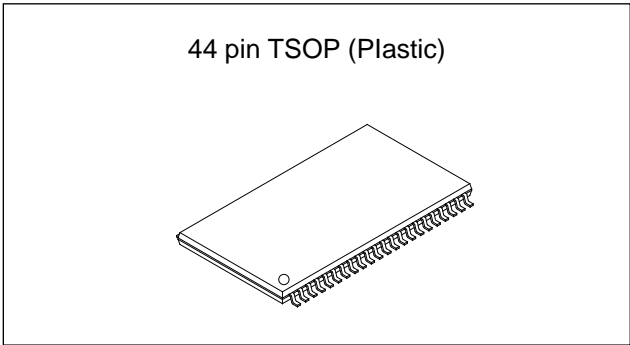
65536-word × 16-bit High Speed CMOS Static RAM

Description

CXK5V16100TM is a general purpose high speed CMOS static RAM organized as 65536-words by 16-bits. Operating on a single 3.3V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Extended operating temperature range: -25 to +85°C
- Fast access time: (Access time)
 - 85LLX 85ns (max.)
 - 10LLX 100ns (max.)
- Low power consumption operation:
 - Standby / DC operation
 - 1.7μW (typ.) / 3.3mW (typ.)
- Single 3.3V supply: 3.3V±0.3V
- Fully static memory: No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly LVTTTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (min.)
- 400mil 44pin TSOP (type II) package



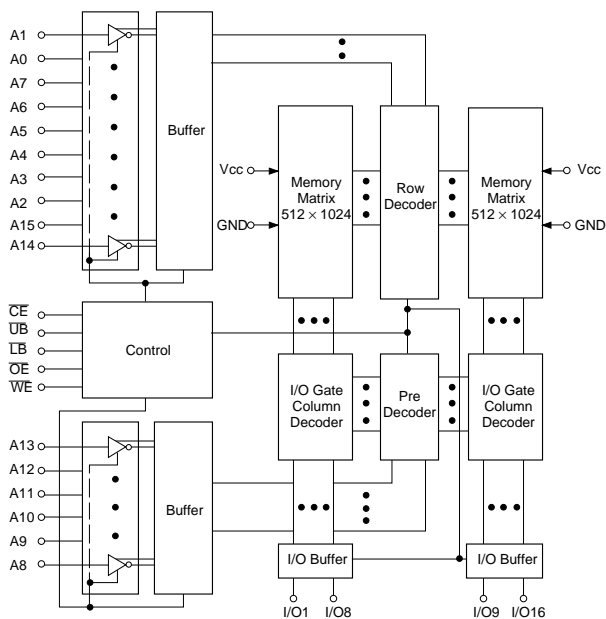
Function

65536-word × 16-bit static RAM

Structure

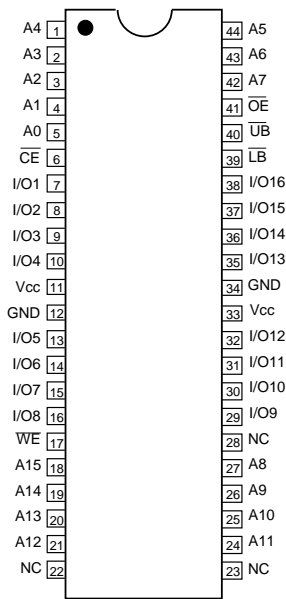
Silicon gate CMOS IC

Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O16	Data input/output
\overline{CE}	Chip enable input
\overline{LB}	Byte enable input (I/O1 to I/O8)
\overline{UB}	Byte enable input (I/O9 to I/O16)
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+3.3V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Input voltage	V _{IN}	-0.5* to Vcc + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • s

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 to I/O8	I/O9 to I/O16	Vcc Current
H	×	×	×	×	Not selected	Not selected	I _{SB1} , I _{SB2}
L	L	H	L	L	Read	Read	I _{CC1} , I _{CC2} , I _{CC3}
			L	H	Read	High-Z	I _{CC1} , I _{CC2} , I _{CC3}
			H	L	High-Z	Read	I _{CC1} , I _{CC2} , I _{CC3}
L	×	L	L	L	Write	Write	I _{CC1} , I _{CC2} , I _{CC3}
			L	H	Write	Not Write/Hi-Z	I _{CC1} , I _{CC2} , I _{CC3}
			H	L	Not Write/Hi-Z	Write	I _{CC1} , I _{CC2} , I _{CC3}
L	H	H	×	×	High-Z	High-Z	I _{CC1} , I _{CC2} , I _{CC3}
L	×	×	H	H	High-Z	High-Z	I _{CC1} , I _{CC2} , I _{CC3}

×: "H" or "L"

DC Recommended Operating Conditions ($T_a = -25$ to $+85^\circ\text{C}$, $\text{GND} = 0\text{V}$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3^*	—	0.8	V

* $V_{IL} = -3.0\text{V}$ Min. for pulse width less than 50ns.

Electrical Characteristics**DC and operating characteristics**($V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $\text{GND} = 0\text{V}$, $T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test condition	Min.	Typ.*	Max.	Unit	
Input leakage current	I_{LI}	$V_{IN} = \text{GND to } V_{CC}$	-1	—	1	μA	
Output leakage current	I_{LO}	$\overline{CE} = V_{IH}$ or $\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{IO} = \text{GND to } V_{CC}$	-1	—	1	μA	
Operating power supply current	I_{CC1}	$\overline{CE} = V_{IL}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} = 0\text{mA}$	—	1	3	mA	
Average operating current	I_{CC2}	Min. cycle Duty = 100% $I_{OUT} = 0\text{mA}$	85LLX	—	40	55	mA
			10LLX	—	35	50	
	I_{CC3}	Cycle time 1 μs Duty = 100% $I_{OUT} = 0\text{mA}$ $\overline{CE} \leq 0.2\text{V}$ $V_{IL} \leq 0.2\text{V}$ $V_{IH} \geq V_{CC} - 0.2\text{V}$	—	10	20	mA	
Standby current	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2\text{V}$	-25 to $+85^\circ\text{C}$	—	—	40	μA
			-25 to $+70^\circ\text{C}$	—	—	20	
			-25 to $+40^\circ\text{C}$	—	—	4	
			$+25^\circ\text{C}$	—	0.5	2	
	I_{SB2}	$\overline{CE} = V_{IH}$	—	0.03	0.6	mA	
Output high voltage	V_{OH}	$I_{OH} = -2.0\text{mA}$	2.4	—	—	V	
Output low voltage	V_{OL}	$I_{OL} = 2.0\text{mA}$	—	—	0.4	V	

* $V_{CC} = 3.3\text{V}$, $T_a = 25^\circ\text{C}$

I/O capacitance

(Ta = 25°C, f = 1MHz)

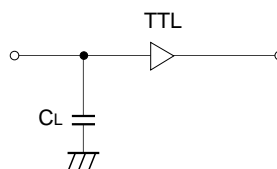
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (V_{CC} = 3.3V ± 0.3V, Ta = -25 to +85°C)

Item	Conditions	
Input pulse high level	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.6V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.4V	
Output load conditions	85ns	C _L * = 30pF, 1TTL
	100ns	C _L * = 100pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	85	—	100	—	ns
Address access time	t _{AA}	—	85	—	100	ns
Chip enable access time (\overline{CE})	t _{CO}	—	85	—	100	ns
Byte enable access time ($\overline{UB}, \overline{LB}$)	t _{BO}	—	40	—	50	ns
Output enable to output valid	t _{OE}	—	40	—	50	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	ns
Byte enable to output in low Z ($\overline{UB}, \overline{LB}$)	t _{BLZ}	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	—	35	—	40	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	—	30	—	35	ns
Byte disable to output in high Z ($\overline{UB}, \overline{LB}$)	t _{BHZ} *	—	30	—	35	ns

* t_{HZ}, t_{OHZ} and t_{BHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

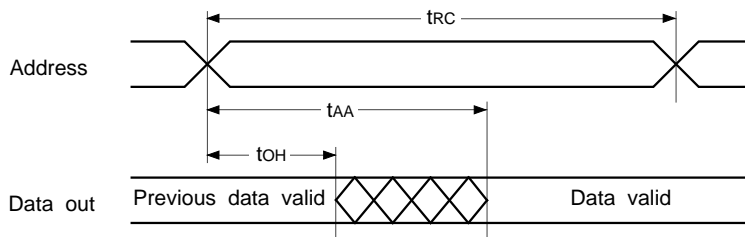
• Write cycle

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	85	—	100	—	ns
Address valid to end of write	t _{AW}	70	—	80	—	ns
Chip enable to end of write	t _{CW}	70	—	80	—	ns
Byte enable to end of write	t _{BW}	70	—	80	—	ns
Data to write time overlap	t _{DW}	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	ns
Write recovery time ($\overline{CE}, \overline{UB}, \overline{LB}$)	t _{WR1}	5	—	5	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	—	35	—	40	ns

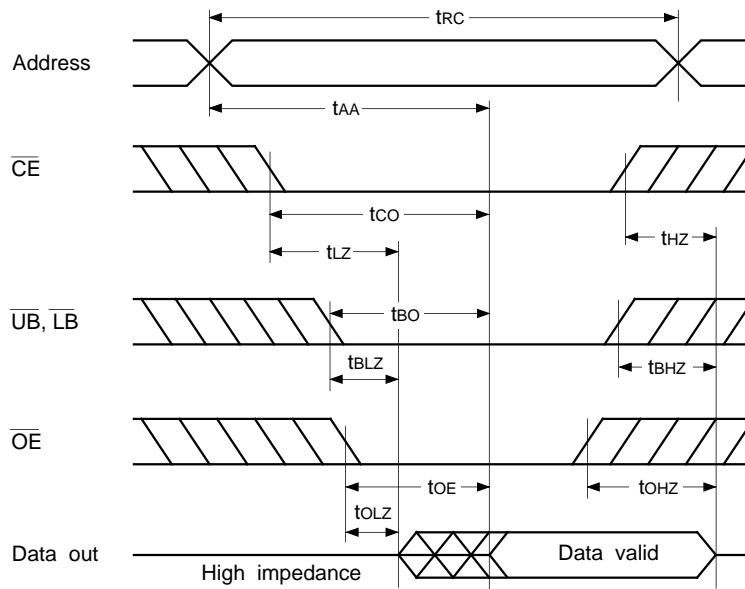
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage levels.

Timing Waveform

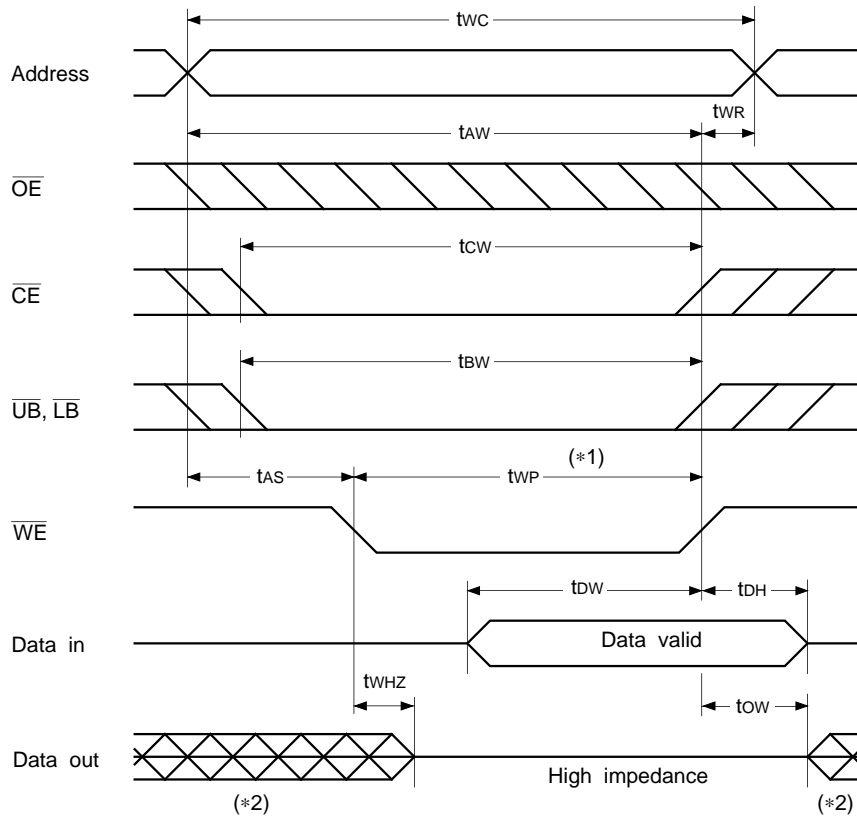
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} and, or $\overline{LB} = V_{IL}$



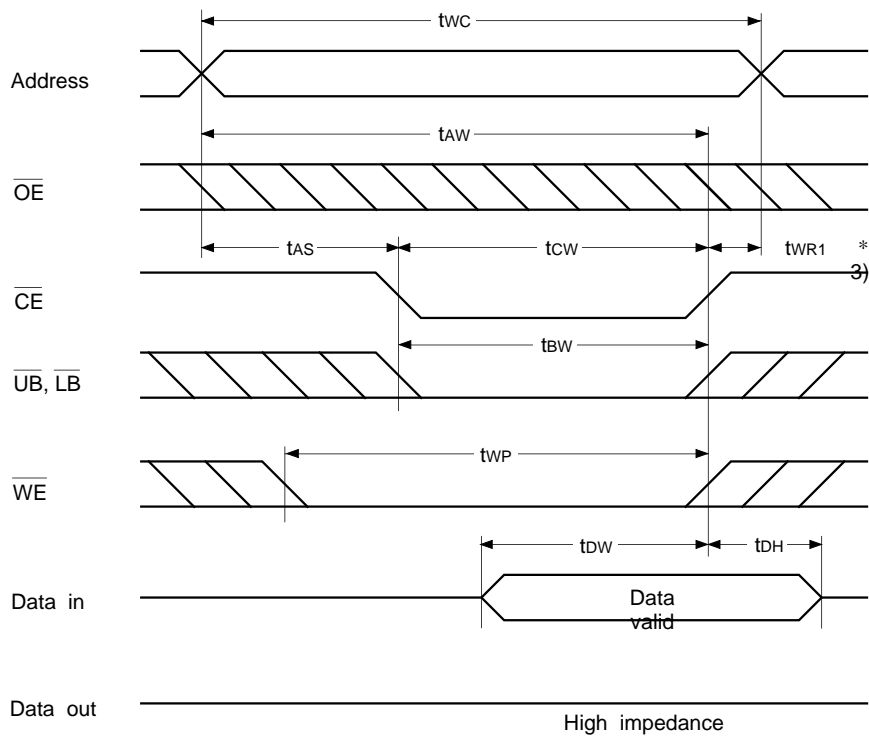
- Read cycle (2) : $\overline{WE} = V_{IH}$



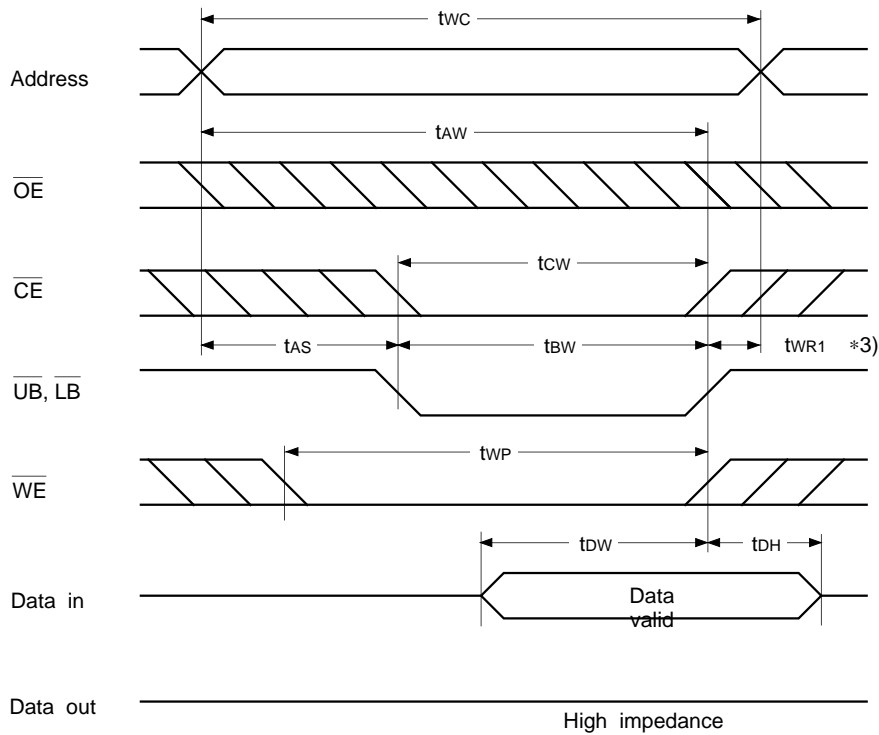
• Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



• Write cycle (3) : \overline{UB} , \overline{LB} control



*1 Write is executed when all of the \overline{CE} , \overline{WE} and (\overline{UB} and, or \overline{LB}) are at low simultaneously.

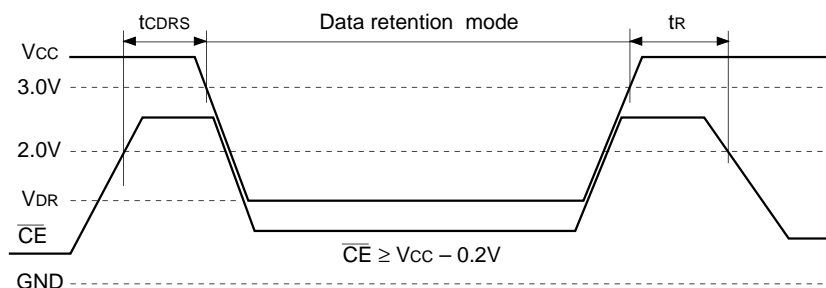
*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} (for I/O1 to 8) is tested from either the rising edge of \overline{CE} or \overline{LB} , whichever comes earlier, until the end of the write cycle.

t_{WR1} (for I/O9 to 16) is tested from either the rising edge of \overline{CE} or \overline{UB} , whichever comes earlier, until the end of the write cycle.

Data Retention Waveform

- Low supply voltage data retention waveform



Data Retention Characteristics

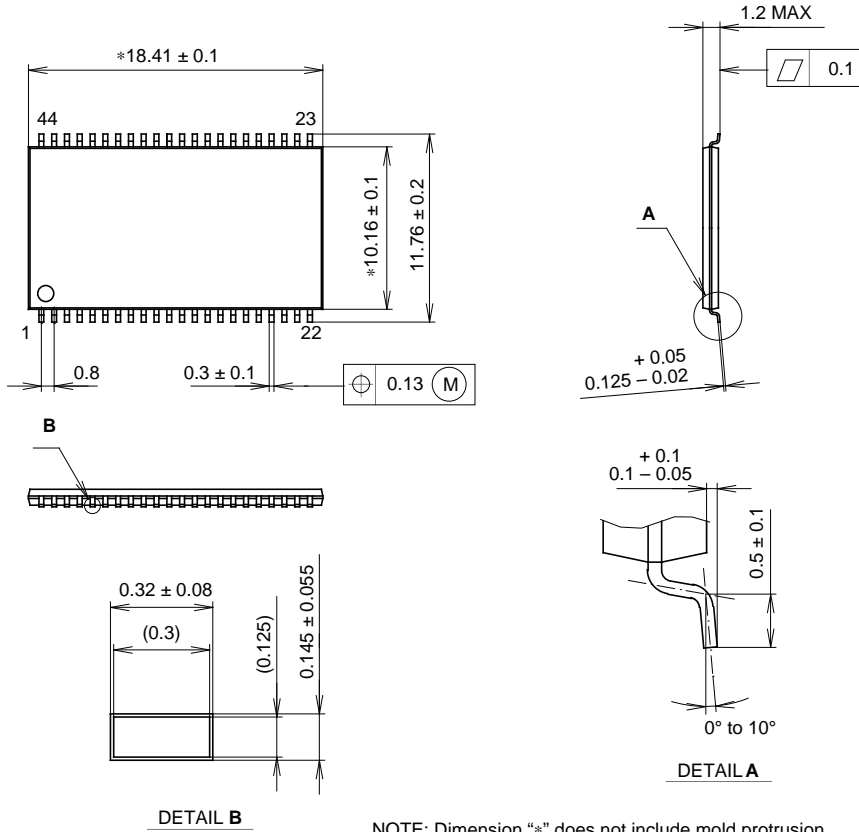
(Ta = -25 to +85°C)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	
Data retention voltage	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	3.6	V	
Data retention current	I _{CCDR1}	V _{CC} = 3.0V	-25 to +85°C	—	—	24	μA
			-25 to +70°C	—	—	12	
			-25 to +40°C	—	—	2.4	
			+25°C	—	0.4	1.2	
	I _{CCDR2}	V _{CC} = 2.0 to 3.6V	—	0.5*	40	μA	
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t _R		5	—	—	ms	

* V_{CC} = 3.3V, Ta = 25°C

Package Outline Unit: mm

44PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01
EIAJ CODE	TSOP (II) 044-P-0400-A
JEDEC CODE	_____

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g