SONY

# CXL1501M

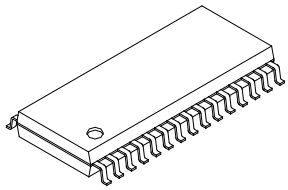
## CMOS-CCD Signal Processor

**For the availability of this product, please contact the sales office.**

### Description

The CXL1501M is a CMOS-CCD signal processor designed for 8-mm VCR video signal processing. In combination with the 8-mm VCR video Y/C signal processing IC CXA1200Q, this IC configures a comb filter for Y/C separation in recording an image and elimination of crosstalk in playing back.

30 pin SOP (Plastic)



### Features

- Single power supply 5V
- Low power consumption 225mW (Typ.)
- Built-in peripheral circuits
- Completely adjustment free
- Built-in quadruple progression PLL circuit
- For NTSC signals

### Functions

- 1H comb filter output
- Dropout compensation (D.O.C) output
- Delay time matching through output (THR)
- PLL circuit (quadruple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit

### Structure

CMOS-CCD

### Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 6 | V |
| • Operating temperature | Topr | –10 to +60 | °C |
| • Storage temperature | Tstg | –55 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 500 | mW |

### Recommended Operating Conditions (Ta = 25°C)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 5 ± 5% | V |

### Recommended Clock Conditions (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Input clock amplitude | $V_{CLK}$ | 0.4 to 1.0 (0.5Vp-p Typ.) | Vp-p |
| • Clock frequency | $f_{CLK}$ | 3.579545 | MHz |
| • Input clock waveform | sine wave | | |

### Input Signal Amplitude

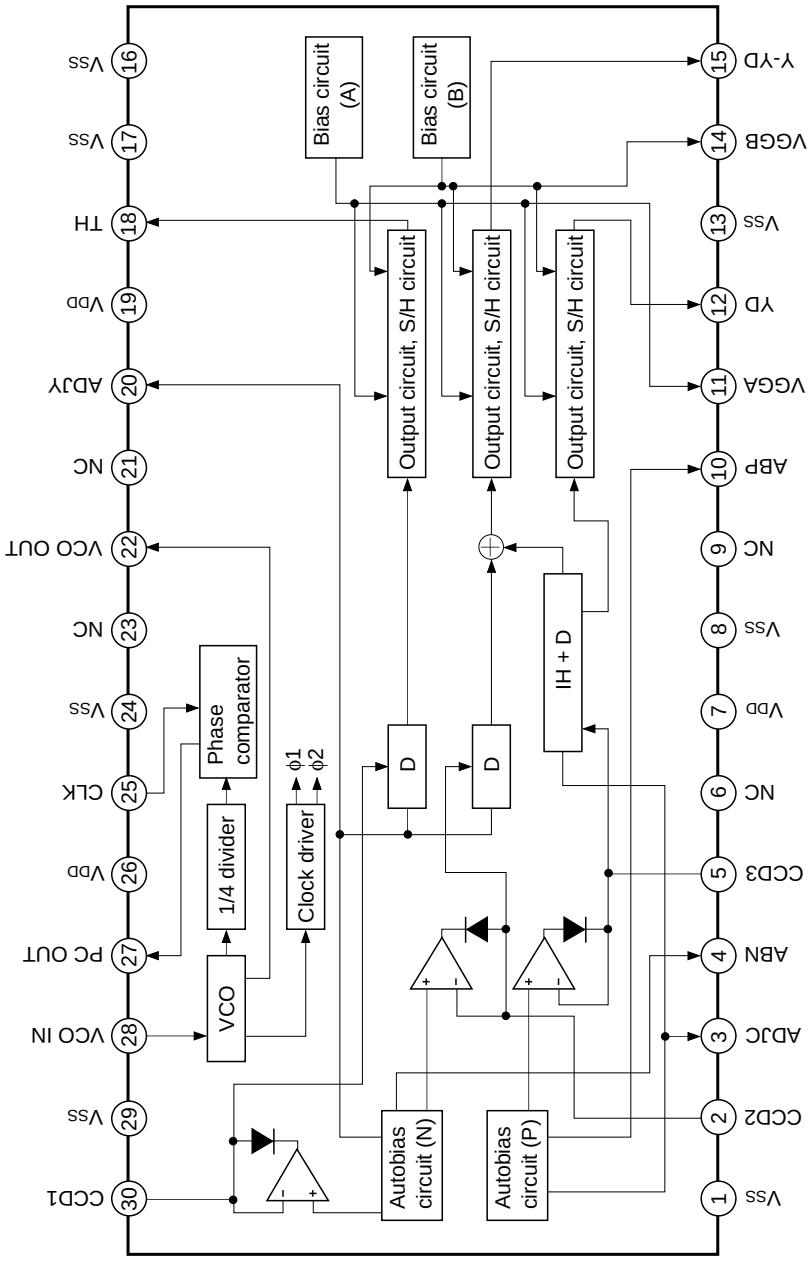
| | | | |
|---|---|---|---|
| | $V_{SIG}$ | 571 (Max.) | mVp-p |





E71050-PS

**Block Diagram and Pin Configuration (Top View)**



**Pin Description**

| Pin No. | Symbol | I/O | Description | Impedance (Ω) |
|---|---|---|---|---|
| 1 | $V_{SS}$ | — | GND | |
| 2 | CCD2 | I | Signal input 2 (Reverse phase signal) | > 100k (at no clamp) |
| 3 | ADJC | O | Forward phase CCD bias DC output | 600 to 2k |
| 4 | ABN | O | Reverse phase autobias DC output | 2k to 20k |
| 5 | CCD3 | I | Signal input 3 (Forward phase signal) | > 100k (at no clamp) |
| 6 | NC | — | | |
| 7 | $V_{DD}$ | — | 5V power supply (For clock driver) | |
| 8 | $V_{SS}$ | — | GND | |
| 9 | NC | — | | |
| 10 | ABP | O | Forward phase autobias DC output | 2k to 20k |
| 11 | VGGA | O | Gate bias (A) DC output | 2k to 10k |
| 12 | YD | O | D.O.C signal output (Reverse phase signal) | 40 to 500 |
| 13 | $V_{SS}$ | — | GND | |
| 14 | VGGB | O | Gate bias (B) DC output | 2k to 10k |
| 15 | Y-YD | O | Comb filter signal output | 40 to 500 |
| 16 | $V_{SS}$ | — | GND | |
| 17 | $V_{SS}$ | — | GND | |
| 18 | TH | O | THR signal output (Forward phase signal) | 40 to 500 |
| 19 | $V_{DD}$ | — | 5V power supply (For analog) | |
| 20 | ADJY | O | Reverse phase CCD bias DC output | 600 to 2k |
| 21 | NC | — | | |
| 22 | VCO OUT | O | VCO output | |
| 23 | NC | — | | |
| 24 | $V_{SS}$ | — | GND | |
| 25 | CLK | I | Clock input | 4k to 40k |
| 26 | $V_{DD}$ | — | 5V power supply (For digital) | |
| 27 | PC OUT | O | Phase comparator output | 2k to 5k |
| 28 | VCO IN | I | VCO input | > 100k |
| 29 | $V_{SS}$ | — | GND | |
| 30 | CCD1 | I | Signal input 1 (Reverse phase signal) | > 100k (at no clamp) |

## Electrical Characteristics

(Ta = 25°C, $V_{DD}$ = 5V, $f_{CLK}$ = 3.579545MHz, $V_{CLK}$ = 500mVp-p sine wave)
See the Electrical Characteristics Test Circuit.

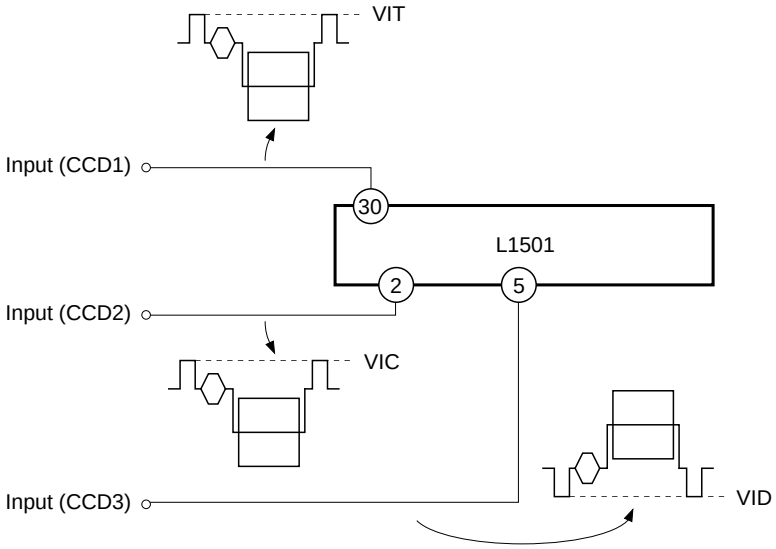
| Item | Symbol | Test conditions*1 | SW conditions | | | | | | | | | Bias conditions*2 (V) | | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | $V_{BIAS}1$ | $V_{BIAS}2$ | $V_{BIAS}3$ | | | | | |
| Supply current | $I_{DD}$ | — | a | a | a | a | a | a | a | — | — | — | — | — | 35 | 45 | 55 | mA | *3 |
| Low frequency gain | GLT | 196.678kHz 500mVp-p sine wave | a | a | a | a | a | a | a | a | b | — | — | — | –5.0 | –3.0 | –1.0 | dB | *4 |
| | GLC | | a | a | a | a | a | a | a | b | b | | | | | | | | |
| | GLD | | a | a | a | a | a | a | a | c | b | | | | | | | | |
| High frequency gain | GHT | 3.579545MHz 150mVp-p sine wave | c | a | a | a | b | b | b | a | b | VIT –0.25 | VIC –0.25 | VID +0.25 | –6.5 | –4.5 | –2.5 | dB | *5 |
| | GHC | | c | a | a | a | b | b | b | b | b | | | | | | | | |
| | GHD | | c | a | a | a | b | b | b | c | b | | | | | | | | |
| Frequency response | fT | 196.678kHz ↔3.579545MHz 150mVp-p sine wave | b↔c | a | a | a | b | b | b | a | b | VIT –0.25 | VIC –0.25 | VID +0.25 | –2.5 | –1.5 | –0.5 | dB | *6 |
| | fc | | b↔c | a | a | a | b | b | b | b | b | | | | | | | | |
| | fD | | b↔c | a | a | a | b | b | b | c | b | | | | | | | | |
| Differential gain | DGT | 5-staircase wave*7 | f | a | a | a | a | a | a | a | c | — | — | — | 0 | 3 | 7 | % | *7 |
| | DGC | | f | a | a | a | a | a | a | b | c | | | | | | | | |
| | DGD | | f | a | a | a | a | a | a | c | c | | | | | | | | |
| Differential phase | DPT | 5-staircase wave*7 | f | a | a | a | a | a | a | a | c | — | — | — | 0 | 3 | 7 | degree | *7 |
| | DPC | | f | a | a | a | a | a | a | b | c | | | | | | | | |
| | DPD | | f | a | a | a | a | a | a | c | c | | | | | | | | |
| S/H pulse coupling | VPT | No-signal input | — | b | b | b | b | b | b | a | a | VIT | VIC | VID +0.5 | — | — | 350 | mVp-p | *8 |
| | VPC | | — | b | b | b | b | b | b | b | a | | | | | | | | |
| | VPD | | — | b | b | b | b | b | b | c | a | | | | | | | | |
| S/N ratio | SNT | No-signal input*9 | — | b | b | b | a | a | a | a | d | — | — | — | — | –56 | –52 | dB | *9 |
| | SNC | | — | b | b | b | a | a | a | b | d | | | | | | | | |
| | SND | | — | b | b | b | a | a | a | c | d | | | | | | | | |

| Item | Symbol | Test conditions*1 | SW conditions | | | | | | | | | Bias conditions*2 (V) | | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | $V_{BIAS}1$ | $V_{BIAS}2$ | $V_{BIAS}3$ | | | | | |
| Chroma comb depth min. gain | C-CD | 3.579545MHz 200mVp-p sine wave ↔ 3.587412MHz 200mVp-p sine wave | d↔e | a | a | a | b | b | b | b | b | *10 | *10 | *10 | — | — | –27 | dB | *10 |

**Notes)**

*1 Adjust the output amplitude of the inversion and the non-inversion amplifiers in the signal input block to an equal value, as well as the phase difference to a precise 180°.
Also set the clock and input signal frequency accurately.

*2 VIT, VIC and VID are defined as follows:
VIT, VIC and VID are input signal clamp levels. They clamps the Video signal sync tip level. They are the pin voltages at no-input signal for pins 30, 2 and 5, respectively.




Testing of VIT, VIC and VID is executed with a voltmeter under the following SW conditions:

| Item | SW conditions | | | | | | | | | | | Test point |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
| VIT | — | b | b | b | a | a | a | — | — | — | — | V1 |
| VIC | — | b | b | b | a | a | a | — | — | — | — | V2 |
| VID | — | b | b | b | a | a | a | — | — | — | — | V3 |

As VIT, VIC and VID differ with each IC, they are to be tested respectively.

*3 This is the IC supply current value during clock and signal input.

*4 GLT, GLC and GLD are output gains of TH, Y-YD, and YD pins when a 500mVp-p, 196.678kHz sine wave is simultaneously fed to CCD1, CCD2, and CCD3 pins respectively.

(Example of calculation)

$$GLT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

*5 GHT, GHC, and GHD are output gains of TH, Y-YD and YD pins when a 150mVp-p, 3.579545MHz sine wave is simultaneously fed to CCD1, CCD2, and CCD3 pins respectively.
Bias at input ($V_{BIAS}1$, $V_{BIAS}2$ and $V_{BIAS}3$) is tested respectively at VIT – 0.25V, VIC – 0.25V and VID + 0.25V.

(Example of calculation)

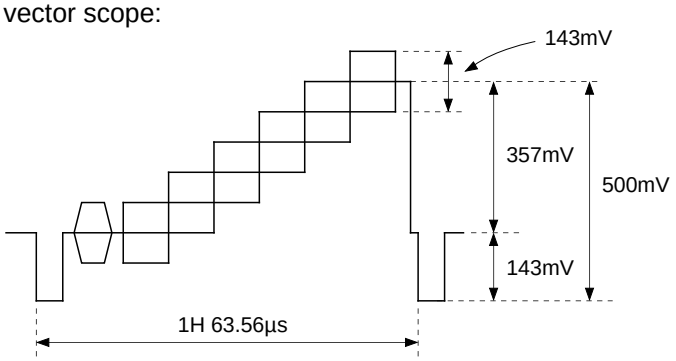
$$GHT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{\text{150 [mVp-p]}} \text{ [dB]}$$

*6 Indicates the dissipation at 3.579545MHz in relation to 196.678kHz. From the output voltage at TH, Y-YD and YD pins when a 150mVp-p, 196.678kHz sine wave is simultaneously fed to CCD1, CCD2 and CCD3 pins, and from the output voltage at TH, Y-YD and YD pins when a 150mVp-p, 3.579545MHz sine wave is simultaneously fed to same, calculation is made according to the following formula. The input block bias for $V_{BIAS}1$, $V_{BIAS}2$ and $V_{BIAS}3$ is tested at VIT – 0.25V, VIC – 0.25V and VID + 0.25V, respectively.

(Example of calculation)

$$fT = 20 \log \frac{\text{TH pin output voltage (3.579545MHz) [mVp-p]}}{\text{TH pin output voltage (196.678kHz) [mVp-p]}} \text{ [dB]}$$

*7 The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:




CCD3 pin input waveform (the input waveform of CCD1 and CCD2 pins is the inverted waveform of the figure above.)

*8 The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input block bias is tested at VITV, VICV, and VID + 0.5V.

*9 The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 4MHz. Vn [Vrms]

The signal component is determined either by testing the output voltage (the same test system as that of noise level) at input of 357mVp-p, 196.678kHz, or by performing calculation from the values of GLT, GLC, and GLD in accordance with the following formula. Vs [Vp-p]

(Example of Vs calculation)

$V_{S\text{-}T} = 0.357 \times 10^{\frac{GLT}{20}}$ ($V_{S\text{-}T}$: TH output voltage)

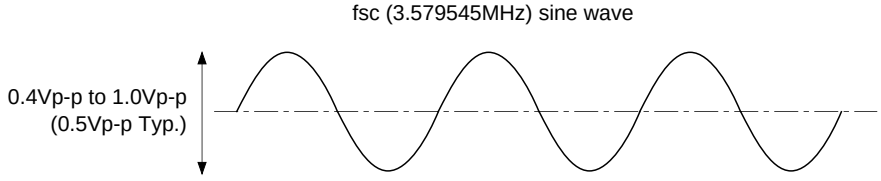
(Example of S/N ratio calculation)

$$SNT = 20 \log \frac{Vn\text{-}T \text{ (noise component) [Vrms]}}{V_{S\text{-}T} \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

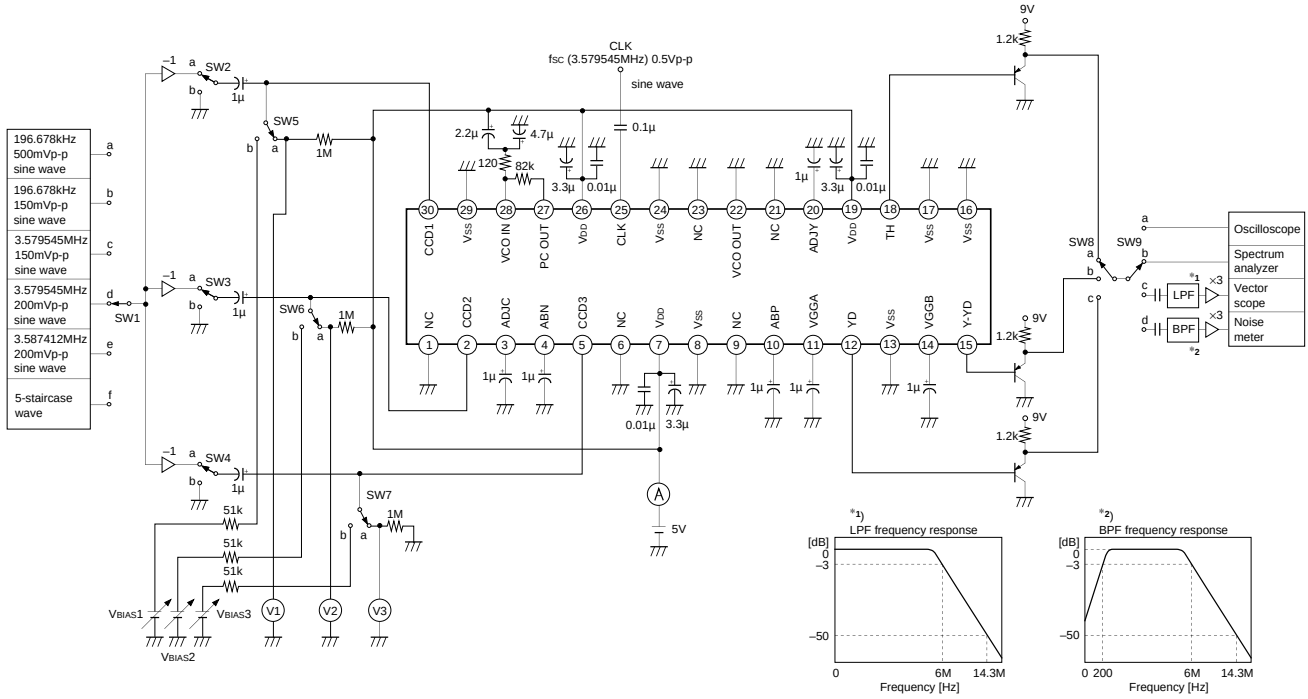
*10 C-CD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200mVp-p, 3.579545MHz sine wave is simultaneously fed to CCD1, CCD2 and CCD3 pins and from the Y-CD pin output voltage when a 200mVp-p, 3.587412MHz sine wave is simultaneously fed to same. The input block bias is set to VIT – 0.3V, VIC – 0.3V and VID + 0.3V, respectively.

$$C\text{-}CD = 20 \log \frac{\text{Y-YD pin output voltage (3.587412MHz) [mVp-p]}}{\text{Y-YD pin output voltage (3.579545MHz) [mVp-p]}} \text{ [dB]}$$

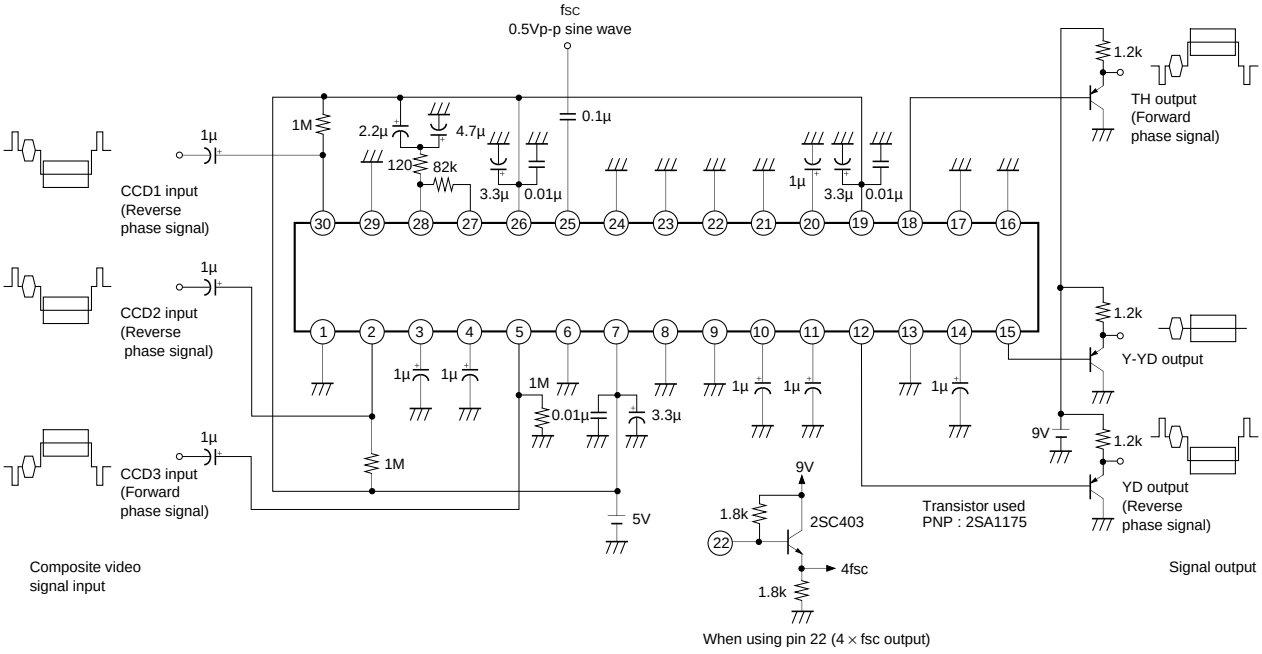
CLOCK



## Electrical Characteristics Test Circuit

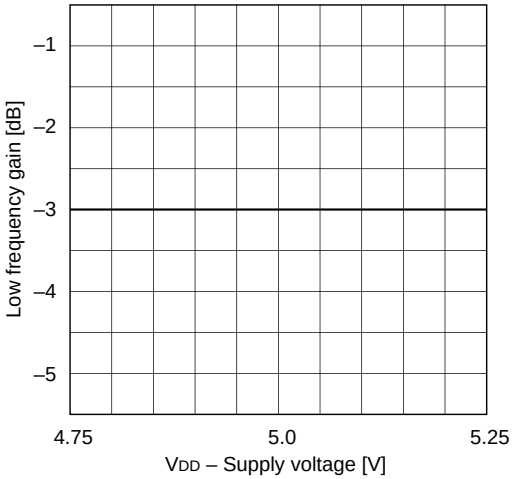



## Application Circuit

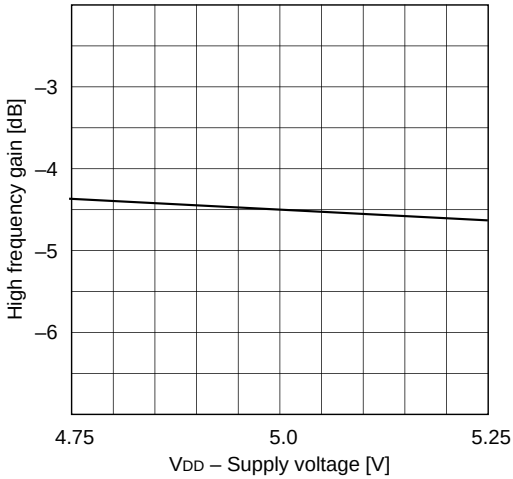



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

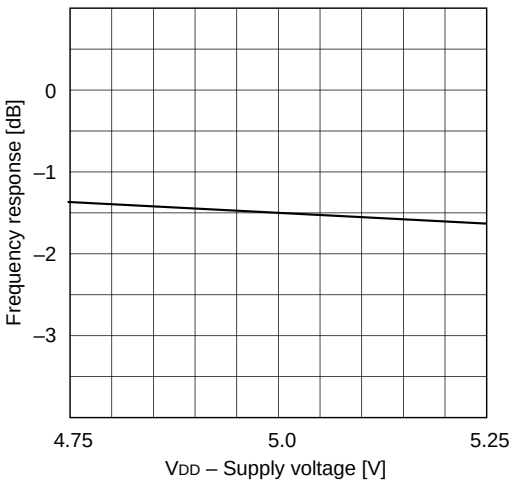
**Low frequency gain vs. Supply voltage**



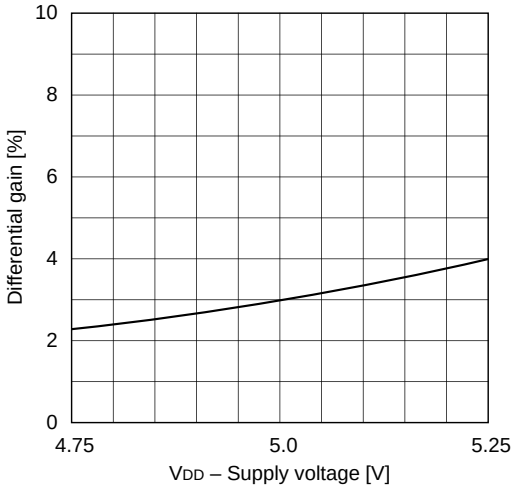

**High frequency gain vs. Supply voltage**



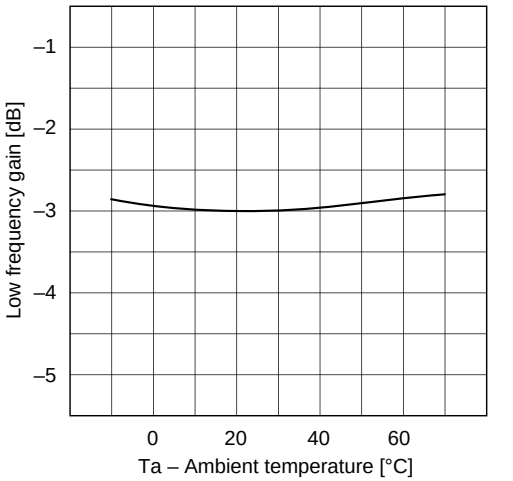

**Frequency response vs. Supply voltage**



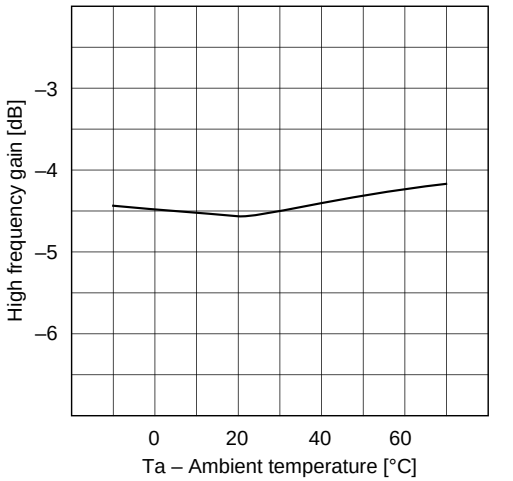

**Differential gain vs. Supply voltage**



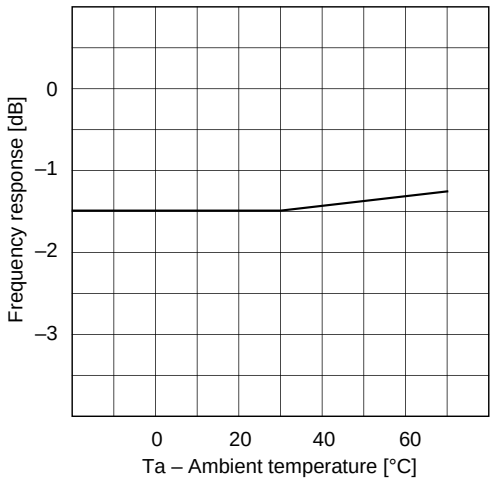

**Low frequency gain vs. Ambient temperature**



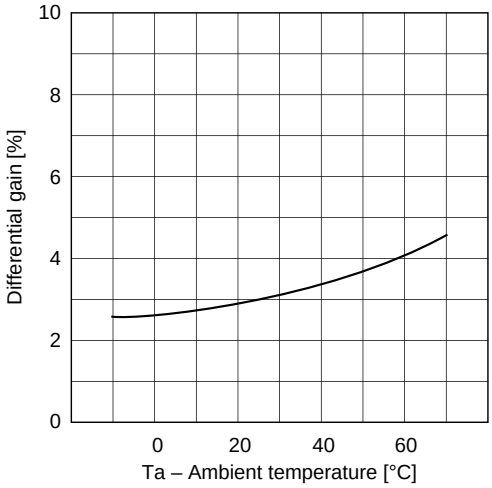

**High frequency gain vs. Ambient temperature**



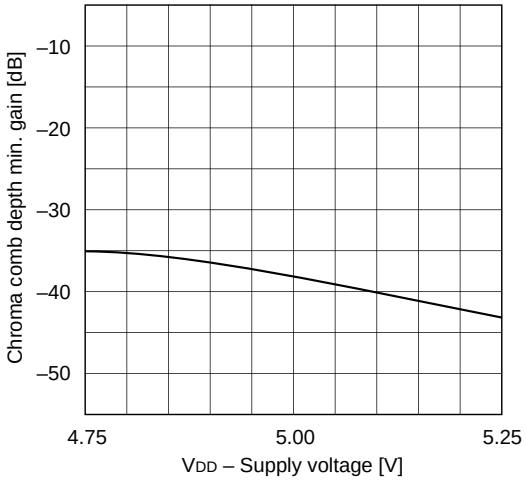
**Frequency response vs. Ambient temperature**



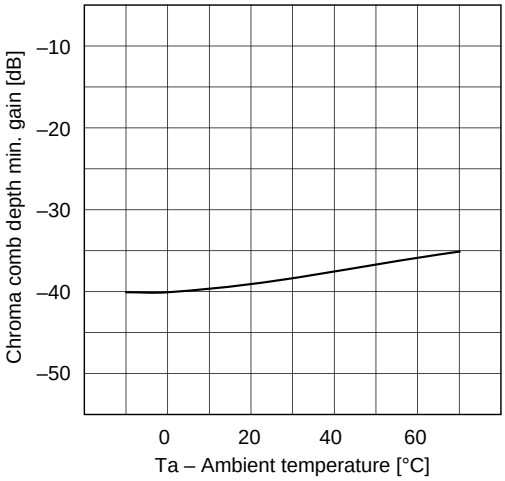

**Differential gain vs. Ambient temperature**



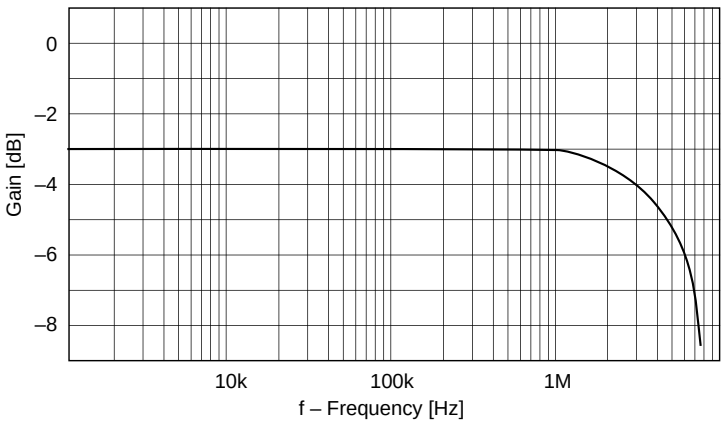

**Chroma comb depth min. gain vs. Supply voltage**



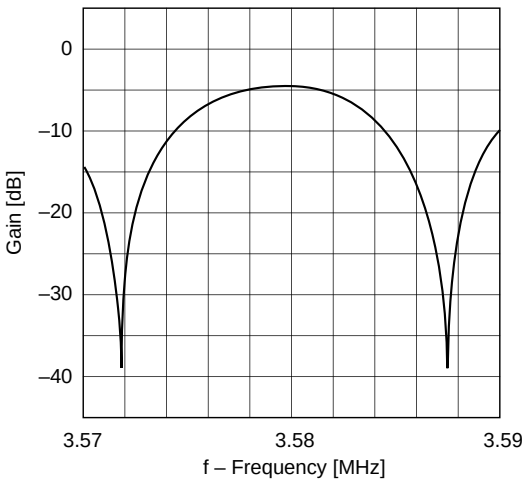

**Chroma comb depth min. gain vs. Ambient temperature**




**Frequency response (TH, YD Output)**

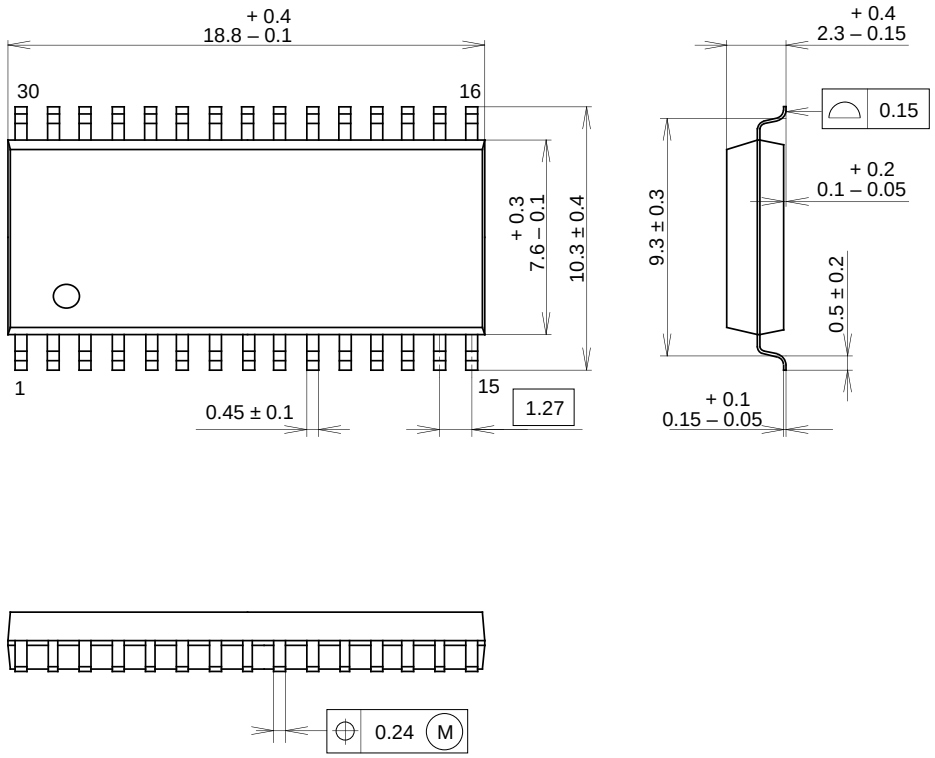



**Chroma comb response (Y-YD Output)**



**Package Outline** Unit: mm

30PIN SOP (PLASTIC)




| | |
|---|---|
| SONY CODE | SOP-30P-L01 |
| EIAJ CODE | SOP030-P-0375 |
| JEDEC CODE | ——— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 0.7g |