

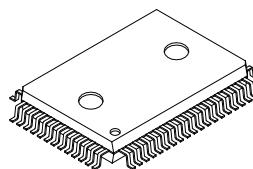
CMOS 8-bit Single Chip Microcomputer

Description

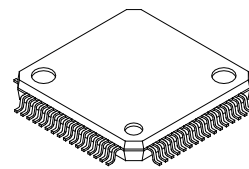
The CXP81120/81124 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, PWM output, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP81120/81124 provides power-on reset function, sleep/stop function which enables to lower power consumption.

64 pin QFP (Plastic)



64 pin LQFP (Plastic)



Features

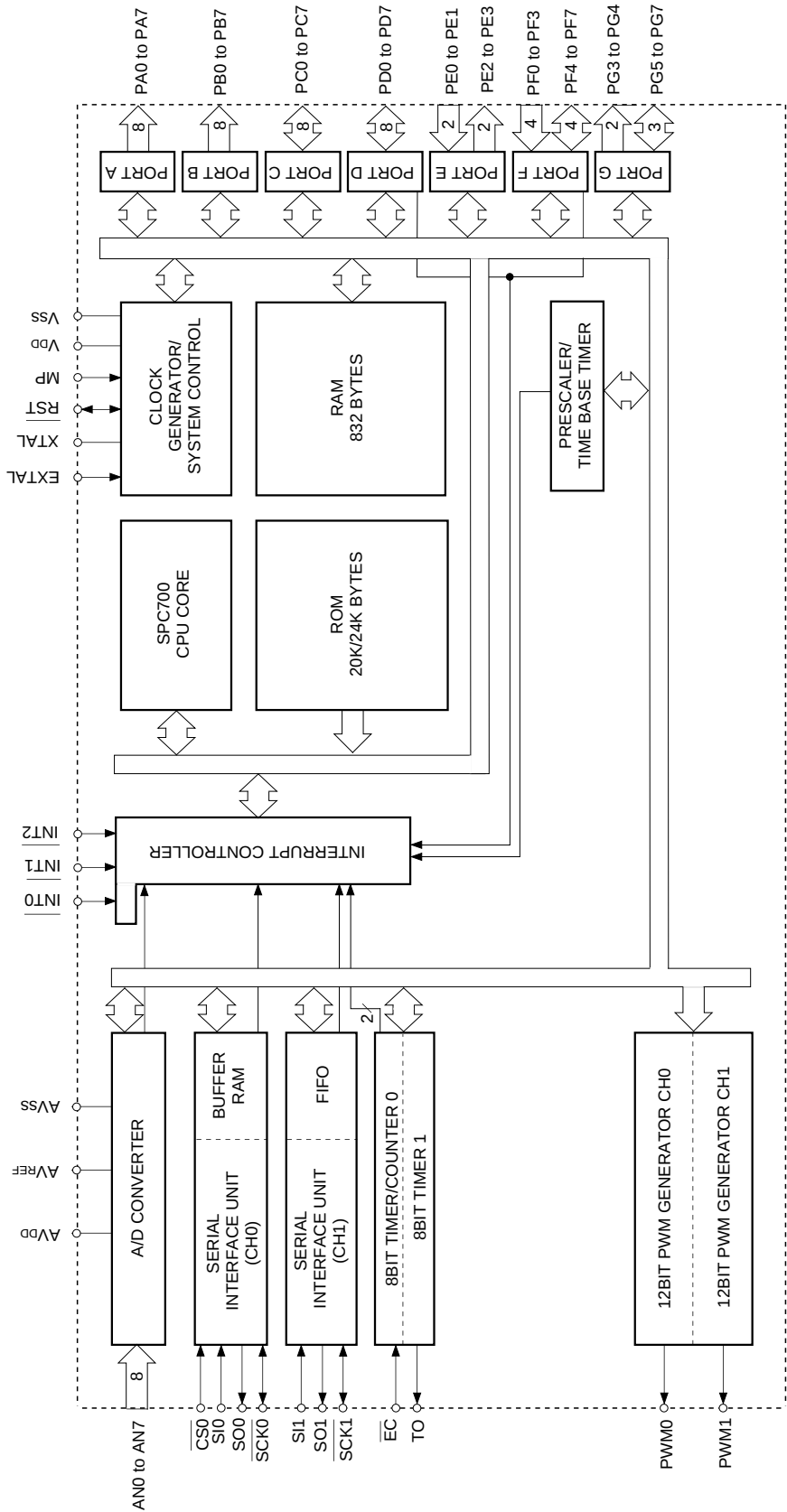
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (3.0 to 5.5V)
- Incorporated ROM capacity
 - 20K bytes (CXP81120)
 - 24K bytes (CXP81124)
- Incorporated RAM capacity
 - 832 bytes
- Peripheral functions
 - A/D converter
 - 8-bit, 8-channel, successive approximation system
(Conversion time: 20μs at 16MHz)
 - Serial interface
 - Incorporated buffer RAM (1 to 32 bytes auto transfer), 1 channel
 - Incorporated 8-bit and 8-stage FIFO
(1 to 8 bytes auto transfer), 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer
 - PWM output
 - 12 bits, 2 channels
- Interruption
 - 10 factors, 10 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 64-pin plastic QFP/LQFP
- Piggyback/evaluator
 - CXP81100 64-pin ceramic PQFP

Structure

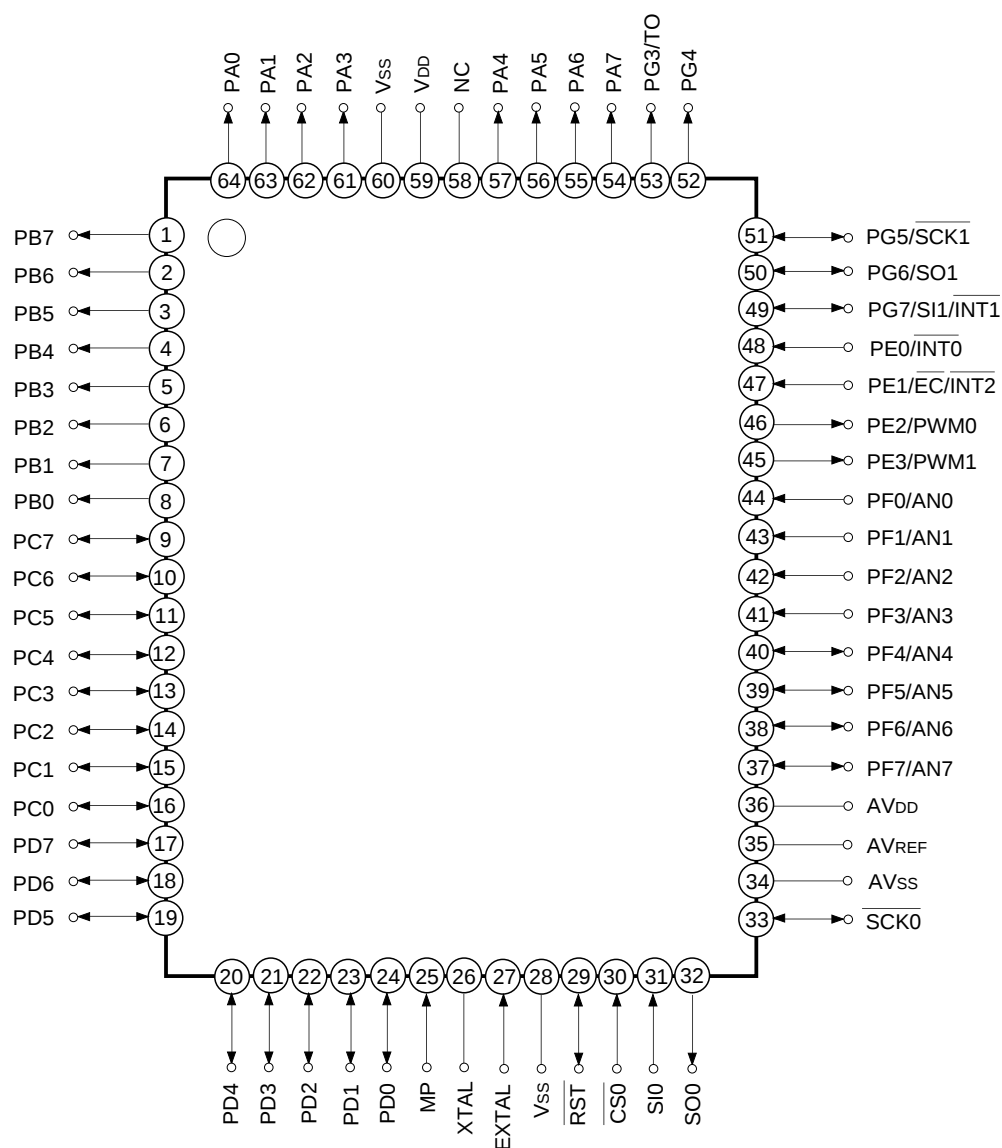
Silicon gate CMOS IC

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram

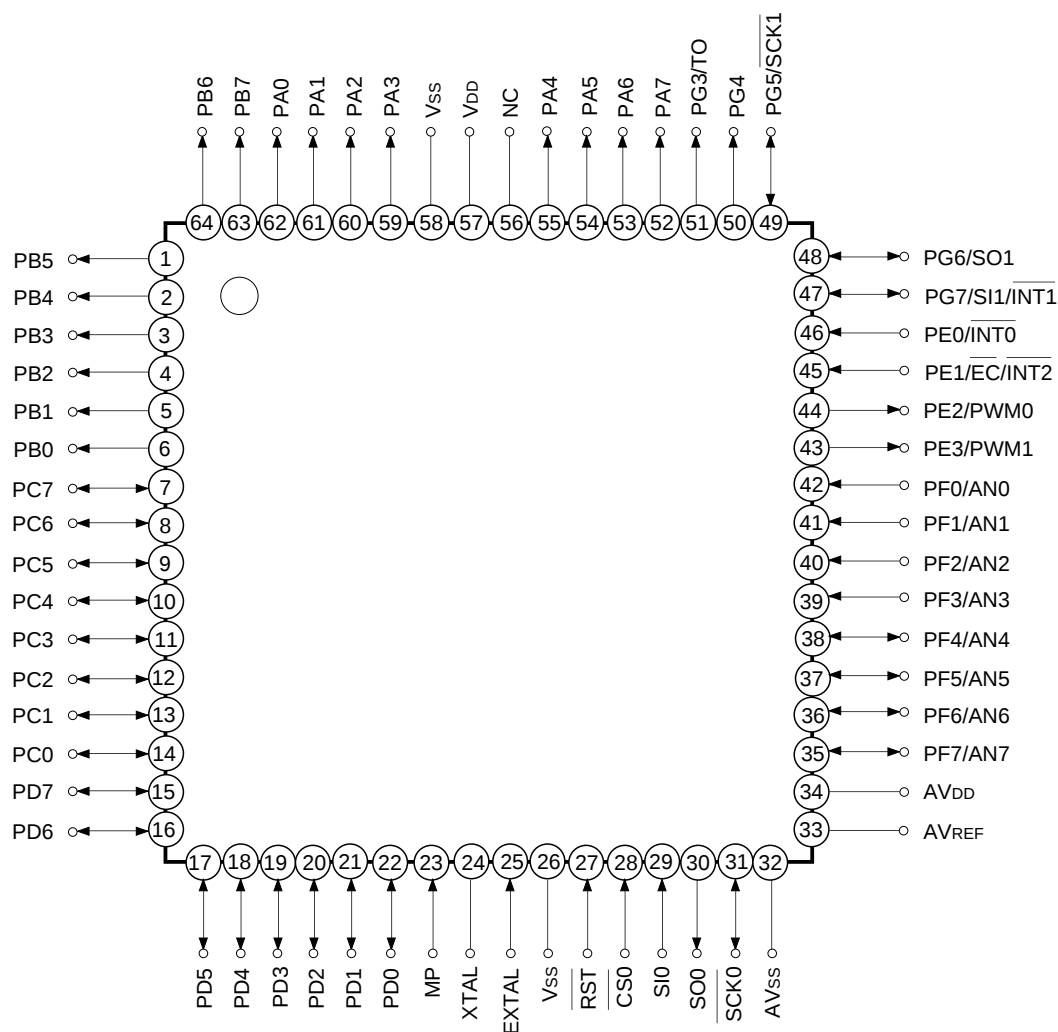


Pin Configuration (Top View) 64-pin QFP



- Note)**
1. NC (Pin 58) is always connected to VDD.
 2. Vss (Pins 28 and 60) are both connected to GND.
 3. MP (Pin 25) is always connected to GND.

Pin Configuration (Top View) 64-pin LQFP



- Note)**
1. NC (Pin 56) is always connected to V_{DD}.
 2. Vss (Pins 26 and 58) are both connected to GND.
 3. MP (Pin 23) is always connected to GND.

Pin Description

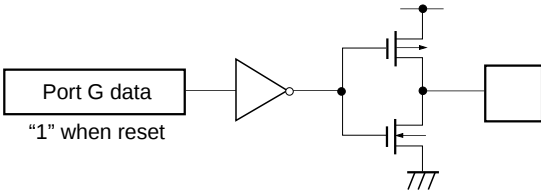
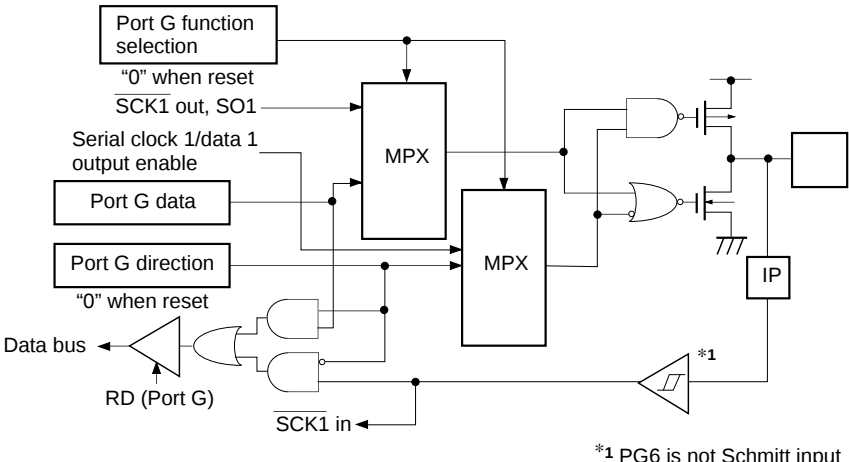
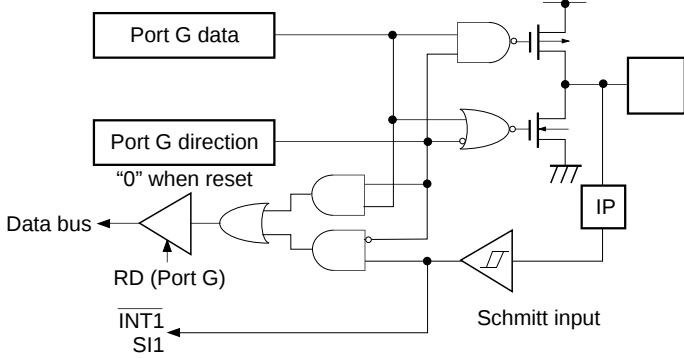
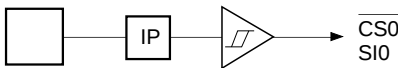
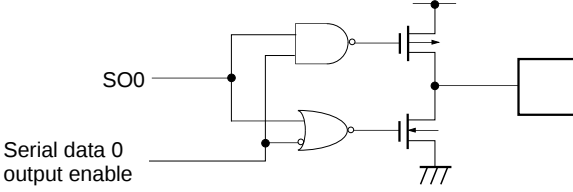
Symbol	I/O	Description		
PA0 to PA7	Output	(Port A) 8-bit output port. (8 pins)		
PB0 to PB7	Output	(Port B) 8-bit output port. (8 pins)		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O and function as standby release input can be set in a unit of single bits. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 4-bit port. Lower 2 bits are for input; upper 2 bits are for output. (4 pins)	Input to request external interruption. Active at the falling edge. (2 pins)	
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$	Input/Input/ Input		External event input for timer/counter.	
PE2/PWM0	Output/Output		12-bit PWM output. (2 pins)	
PE3/PWM1	Output/Output			
PF0/AN0 to PF3/AN3	Input/Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. Lower 4 bits also serve as standby release input. (8 pins)		Analog input to A/D converter. (8 pins)
PF4/AN4 to PF7/AN7	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O.		
SO0	Output	Serial data (CH0) output.		
SI0	Input	Serial data (CH0) input.		
$\overline{\text{CS0}}$	Input	Serial interface (CH0) chip select input.		
PG3/TO	Output/Output	(Port G) 5-bit port. Lower 2 bits are for output; upper 3 bits are for I/O. I/O can be set in a unit of single bits. (5 pins)	Timer/counter rectangular wave output.	
PG4	Output			
PG5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.	
PG6/SO1	I/O/Output		Serial data (CH1) output.	
PG7/SI1/ $\overline{\text{INT1}}$	I/O/Input Input		Serial data (CH1) input.	Input to request external interruption. Active at the falling edge.
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.		
XTAL	Output			
$\overline{\text{RST}}$	I/O	System reset; active at Low level. $\overline{\text{RST}}$ pin is I/O pin, which outputs “Low” level by incorporated power-on reset function when power turns on. (Mask option)		

Symbol	I/O	Description
NC		NC pin. Connect to V _{DD} for normal operation.
MP	Input	Test mode pin. Always connect to GND.
AV _{DD}		Positive power supply of A/D converter.
AV _{REF}	Input	Reference voltage input of A/D converter.
AV _{SS}		GND of A/D converter.
V _{DD}		Positive power supply.
V _{SS}		GND. Connect both V _{SS} pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format		When reset
PA0 to PA7 PB0 to PB7 16 pins	Port A Port B		Hi-Z
PC0 to PC7 8 pins	Port C		Hi-Z
PD0 to PD7 8 pins	Port D		Hi-Z
PE0/ $\overline{\text{INT0}}$ 1 pin	Port E		Hi-Z
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$ 1 pin	Port E		Hi-Z

Pin	Circuit format	When reset
PE2/PWM0 PE3/PWM1 2 pins	Port E	Hi-Z
PF0/AN0 to PF3/AN3 4 pins	Port F	Hi-Z
PF4/AN4 to PF7/AN7 4 pins	Port F	Hi-Z
PG3/TO 1 pin	Port G	High level

Pin	Circuit format	When reset
PG4 1 pin	Port G 	H level
PG5/SCK1 PG6/SO1 2 pins	Port G  *1 PG6 is not Schmitt input	Hi-Z
PG7/SI1/INT1 1 pin	Port G 	Hi-Z
CS0 SI0 2 pins	Schmitt input 	Hi-Z
SO0 1 pin		Hi-Z

Pin	Circuit format	When reset
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	• Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes "High" level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level
MP 1 pin		Hi-Z

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0	V	
	AV _{SS}	−0.3 to +0.3	V	
	AV _{REF}	AV _{SS} to +7.0	V	
Input voltage	V _{IN}	−0.3 to +7.0*1	V	
Output voltage	V _{OUT}	−0.3 to +7.0*1	V	
High level output current	I _{OH}	−5	mA	
High level total output current	ΣI _{OH}	−50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	
Low level total output current	ΣI _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-64P-L01
		380	mW	LQFP-64P-L01

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V. (CS0 and SI0 excluded.)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	3.0	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing mode
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode
		2.5	5.5	V	Guaranteed data hold range during stop mode
Analog voltage	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3
			5.5	V	CMOS Schmitt input*4
	V _{IHEX}	V _{DD} – 0.4	V _{DD} + 0.3	V	EXTAL pin*5
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7
			0.2V _{DD}	V	*2, *6
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3, *4
	V _{ILEX}	–0.3	0.4	V	EXTAL pin*5
Operating temperature	T _{opr}	–20	+75	°C	

*1 AV_{DD} should be the same voltage as V_{DD}.

*2 Normal input port (PC, PD, PF0 to PF3 and PG6 pins), MP pin.

*3 SCK0, RST, INT0, EC/INT2, SCK1 and SI1/INT1 pins.

*4 CS0 and SI0 pins.

*5 Specified only when the external clock is input.

*6 In case of 3.0 to 3.6V supply voltage (V_{DD}).

*7 In case of 4.5 to 5.5V supply voltage (V_{DD}).

DC Characteristics

Supply voltage ($V_{DD} = 4.5$ to $5.5V$)

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, SO0, SCK0, RST*1	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	(V _{OL} only) PG3 to PG7	$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.5		-40	μA
	I_{ILR}	RST*2	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-1.5		-400	μA
I/O leakage current	I_{IZ}	PA to PG, MP, CS0, SI0, SO0, SCK0, RST*2	$V_{DD} = 5.5V$, $V_I = 0, 5.5V$			± 10	μA
Supply current*3	I_{DD1}	V_{DD}	1/2 frequency dividing mode $V_{DD} = 5V \pm 0.5V$, 16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		20	40	mA
	I_{DDS1}		Sleep mode $V_{DD} = 5V \pm 0.5V$, 16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		1	5	mA
	I_{DDS3}		Stop mode $V_{DD} = 5.5V$, termination of 16MHz oscillation			10	μA
Input capacity	C_{IN}	PC, PD, PE0, PE1, PF, PG5 to PG7, RST, CS0, SI0, SCK0, EXTAL	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 RST pin is specified only when the power-on reset circuit is selected with mask option.

*2 For RST pin, specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

*3 When all output pins are open.

DC Characteristics

Supply voltage ($V_{DD} = 3.0$ to $3.6V$)

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, $\overline{SO0}$, $\overline{SCK0}$, $\overline{RST}^{*1}$	$V_{DD} = 3.0V$, $I_{OH} = -0.15mA$	2.7			V
			$V_{DD} = 3.0V$, $I_{OH} = -0.5mA$	2.3			V
Low level output voltage	V_{OL}	(V _{OL} only) PG3 to PG7	$V_{DD} = 3.0V$, $I_{OL} = 1.2mA$			0.3	V
			$V_{DD} = 3.0V$, $I_{OL} = 1.6mA$			0.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.6V$, $V_{IH} = 3.6V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.3		-20	μA
	I_{ILR}	$\overline{RST}^{*2}$	$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.9		-200	μA
I/O leakage current	I_{IZ}	PA to PG, MP, $\overline{CS0}$, $\overline{SI0}$, $\overline{SO0}$, $\overline{SCK0}$, $\overline{RST}^{*2}$	$V_{DD} = 3.6V$, $V_I = 0, 3.6V$			± 10	μA
Supply current ^{*3}	I_{DD2}	V_{DD}	1/2 frequency dividing mode $V_{DD} = 3.3V \pm 0.3V$, 12MHz crystal oscillation ($C_1 = C_2 = 15pF$)		10	20	mA
	I_{DDS2}		Sleep mode $V_{DD} = 3.3V \pm 0.3V$, 12MHz crystal oscillation ($C_1 = C_2 = 15pF$)		0.5	2.5	mA
	I_{DDS3}		Stop mode $V_{DD} = 5.5V$, termination of 12MHz oscillation			10	μA
Input capacity	C_{IN}	PC, PD, PE0, PE1, PF, PG5 to PG7, $\overline{RST}$, $\overline{CS0}$, $\overline{SI0}$, $\overline{SCK0}$, EXTAL	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 $\overline{RST}$ pin is specified only when the power-on reset circuit is selected with mask option.

*2 For $\overline{RST}$ pin, specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

*3 When all output pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, V_{DD} = 3.0 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f _c	XTAL EXTAL	Fig. 1, Fig. 2 V _{DD} = 4.5 to 5.5V	1	16	MHz
				1	12	
System clock input pulse width	t _{XL} , t _{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive) V _{DD} = 4.5 to 5.5V	28		ns
				37.5		
System clock input rise and fall times	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count input clock pulse width	t _{EL} , t _{EH}	$\overline{EC}$	Fig. 3	4t _{sys} *1		ns
Event count input clock rise and fall times	t _{ER} , t _{EF}	$\overline{EC}$	Fig. 3		20	ms

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/f_c (Upper 2 bits = "00"), 4000/f_c (Upper 2 bits = "01"), 16000/f_c (Upper 2 bits = "11")

Fig. 1. Clock timing

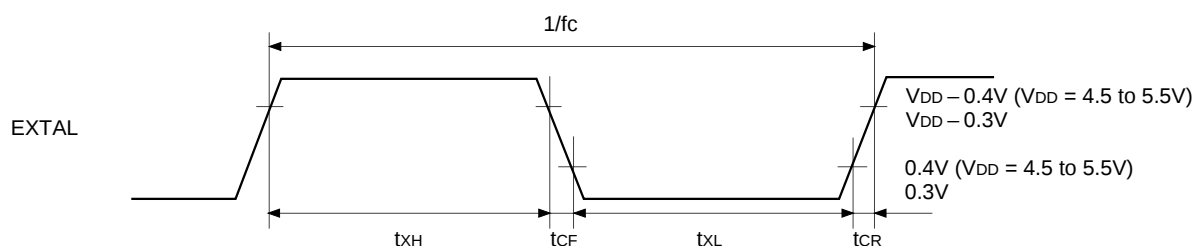


Fig. 2. Clock applied condition

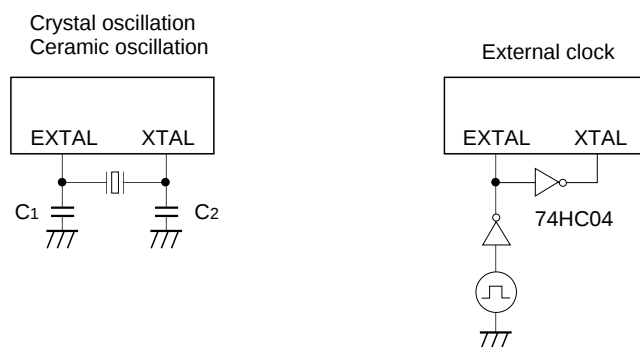
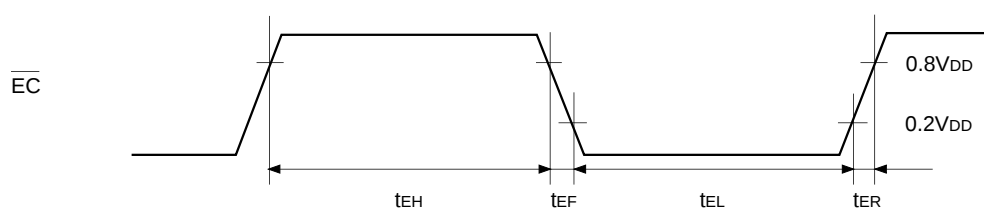


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 100$		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK}}$ input mode	$-t_{\text{sys}} + 100$		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK}}$ input mode	$2t_{\text{sys}} + 100$		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK}}$ input mode		$2t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) $\overline{\text{CS}}$, $\overline{\text{SCK}}$, SI and SO represents $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, SI0, and SO0, respectively.

Note 3) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 250$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 250$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 150$		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	$-t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	$2t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		$2t_{sys} + 250$	ns
			$\overline{SCK}$ output mode		125	ns

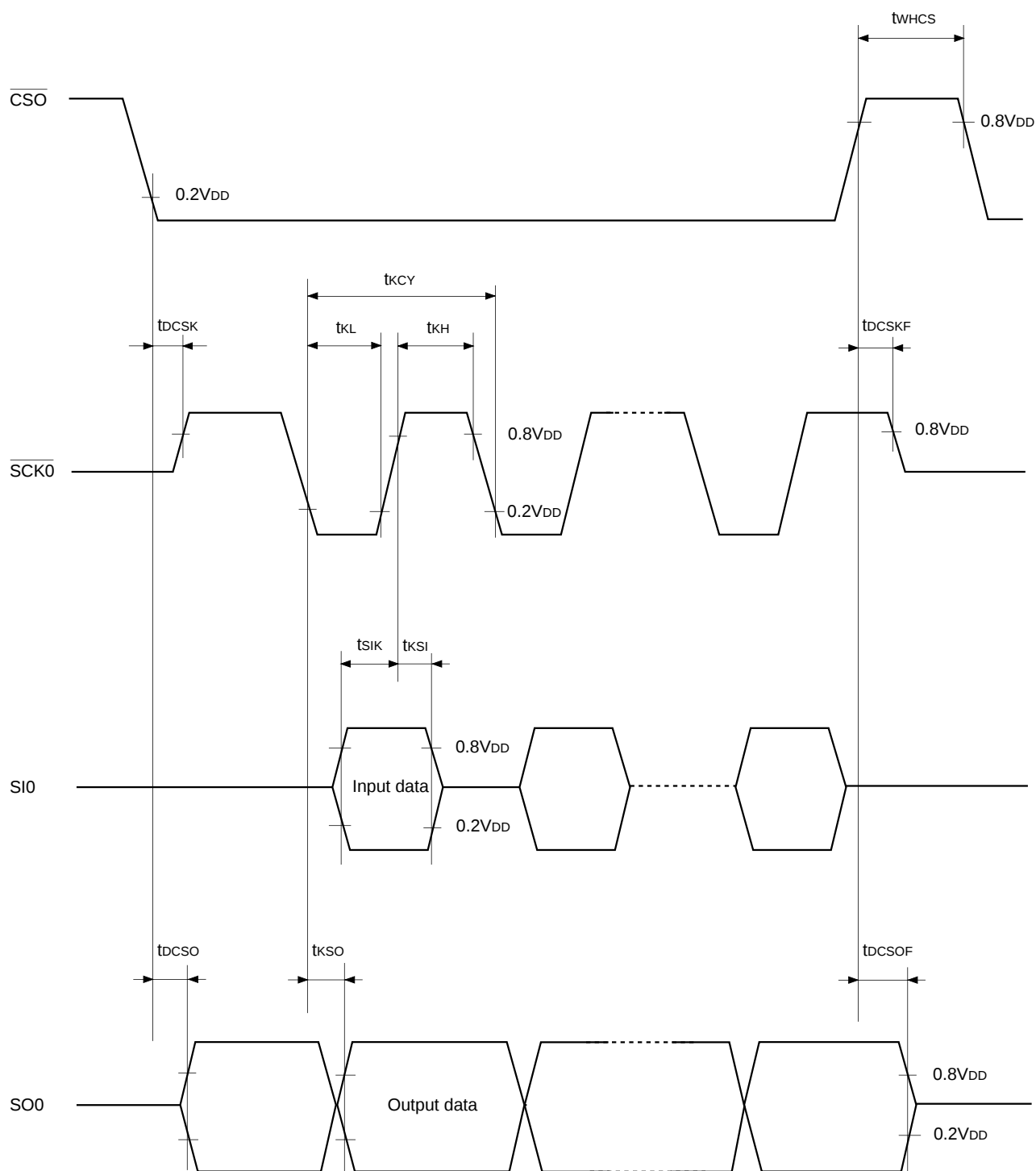
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represents $\overline{CS0}$, $\overline{SCK0}$, SI0, and SO0, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode)(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	SCK1	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
SCK1 high and low level widths	t_{KH} t_{KL}	SCK1	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for SCK1 $\uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for SCK1 $\uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 $\downarrow \rightarrow$ SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (SIO mode)(Ta = -20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

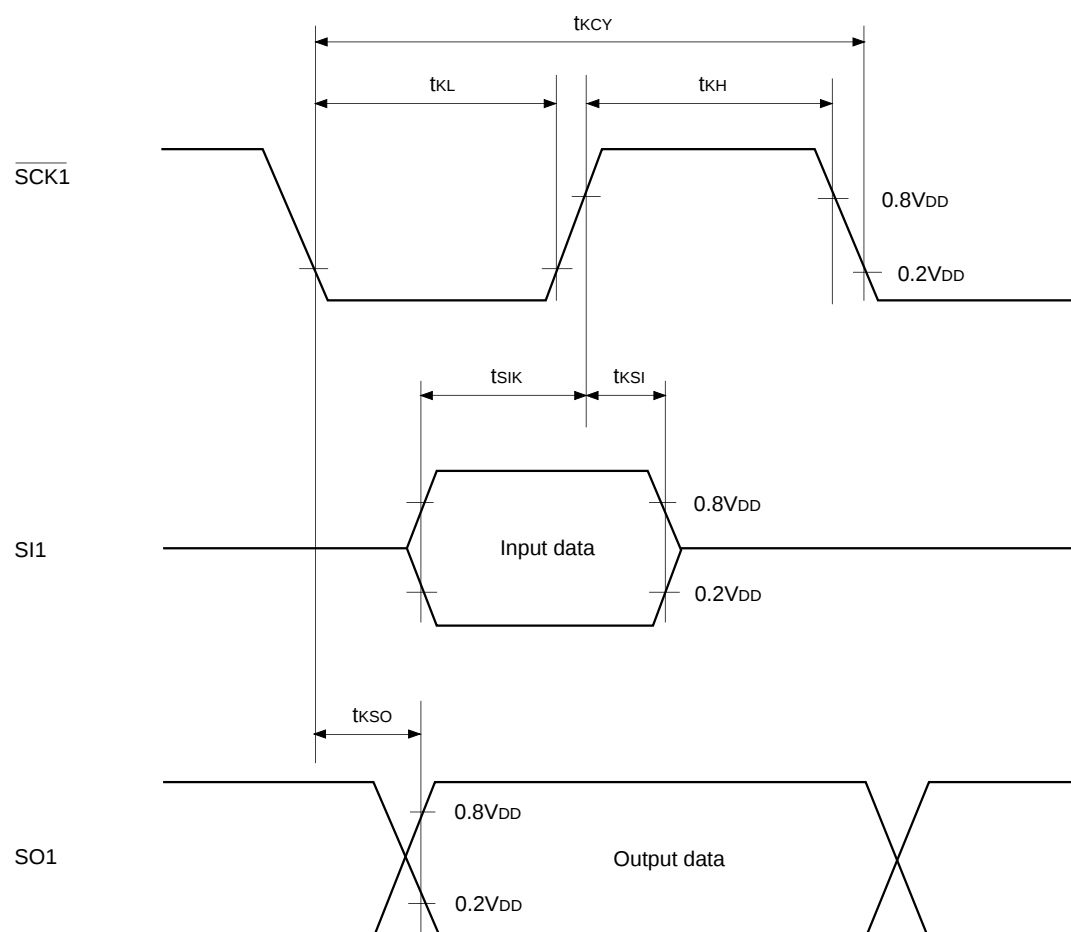
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	SCK1	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
SCK1 high and low level widths	t_{KH} t_{KL}	SCK1	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 150$		ns
SI1 input setup time (for SCK1 $\uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for SCK1 $\uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
SCK1 $\downarrow \rightarrow$ SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode) ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 01FAH) lower 2 bits (SO1 clock selection) is set at $104\mu\text{s}$ according to the system clock frequency.

Note) The load of SO1 pin is $50\text{pF} + 1\text{TTL}$.

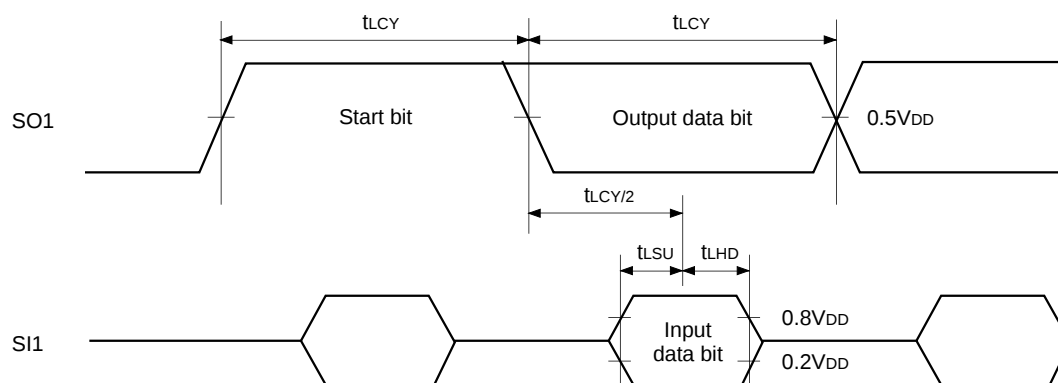
Serial transfer (CH1) (Special mode) ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 3.6V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		μs
SI1 data setup time	t_{LSU}	SI1		2			μs
SI1 data hold time	t_{LHD}	SI1		2			μs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 01FAH) lower 2 bits (SO1 clock selection) is set at $104\mu\text{s}$ according to the system clock frequency.

Note) The load of SO1 pin is 50pF .

Fig. 6. Serial transfer CH1 timing (Special mode)



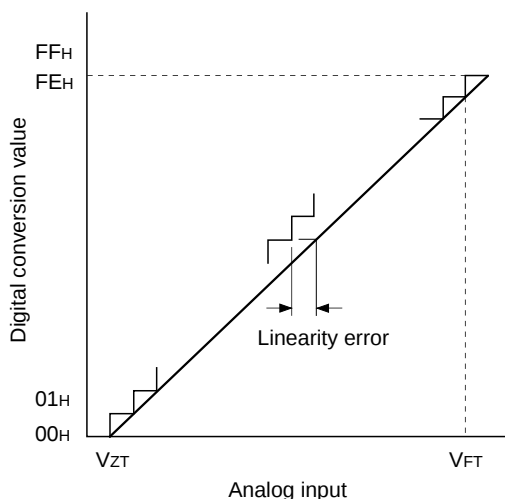
(3) A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$			± 1	LSB
Absolute error			$V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 2	LSB
Conversion time	t_{CONV}			$160/f_{\text{ADC}}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{\text{ADC}}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{\text{REF}} = 4.0$ to 5.5V		0.6	1.0	mA
			Sleep mode Stop mode			10	μA

A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 3.0$ to 3.6V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$			± 1	LSB
Absolute error			$V_{DD} = AV_{DD} = AV_{REF} = 3.3\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 2	LSB
Conversion time	t_{CONV}			$160/f_{\text{ADC}}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{\text{ADC}}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{\text{REF}} = 2.7$ to 3.6V		0.4	0.7	mA
			Sleep mode Stop mode			10	μA

Fig. 7. Definitions of A/D converter terms



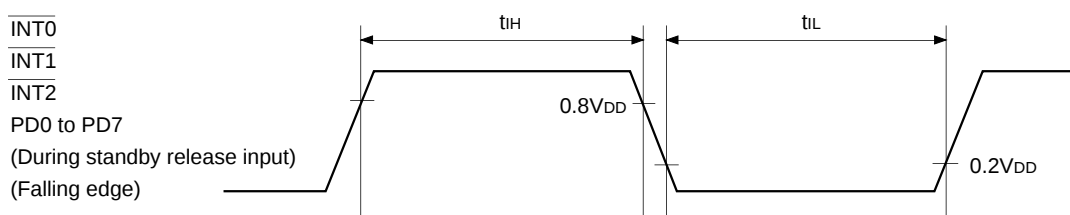
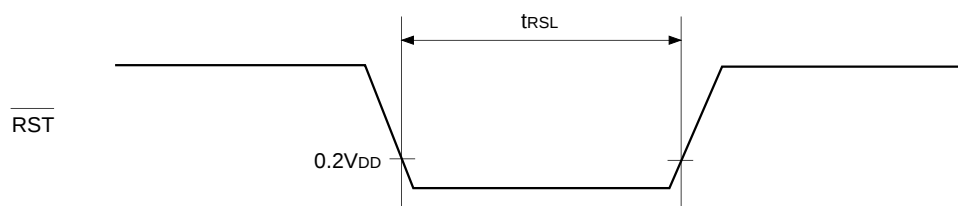
*1 The value of f_{ADC} is as follows by interruption selection/
ADC operation clock selection register (MSC: 01FF_H)
bit 0 (ADCCCK).

When PS2 is selected, $f_{\text{ADC}} = f_c/2$

When PS1 is selected, $f_{\text{ADC}} = f_c$

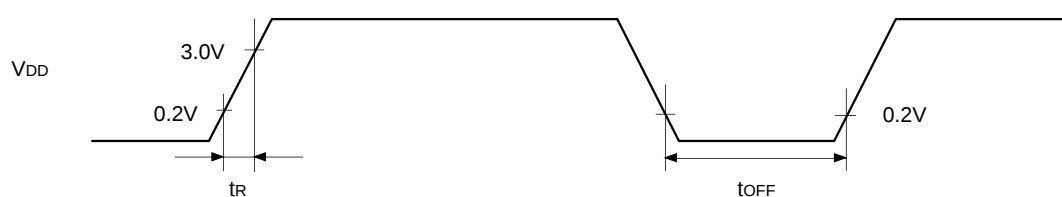
(4) Interruption, reset input ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ PJ0 to PJ7		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 8. Interruption input timing**Fig. 9. Reset input timing****(5) Power-on reset*1** ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power-on reset	0.05	30	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

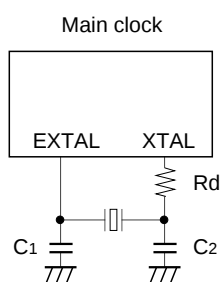
*1 Specifies only when power-on reset function is selected.

Fig. 10. Power-on reset

The power supply should be turned on smoothly.

Appendix

Fig. 11. SPC 700 Series recommended oscillation circuit



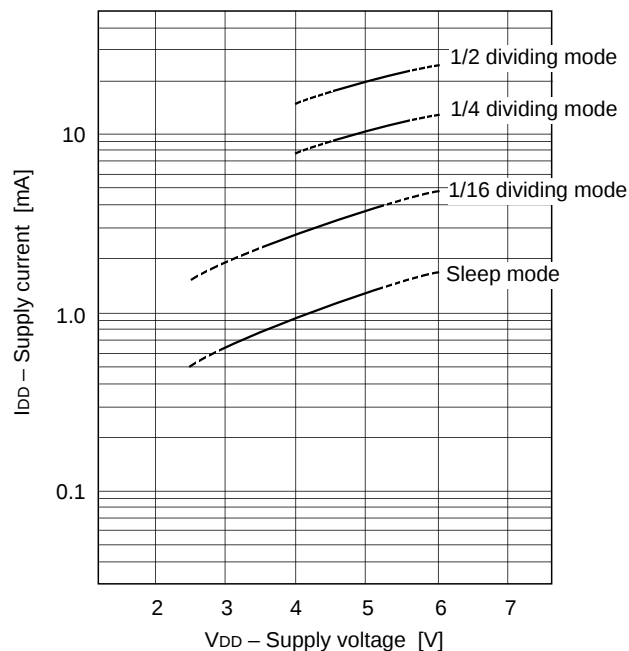
Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	R _d (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

Mask Option Table

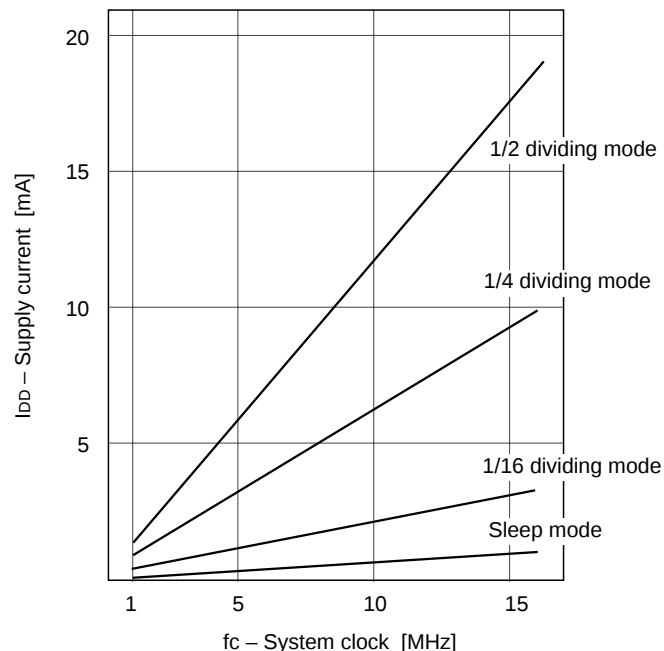
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

Characteristics Curve

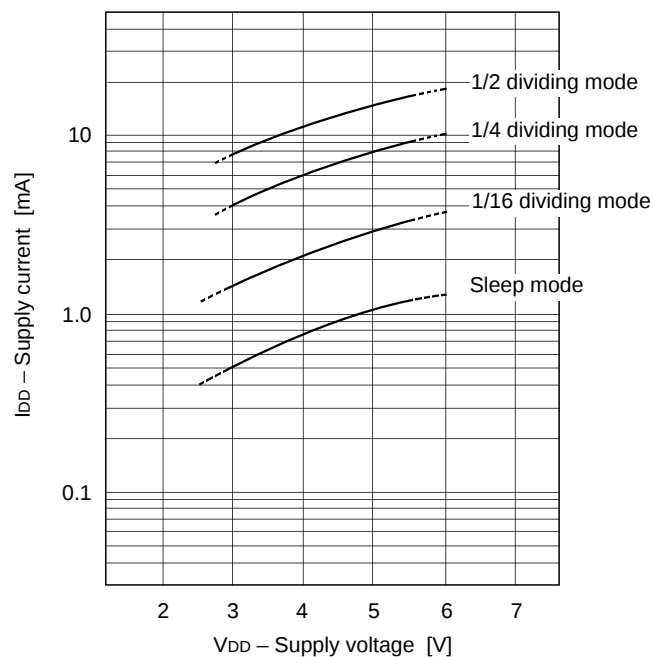
I_{DD} vs. V_{DD}
(f_c = 16MHz, T_a = 25°C, Typical)



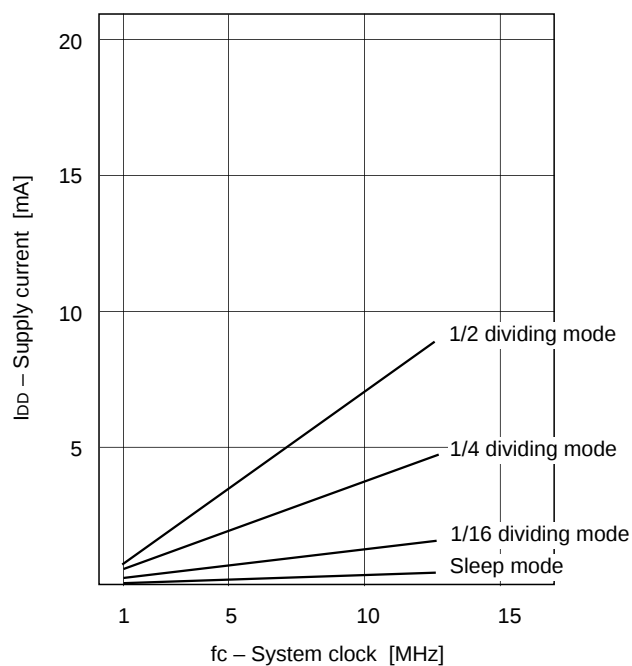
I_{DD} vs. f_c
(V_{DD} = 5V, T_a = 25°C, Typical)



I_{DD} vs. V_{DD}
(f_c = 12MHz, T_a = 25°C, Typical)



I_{DD} vs. f_c
(V_{DD} = 3.3V, T_a = 25°C, Typical)



Unit: mm

Technical drawing of a rectangular component with dimensions and tolerances. The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 23.9 ± 0.4
- Inner width: $20.0 \begin{smallmatrix} +0.4 \\ -0.1 \end{smallmatrix}$
- Overall height: 17.9 ± 0.4
- Inner height: $14.0 \begin{smallmatrix} +0.4 \\ -0.1 \end{smallmatrix}$
- Pin 1 location (bottom left): 1.0
- Pin 19 location (bottom right): $0.4 \begin{smallmatrix} +0.15 \\ -0.1 \end{smallmatrix}$
- Pin 51 location (top left): 51
- Pin 33 location (top right): 33
- Pin 32 location (right side): 32
- Pin 20 location (bottom right): 20
- Pin 64 location (bottom left): 64

Side View Dimensions:

- Overall height: 16.3
- Pin 1 location (bottom left): 0.8 ± 0.2
- Pin 19 location (bottom right): $2.75 \begin{smallmatrix} +0.35 \\ -0.15 \end{smallmatrix}$
- Pin 51 location (top left): 51
- Pin 33 location (top right): 33
- Pin 32 location (right side): 32
- Pin 20 location (bottom right): 20
- Pin 64 location (bottom left): 64

Other Dimensions:

- Pin 1 location (bottom left): 1.0
- Pin 19 location (bottom right): $0.4 \begin{smallmatrix} +0.15 \\ -0.1 \end{smallmatrix}$
- Pin 51 location (top left): 51
- Pin 33 location (top right): 33
- Pin 32 location (right side): 32
- Pin 20 location (bottom right): 20
- Pin 64 location (bottom left): 64

Notes:

- Pin 1 location (bottom left): 1.0
- Pin 19 location (bottom right): $0.4 \begin{smallmatrix} +0.15 \\ -0.1 \end{smallmatrix}$
- Pin 51 location (top left): 51
- Pin 33 location (top right): 33
- Pin 32 location (right side): 32
- Pin 20 location (bottom right): 20
- Pin 64 location (bottom left): 64

Material and Tolerances:

- Material: ± 0.12 (M)
- Tolerance: ± 0.1
- Pin 1 location (bottom left): 1.0
- Pin 19 location (bottom right): $0.4 \begin{smallmatrix} +0.15 \\ -0.1 \end{smallmatrix}$
- Pin 51 location (top left): 51
- Pin 33 location (top right): 33
- Pin 32 location (right side): 32
- Pin 20 location (bottom right): 20
- Pin 64 location (bottom left): 64

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

[illegible]

NOTE: Dimension “*” does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g