CY2DL818

1:8 Clock Fanout Buffer

Features

- **Low voltage operation**
- **V_{DD} = 3.3V**
- **1:8 fanout**
- **Single-input-configurable for LVDS, LVPECL, or LVTTL**
- **8 pair of LVDS Outputs**
- **Drives either a 50-ohm or 100-ohm load (selectable)**
- **Low input capacitance**
- **Low output skew**
- **Low propagation delay**
- **Typical (tpd < 4 ns)**
- **Packages available include: TSSOP**
- **Does not exceed Bellcore 802.3 standards**
- **Operation at => 350 MHz – 700 Mbps**

Description

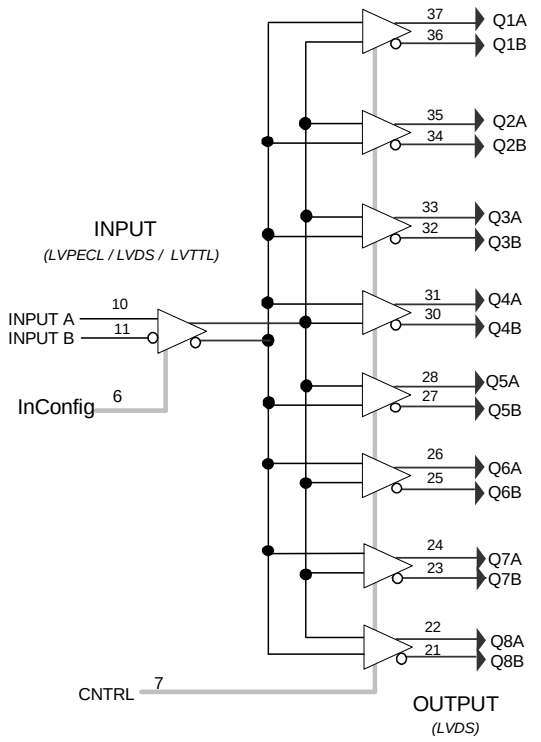
This Cypress series of network circuits is produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic.

The Cypress CY2DL818 fanout buffer features a single LVDS or a single-ended LVTTL-compatible input and eight LVDS output pairs.

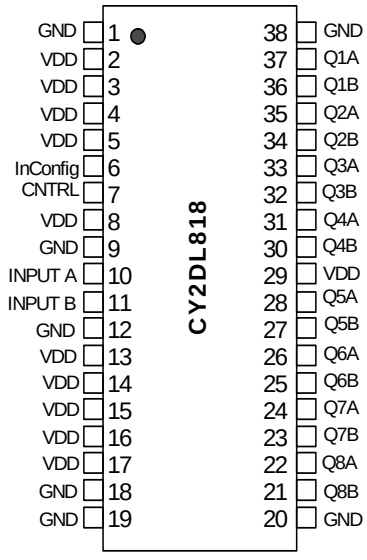
Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock. The Cypress CY2DL818 is ideal for both level translations from single-ended to LVDS and/or for the distribution of LVDS-based clock signals.

The Cypress CY2DL818 has configurable input and output functions. The input can be selectable for LVCMOS/LVTTL, LVPECL, or LVDS signals, while the output drivers support standard and high-drive LVDS. Drive either a 50-ohm or 100-ohm line with a single part number/device.

Block Diagram



Pin Configuration



38 pin TSSOP

Pin Description

Pin Number	Pin Name	Pin Standard Interface	Pin Description
1, 9,12, 18,19,20,38	G_{ND}	POWER	Ground
2,3,4,5,8, 13 14,15,16,17,29	V_{DD}	POWER	Power Supply
10,11	Input A, Input B(#)	Default: LVPECL / LDVS Optional: LVTTL/LVCMOS single pin.	Differential input pair or single line. LVPECL/LVDS default. See InConfig below.
37, 36,35,34, 33,32,31, 30, 28,27,26,25, 24,23,22,21	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, Q6A, Q6B, Q7A, Q7B, Q8A, Q8B	LDVS	Differential Outputs
6	InConfig	LVTTL / LVCMOS	Converts inputs from the default LVPECL/LVDS (logic = 0) To LVTTL/LVCMOS (logic = 1) “default pull-up” See *Figure 5* and *Figure 6* for additional information
7	CNTRL	LVTTL / LVCMOS	Converts into a high-speed driver. Logic = 0 = 100 ohm Logic = 1 = 50-ohm “default pull-up” See *Figure 7* for additional Information

Output Drive Control for Standard and Bus/B/Hi-Drive

CNTRL Pin 7 Binary Value	Drive STD	Impedance	Output Voltage Value
0	Standard	100 Ohms	$V_{O =}$ Voutput
		50 Ohms	$V = 1/2 * V_O$
1	Hi-drive/Bus/B	100 Ohms	$V = 2 * V_O$
		50 Ohms	$V = V_O$

Input Receiver Configuration for Differential or LVTTL/LVCMOS

InCONFIG Pin 6 Binary Value	Input Receiver Family	Input Receiver Type
1	LVTTL in LVCMOS	Single-ended non-inverting, inverting, void of bias resistors.
0	LVDS	Low-voltage differential signaling
	LVPECL	Low-voltage pseudo (positive) emitter coupled logic

Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal

LVTTL/LVCMOS INPUT LOGIC			
Input Condition		Input Logic	Output Logic Q Pins, Q1A or Q1
Ground	Input B (–) Pin 11	Input	Input
	Input A (+) Pin 10	Input – Bar	Input – Bar
VCC	Input B (–) Pin 11	Input	Input – Bar
	Input A (+) Pin 10	Input – Bar	Input
Ground	Input A (+) Pin 10	Input	Input
	Input B (–) Pin 11	Input – Bar	Input – Bar
VCC	Input A (+) Pin 10	Input	Input – Bar
	Input B (–) Pin 11	Input – Bar	Input

Power Supply Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open		0.40	0.5	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL = 100 MHz		40	80	mA

Maximum Ratings[1][2]

Storage Temperature: .....–65°C to + 150°C

Ambient Temperature:.....–40°C to +85°C

Supply Voltage to Ground Potential

(Inputs and V_{CC} only)..... –0.3V to 4.6V

Supply Voltage to Ground Potential

(Outputs only) ..... –0.3V to V_{DD} + 0.3V

DC Input Voltage ..... –0.3V to V_{DD} + 0.3V

DC Output Voltage..... –0.3V to V_{DD} + 0.9V

Power Dissipation..... 0.75W

DC Electrical Characteristics: 3.3V–LVDS Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{ID}	Magnitude of Differential Input Voltage			100		600	mV
V_{IC}	Common-mode of Differential Input Voltage$\|V_{ID}\|$ (min. and max.)			$\|V_{ID}\|/2$	2.4 – ($\|V_{ID}\|/2$)		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level	InConfig/Cntrl Pins	2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max	$V_{IN} = V_{DD}$		±10	±20	µA
I_{IL}	Input Low Current	V_{DD} = Max	$V_{IN} = V_{SS}$		±10	±20	µA
I_I	Input High Current	V_{DD} = Max, $V_{IN} = V_{DD}$(max.)				±20	µA

DC Electrical Characteristics: 3.3V–LVPECL Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
$\|V_{ID}\|$	Differential input voltage p-p	Guaranteed Logic High Level		400		2400	mV
V_{CM}	Common-Mode Voltage			1.65		2.25	V
I_{IH}	Input High Current	V_{DD} = Max	$V_{IN} = V_{DD}$		±10	±20	µA
I_{IL}	Input Low Current	V_{DD} = Max	$V_{IN} = V_{SS}$		±10	±20	µA

DC Electrical Characteristics: 3.3V–LVTTL/LVCMOS Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max	V_{IN} = 2.7V			1	µA
I_{IL}	Input Low Current	V_{DD} = Max	V_{IN} = 0.5V			–1	µA
I_I	Input High Current	V_{DD} = Max., $V_{IN} = V_{DD}$(Max)				20	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = -18mA			–0.7	–1.2	V
V_H	Input Hysteresis				80		mV

DC Electrical Characteristics: 3.3V–LVDS OUTPUT

Parame-ter	Description	Conditions		Min.	Typ.	Max.	Unit
$\|V_{OD}\|$	Differential Output Voltage p-p	V_{DD} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}	RL = 100 ohm	0.25		0.55	V
Risetime	Pin Control (pin 7) logic is “FALSE” **defaulting to 100-ohm output** DIfferential 20% to 80%	CL – 10 pF RL and CL to G_{ND} CL = $C_{intrinsic}$ and $C_{external}$ See *Figure 3*			800	1500	ps
Falltime					800	1500	ps
Risetime	Pin Control (pin 7) logic is “TRUE” **setting 50-ohm output drivers** differential 20% to 80%	CL – 10 pF RL and CL to G_{ND} CL = $C_{intrinsic}$ and $C_{external}$ See *Figure 3*	RL = 50 ohm		350	600	ps
Falltime					350	600	ps
I_{OS}	Output Short Circuit	D_{OUT} = 0V or D_{OUT} = 0V				–10	mA
V_{OH}	Output Voltage high		RL = 100 ohm			1550	mV
V_{OL}	Output Voltage low			925			mV

Notes:

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

AC Switching Characteristics @ 3.3 V V_{DD} = 3.3V ±5%, Temperature = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ	Max	Unit
t_{PLH}	Propagation Delay – Low to High			4.5		ns
t_{PHL}	Propagation Delay – High to Low			4.5		ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)				200	ps
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$)			200		ps
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.				1.6	ns

High Frequency Parametrics

Parameter	Description	Conditions	Min.	Typ	Max	Unit
F_{max}	Maximum frequency V_{DD} = 3.3V	50% duty cycle tW(50-50) Standard Load Circuit. LVDS V_{ID} = 100 mV			400	MHz
D_j	Deterministic Jitter	50% duty cycle tW(50-50) Standard Load Circuit. LVDS V_{ID} = 100 mV		50		ps

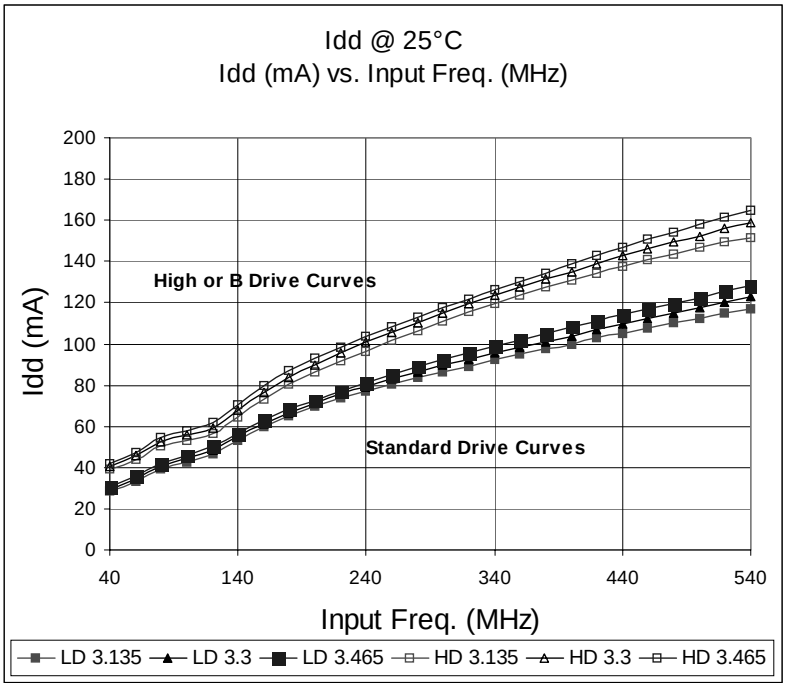
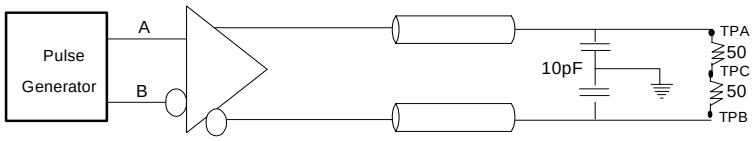


Figure 1. IDD Current vs. Frequency in Low Drive and High Drive Full Load



Standard Termination

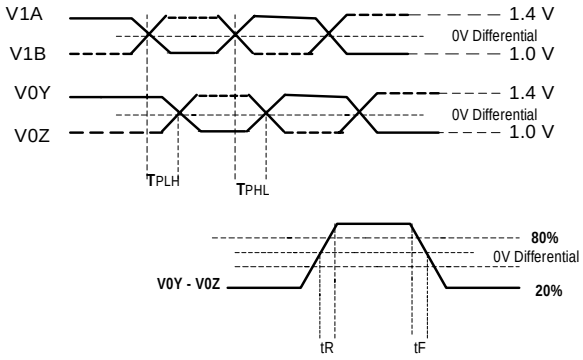


Figure 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time[3,4,5,6]

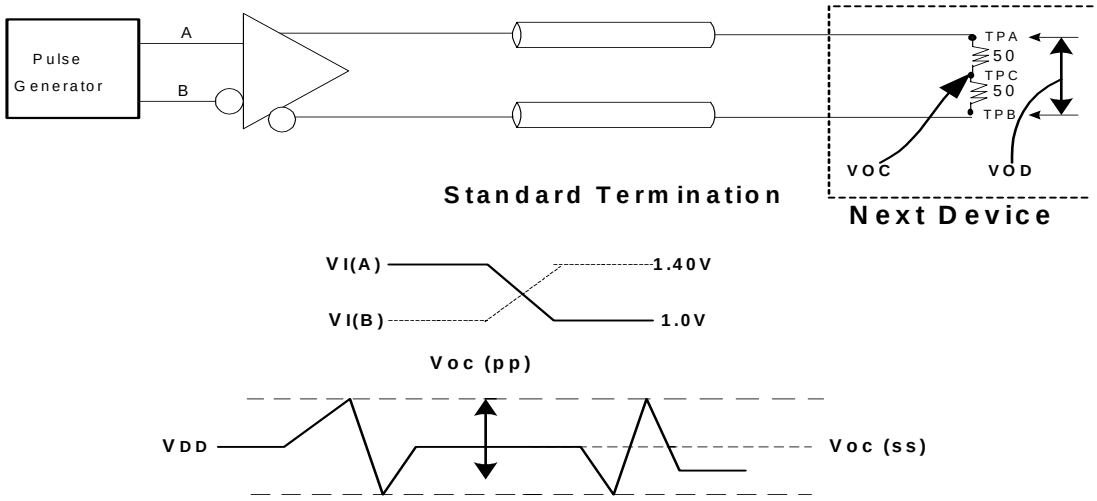
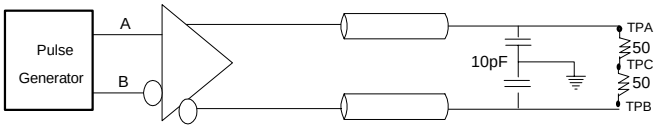


Figure 3. Test Circuit and Voltage Definitions for the Driver Common-Mode Output Voltage[3,4,5,6,7]

Notes:

3. All input pulses are supplied by a frequency generator with the following characteristics: TR and tF ≤ 1 ns; pulse rate = 50 Mpps; pulse width = 10 ± 0.2 ns.
4. RL = 50 ohm/100 ohm ± 1%.
5. CL includes instrumentation and fixture capacitance within 6 mm of the DUT.
6. TPA and B are used for prop delay and Rise/Fall Measurements. TPC is used for VOC measurements only.
7. All outputs should be loaded, used or not, in order to minimize noise and currents.



Standard Termination

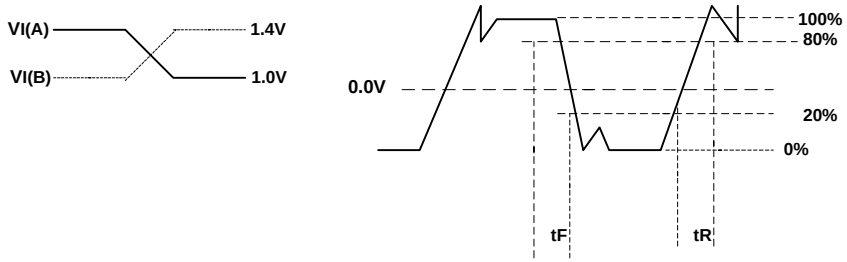
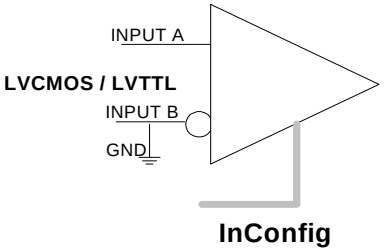
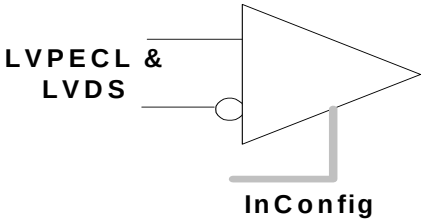


Figure 4. Test Circuit and Voltage Definitions for the Differential Output Signal [3,4,5,6]



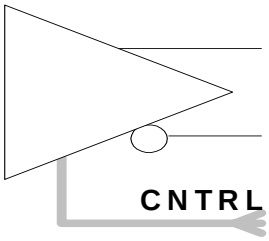
1	**LVTTL/LVCMOS**

Figure 5. InConfig Control for LVCMOS Input[8]



0	**LVDS/LVPECL**

Figure 6. InConfig Control for Differential Input[9]



0	Standard	100 Ohms	'Vo = Vo
		50 Ohms	'Vo = 1/2 Vo
1	Hi Drive B	100 Ohms	'Vo = 2 Vo
		50 Ohms	'Vo = Vo

Figure 7. CNTRL Control for Standard or High-drive Drivers[10]

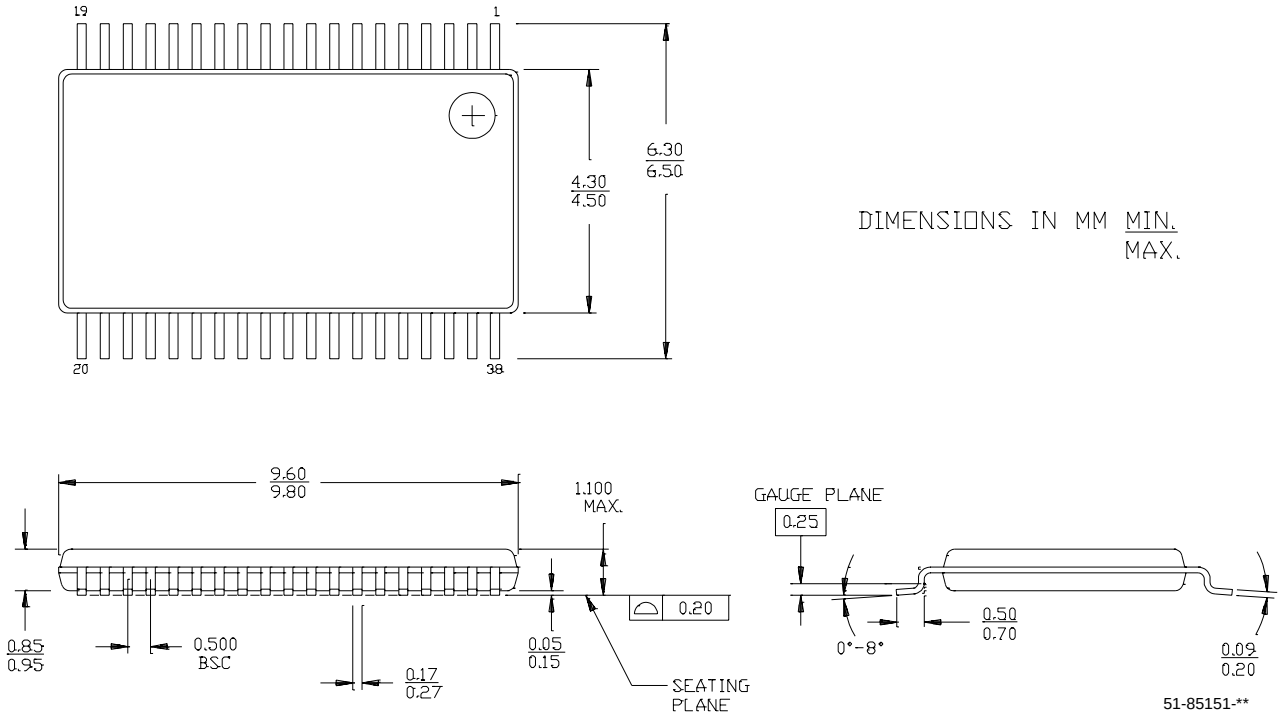
Notes:
8. See Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal on page 2.
9. LVPECL or LVDS differential input value.
10. Standard 100-ohm output impedance: high-drive 50-ohm output impedance.

Ordering Information

Part Number	Package Type	Product Flow
CY2DL818ZI	38-pin TSSOP	Industrial, –40° to 85°C
CY2DL818ZIT	38-pin TSSOP–Tape and Reel	Industrial, –40° to 85°C
CY2DL818ZC	38-pin TSSOP	Commercial, 0° to 70°C
CY2DL818ZCT	38-pin TSSOP–Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

38-pin TSSOP (4.40 mm body) Z38



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Document Title: CY2DL818 1:8 Clock Fanout Buffer Document Number: 38-07058				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115151	05/30/02	EHX	New Data Sheet
*A	117611	09/16/02	RGL	Changed the figure cross reference in page 2 and added a note 6 in page 5
*B	122745	12/15/02	RBI	Added power-up requirements to maximum ratings information.