

## 64K x 16 Static RAM

### Features

- 2.7V–3.6V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
  - 54 mW (max.) (15 mA)
- Low standby power (70 ns, LL version)
  - 54  $\mu$ W (max.) (15  $\mu$ A)
- Automatic power-down when deselected
- Independent control of Upper and Lower Bytes
- Available in 44-pin TSOP II (forward) and fBGA

### Functional Description

The CY62126BV is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption by 99% when deselected. The device enters power-down mode when  $\overline{CE}$  is HIGH.

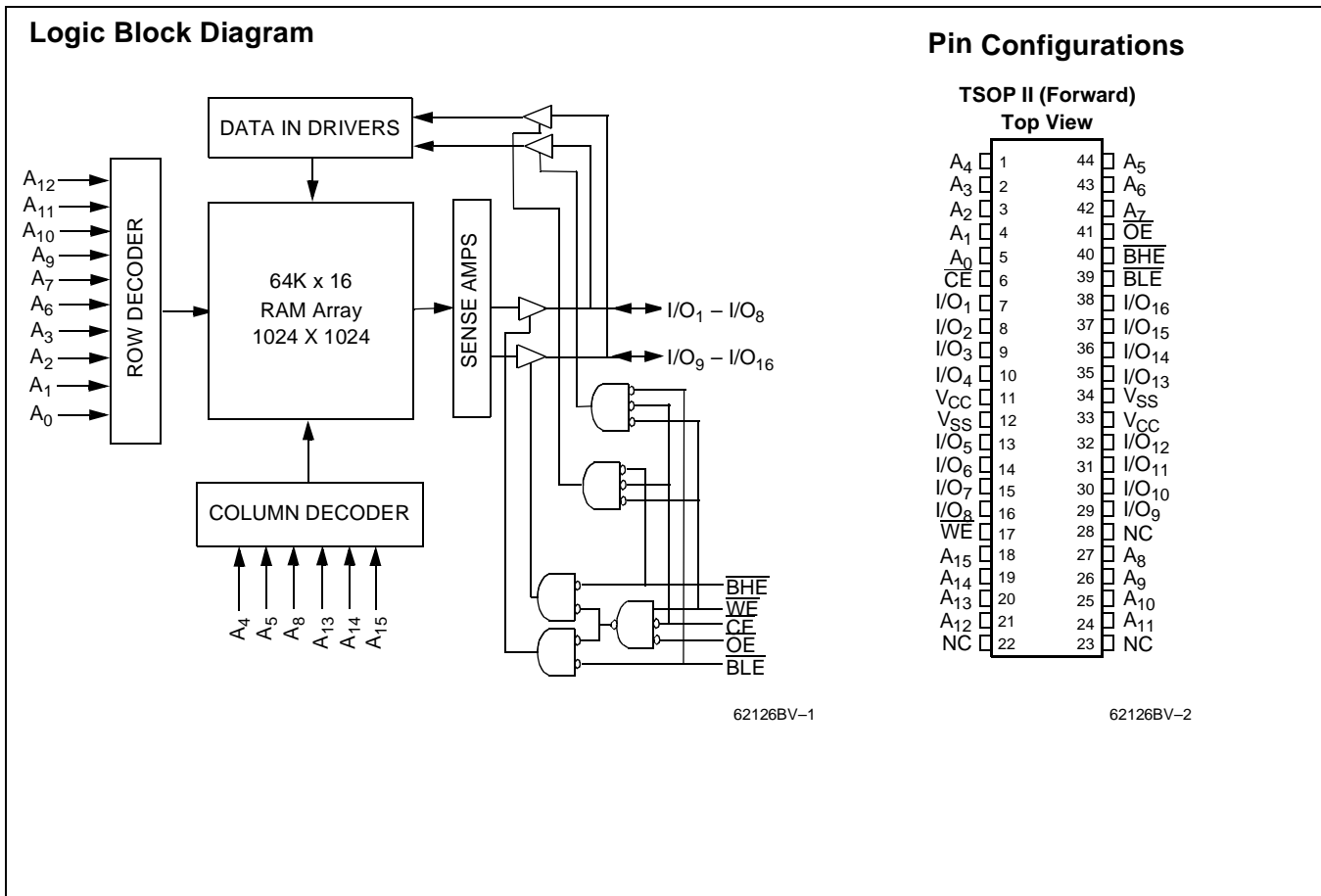
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable

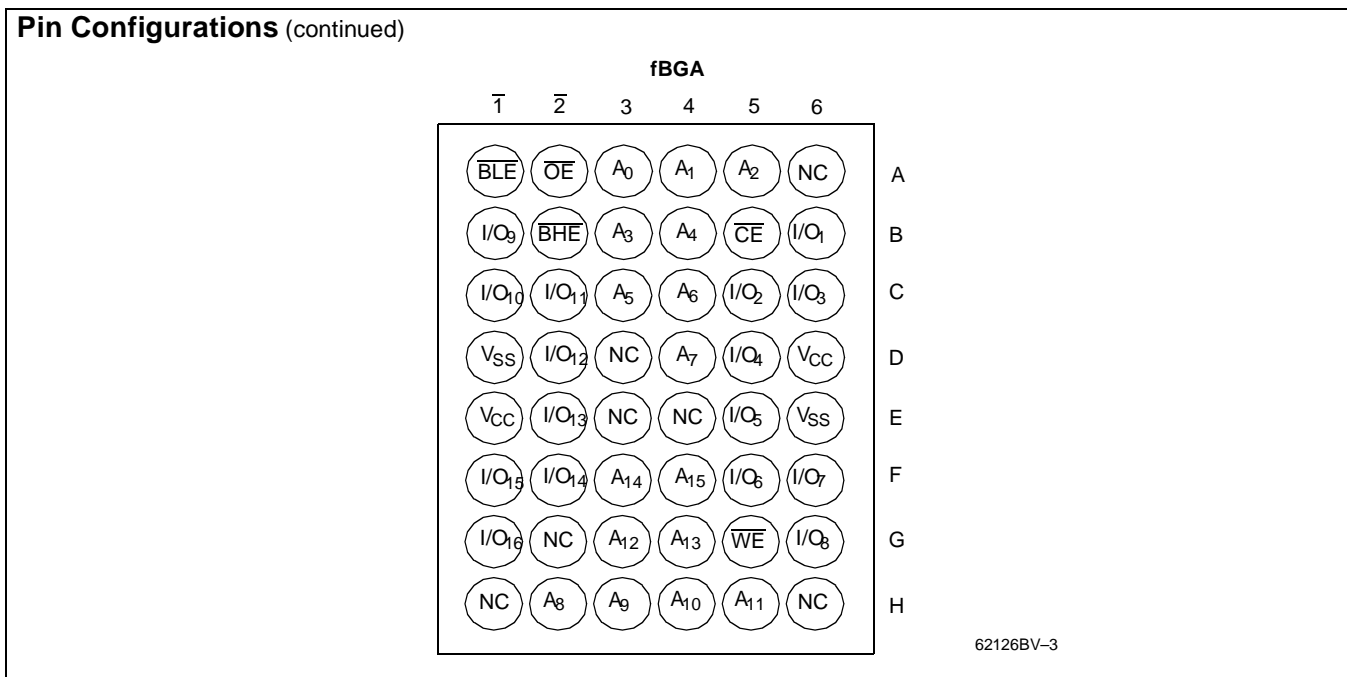
( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the write enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY62126BV is available in standard 44-pin TSOP Type II (forward pinout) and fBGA packages.




**Selection Guide**

	CY62126BV-55	CY62126BV-70	Units
Maximum Access Time	55	70	ns
Maximum Operating Current	20	15	mA
Maximum CMOS Standby Current	15	15	μA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> ..... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

**Notes:**

1. V<sub>L</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
2. T<sub>A</sub> is the "Instant On" case temperature.

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

**Operating Range**

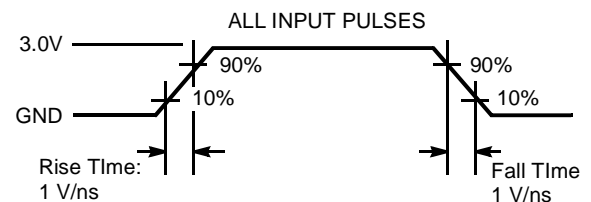
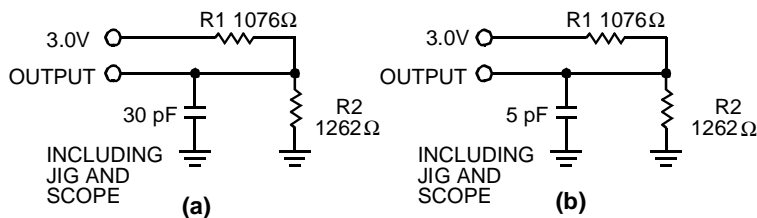
Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V-3.6V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	62126BV			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.2			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3		0.4	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	55 ns		20	mA
			70 ns		15	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>			2	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0		0.5	15	μA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	9	pF
C <sub>OUT</sub>	Output Capacitance		9	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT



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**Notes:**

- Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T<sub>A</sub> = 25°C, V<sub>CC</sub>=3.0V). Parameters are guaranteed by design and characterization, and not 100% tested.
- Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

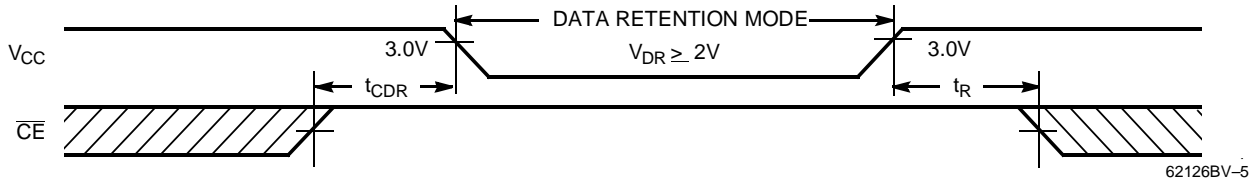
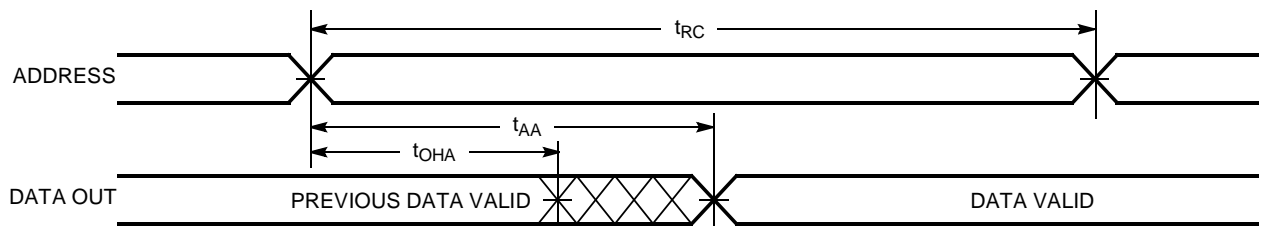
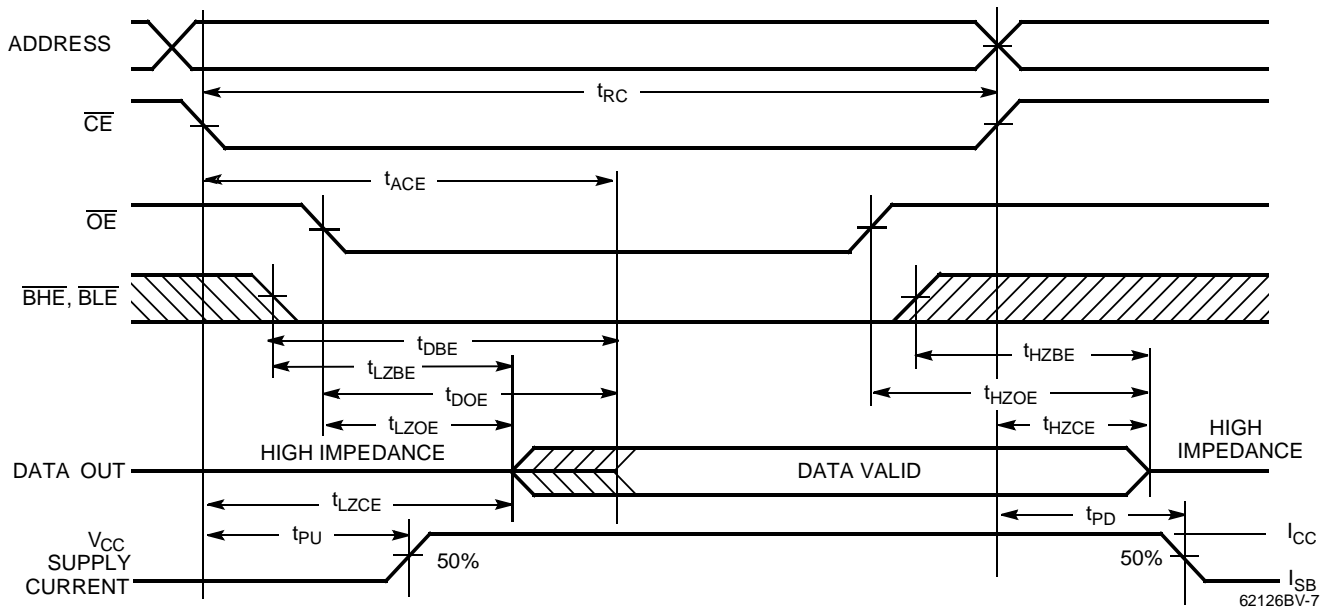
Parameter	Description	62126BV-55		62126BV-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		55		70	ns
$t_{DBE}$	Byte Enable to Data Valid		25		35	ns
$t_{LZBE}$	Byte Enable to LOW Z <sup>[7]</sup>	5		5		ns
$t_{HZBE}$	Byte Disable to HIGH Z <sup>[6, 7]</sup>		20		25	ns
<b>WRITE CYCLE<sup>[8]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-Up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25		25	ns
$t_{BW}$	Byte Enable to End of Write	45		60		ns

**Notes:**

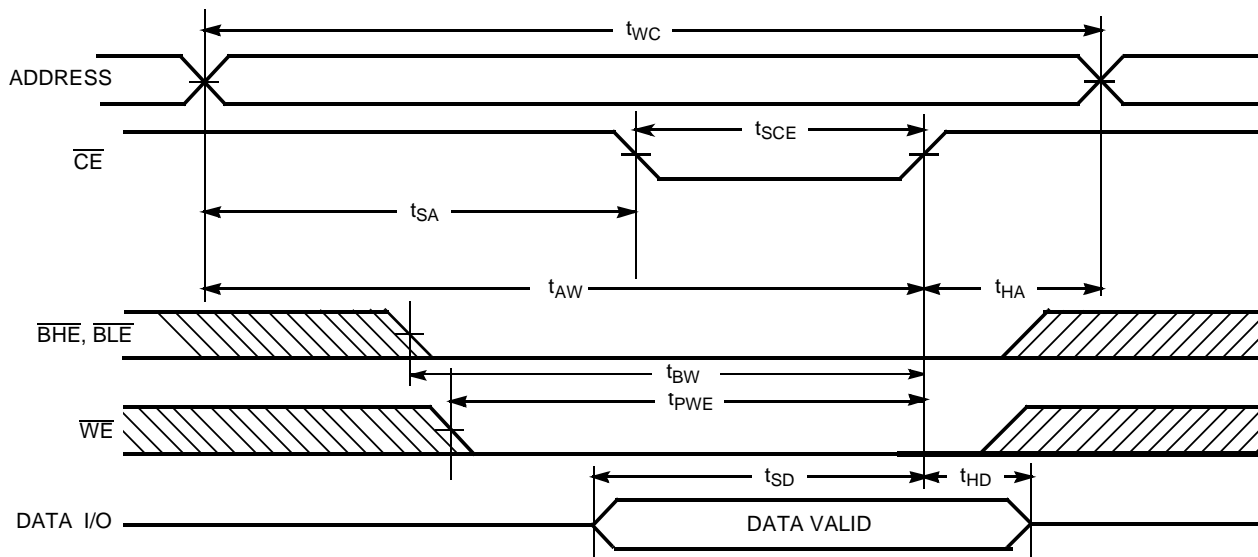
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ , and  $t_{HZBE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ ,  $t_{HZWE}$  is less than  $t_{LZWE}$ , and  $t_{HZBE}$  is less than  $t_{LZBE}$ , for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write. Refer to truth table for further conditions from BHE and BLE.

**Data Retention Characteristics** (Over the Operating Range for "L" and "LL" version only)

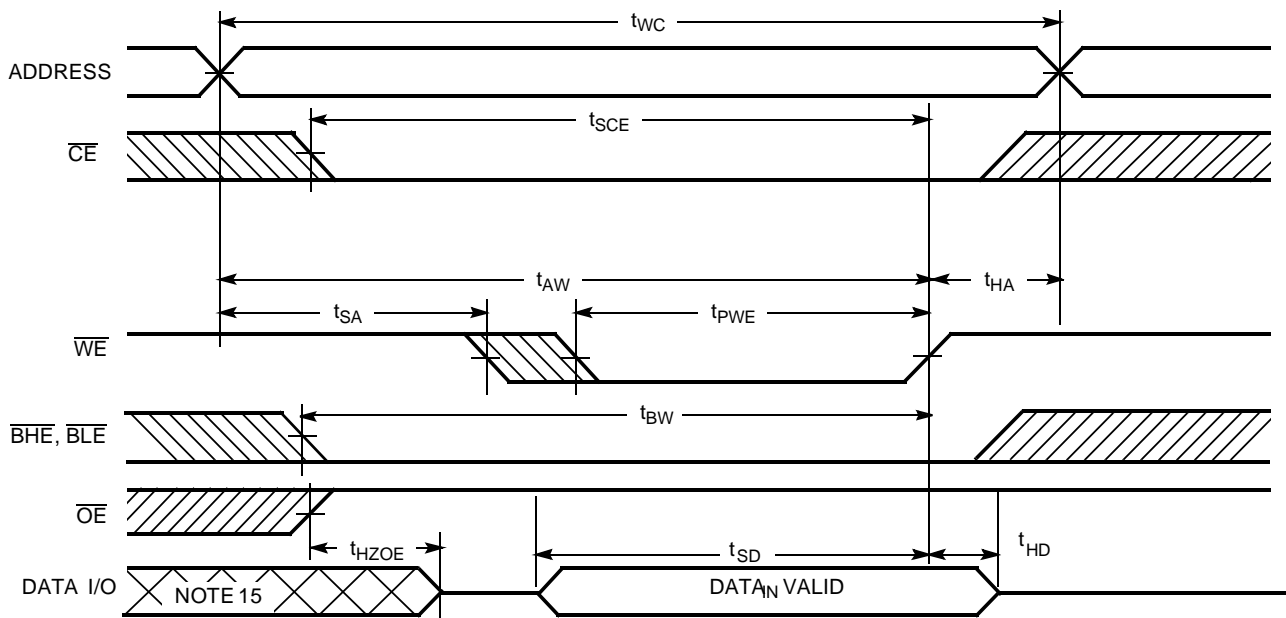
Parameter	Description	Conditions <sup>[9]</sup>	Min.	Typ	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		3.6	V
$I_{CCDR}$	Data Retention Current	$V_{CC}=V_{DR}=2.0V$ , $CE \geq V_{CC} - 0.3V$ ,		0.5	15	$\mu A$
$t_{CDR}$ <sup>[4]</sup>	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$	0			ns
$t_R$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No.1<sup>[10, 11]</sup>**

**Read Cycle No. 2 (OE Controlled)<sup>[11, 12, 13]</sup>**

**Notes:**

9. No input may exceed  $V_{CC} + 0.3V$ .
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$  and  $\overline{BLE} = V_{IH}$ .

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[13, 14]</sup>**


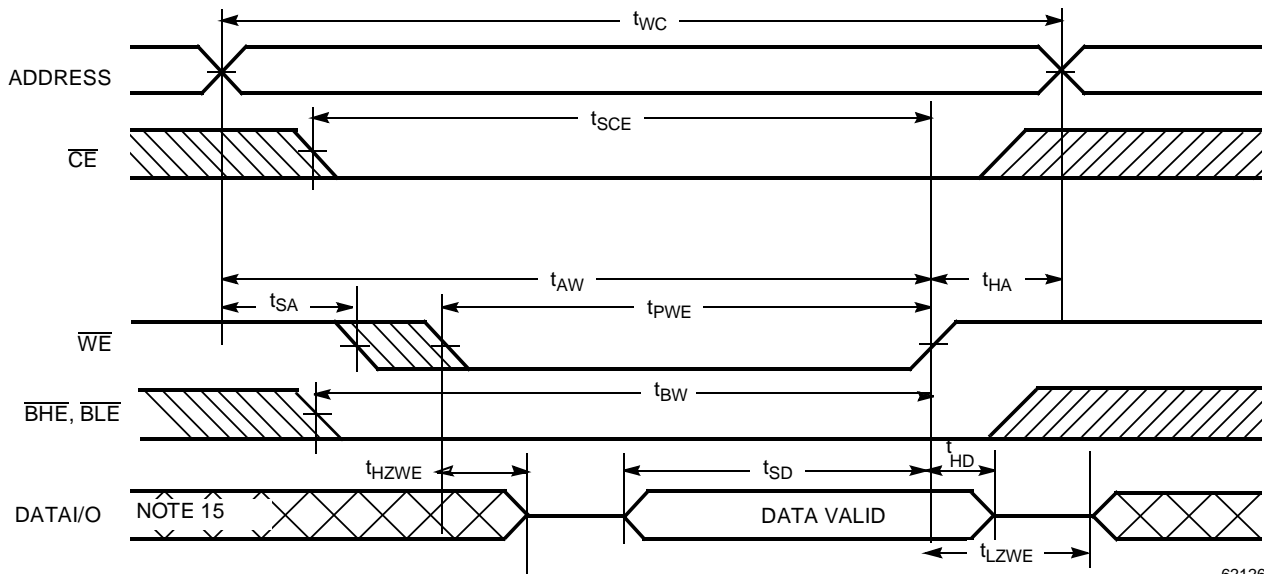
62126BV-8

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**


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**Notes:**

14. If  $\overline{CE}$ ,  $\overline{BHE}$ , or  $\overline{BLE}$  go HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13, 14]</sup>**


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**Truth Table**

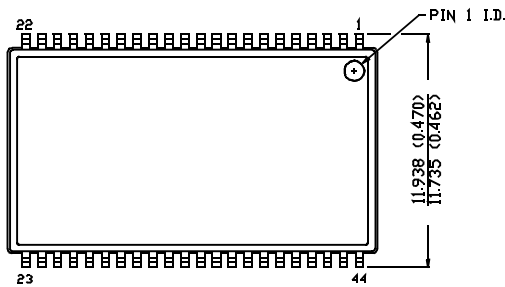
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read All bits	Active ( $I_{CC}$ )
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active ( $I_{CC}$ )
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write All bits	Active ( $I_{CC}$ )
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active ( $I_{CC}$ )
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

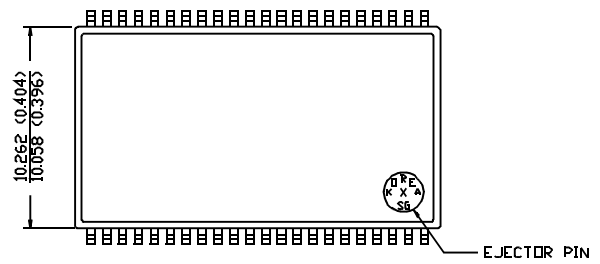
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62126BVLL-55ZI	Z44	44-Lead TSOP II	Industrial
	CY62126BVLL-55BAI	BA48	48-ball Fine Pitch Ball Grid Array	
70	CY62126BVLL-70ZI	Z44	44-Lead TSOP II	
	CY62126BVLL-70BAI	BA48	48-ball Fine Pitch Ball Grid Array	

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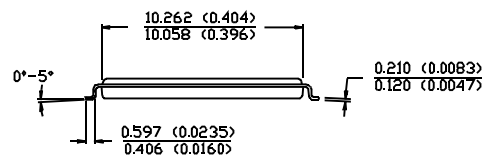
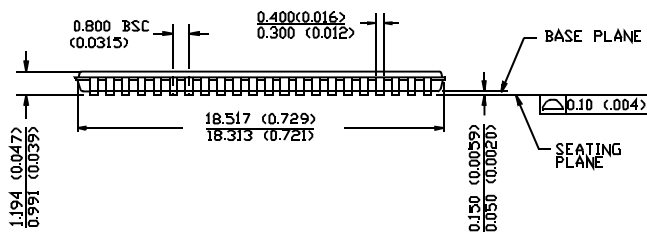
**Package Diagrams**
**44-Pin TSOP II Z44**

 DIMENSION IN MM (INCH)  
 MAX  
 MIN


TOP VIEW



BOTTOM VIEW

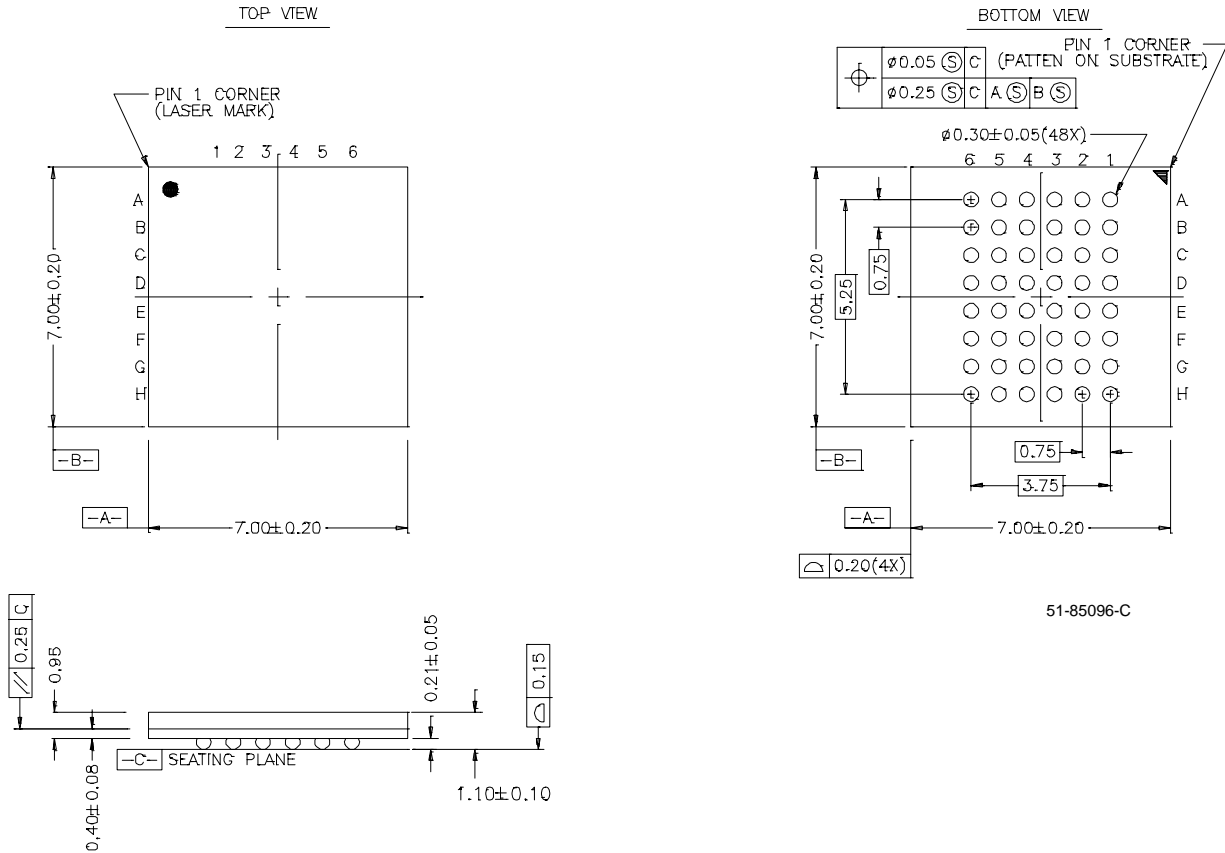


51-85087-A



Package Diagrams (continued)

48-Ball (7.00 mm x 7.00 mm) FBGA BA48



51-85096-C