



# 1 Mb (128K x 8) Static RAM

## Features

- Very high speed: 55 and 70 ns
- Wide voltage range: 2.2V to 3.6V
- Pin compatible with CY62128V
- Ultra-low active power
  - Typical active current: 0.85 mA @ f = 1 MHz
  - Typical active current: 5 mA @ f = f<sub>MAX</sub>
- Ultra-low standby power
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- Packages offered in a 32-lead SOIC, a 32-lead TSOP, a 32-lead Short TSOP, and a 32-lead Reverse TSOP

## Functional Description<sup>[1]</sup>

The CY62128DV30 is a high-performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

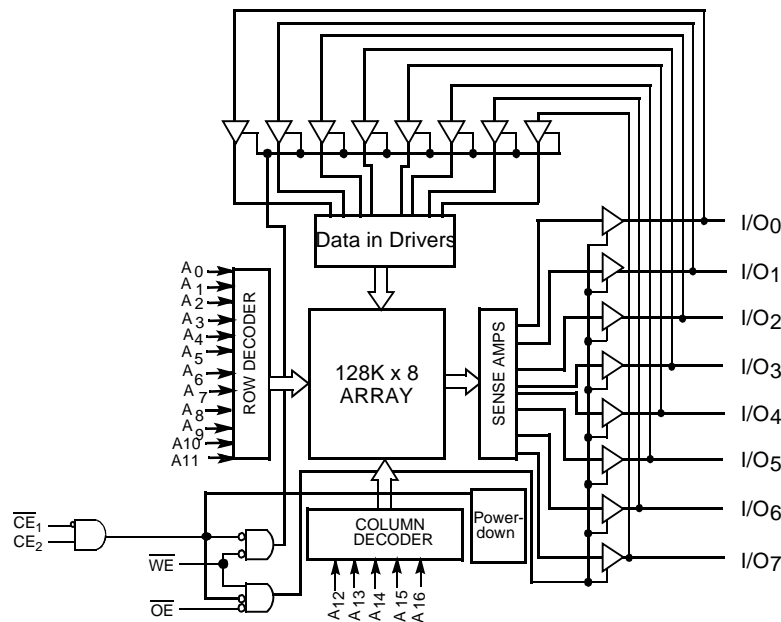
power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $CE_2$ ) LOW. The input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when: deselected Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $CE_2$ ) LOW, outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation (Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 ( $CE_2$ ) HIGH and Write Enable (WE) LOW).

Writing to the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) LOW with Chip Enable 2 ( $CE_2$ ) HIGH and Write Enable (WE) LOW. Data on the eight I/O pins is then written into the location specified on the Address pin (A<sub>0</sub> thro. A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) LOW with Chip Enable 2 ( $CE_2$ ) HIGH and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH) or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH), and WE LOW).

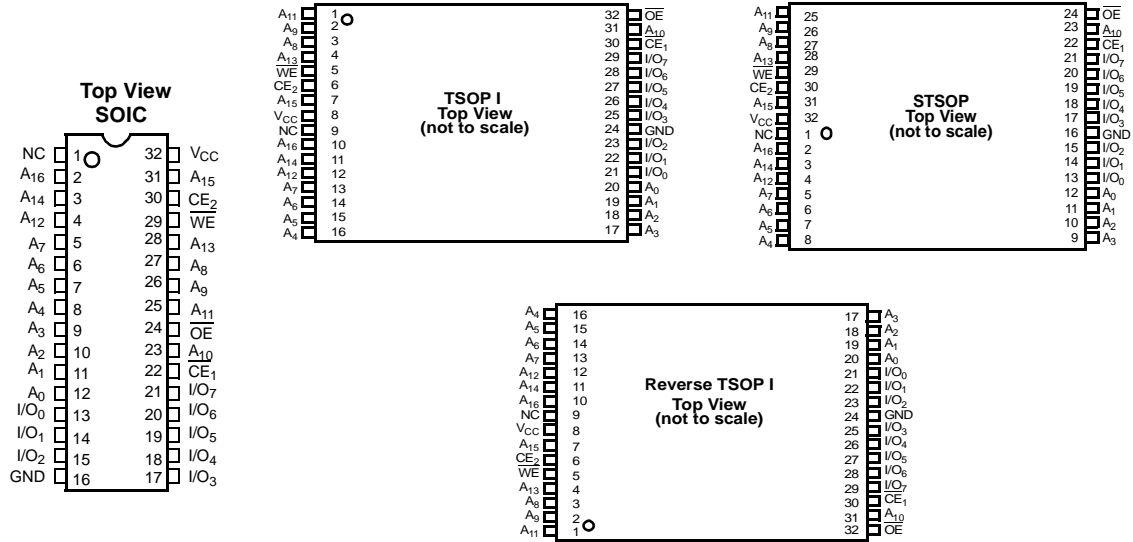
## Logic Block Diagram



**Note:**

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**



**Note:**

- 2. NC pins are not connected to the die.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.3V to 3.9V
- DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup>..... -0.3V to V<sub>CC</sub> + 0.3V

- DC Input Voltage<sup>[3]</sup> ..... -0.3V to V<sub>CC</sub> + 0.3V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current ..... > 200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub> <sup>[4]</sup>
Industrial	-40°C to +85°C	2.2V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating, I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (µA)	
	Min.	Typ.	Max.		f = 1 MHz		f = f <sub>MAX</sub>			
					Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.
CY62128DV30L	2.2	3.0	3.6	55/70	0.85	1.5	5	10	1.5	5
CY62128DV30LL				55/70	0.85	1.5	5	10	1.5	4

**DC Electrical Characteristics** (Over the Operating Range)

Parameter	Description	Test Conditions		CY62128DV30-55/70			Unit
				Min.	Typ. <sup>[5]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0			V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4			
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA			0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA			0.4	
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8		V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2		V <sub>CC</sub> + 0.3	
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3		0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3		0.8	
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	µA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0mA, CMOS level		5	10	mA
		f = 1 MHz			0.85	1.5	
I <sub>SB1</sub>	Automatic CE Power-down Current – CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE,)		L	1.5	5	µA
				LL	1.5	4	
I <sub>SB2</sub>	Automatic CE Power-down Current – CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V		L	1.5	5	µA
				LL	1.5	4	

**Capacitance<sup>[6]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

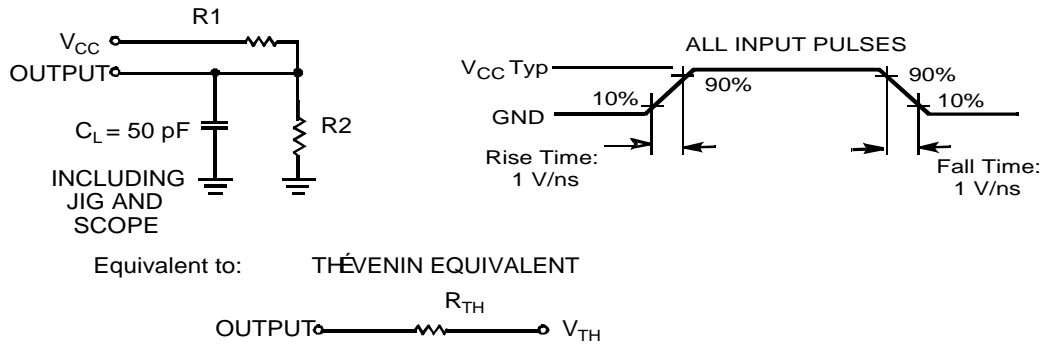
**Notes:**

3. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns., V<sub>IH(max.)</sub> = V<sub>CC</sub>+0.75V for pulse durations less than 20 ns.
4. Full device operation requires linear ramp of V<sub>CC</sub> from 0V to V<sub>CC(min)</sub> and V<sub>CC</sub> must be stable at V<sub>CC(min)</sub> for 500 µs.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
6. Tested initially and after any design or proces changes that may affect these parameters.

**Thermal Resistance**

Parameter	Description	Test Conditions	SOIC	TSOP I	STSOP	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient) <sup>[6]</sup>	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	69	93	65	°C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case) <sup>[6]</sup>		34	17	15	°C/W

**AC Test Loads and Waveforms**

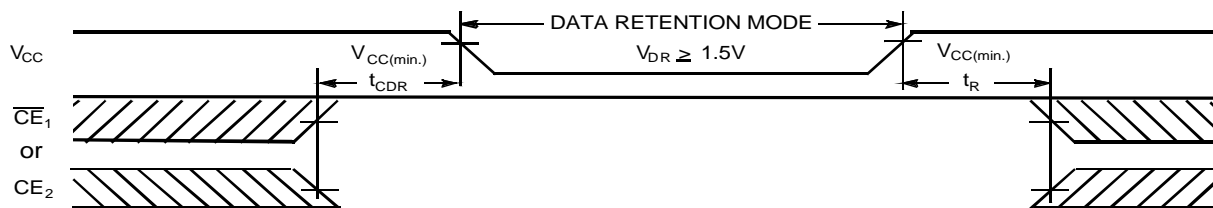


Parameters	2.5V (2.2 – 2.7V)	3.0V (2.7 – 3.6V)	Unit
R1	16600	1103	$\Omega$
R2	15400	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.2	1.75	V

**Data Retention Characteristics**

Parameter	Description	Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5\text{V}$ , $CE_1 \geq V_{CC} - 0.2\text{V}$ , $CE_2 \leq 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$			4	$\mu\text{A}$
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		100			$\mu\text{s}$

**Data Retention Waveform**



**Note:**

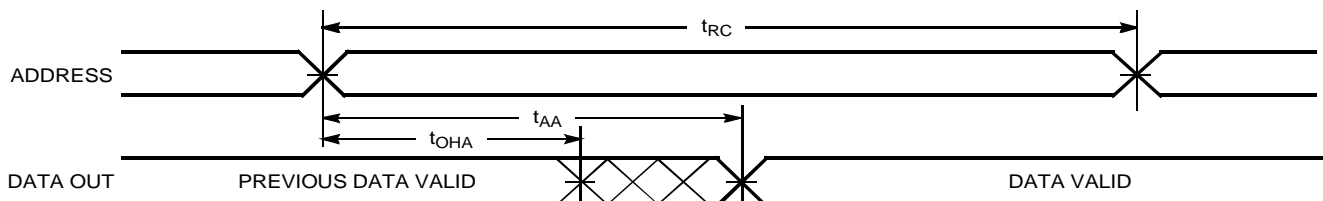
7. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} > 100 \text{ us}$ .

**Switching Characteristics** (Over the Operating Range)<sup>[8]</sup>

Parameter	Description	CY62128DV30-55		CY62128DV30-70		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9,10]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Low Z <sup>[9]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z <sup>[9,10]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Power-up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power-down		55		70	ns
<b>Write Cycle<sup>[11]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Write End	40		60		ns
$t_{AW}$	Address Set-up to Write End	40		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	WE Pulse Width	40		50		ns
$t_{SD}$	Data Set-up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	WE LOW to High Z <sup>[9,10]</sup>		20		25	ns
$t_{LZWE}$	WE HIGH to Low Z <sup>[9]</sup>	10		10		ns

**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[12, 13]</sup>**

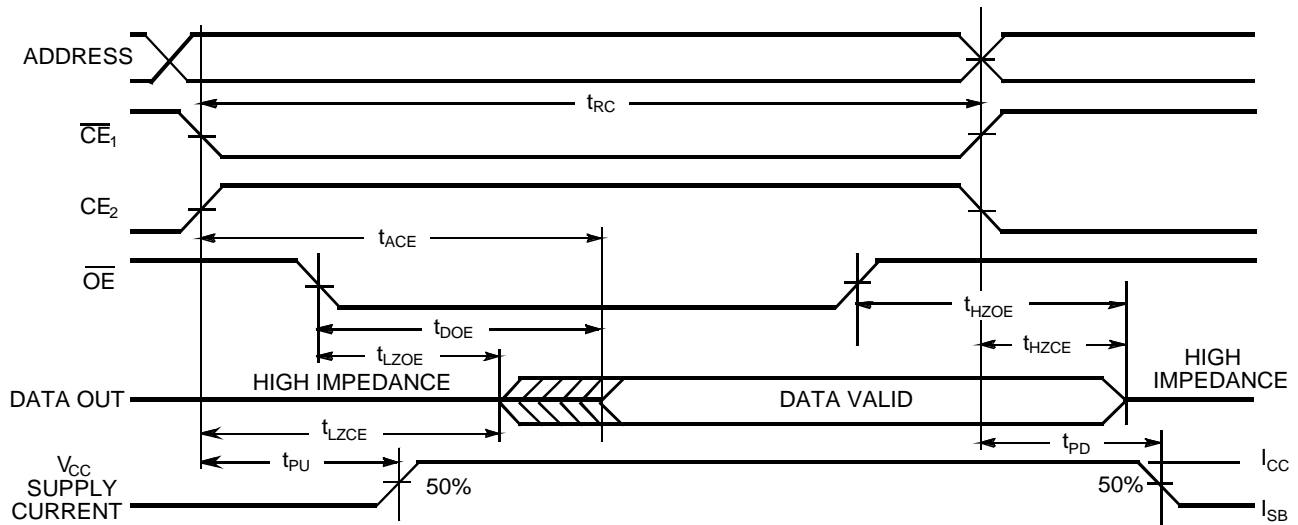


**Notes:**

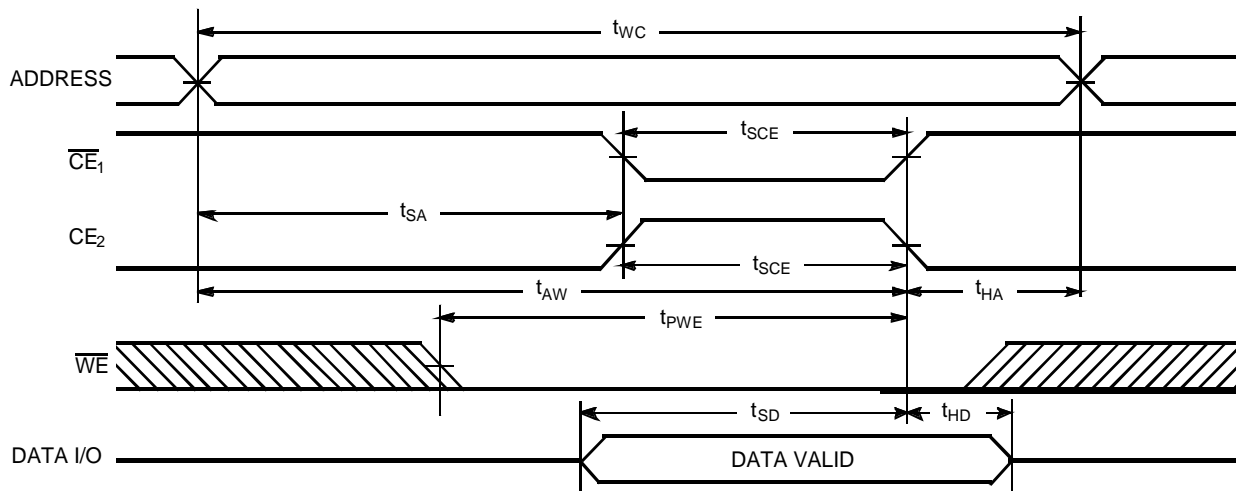
8. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}$ .
9. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ .
10.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
11. The internal write time of the memory is defined by the overlap of WE,  $CE_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals.
12. Device is continuously selected.  $\overline{OE}$ ,  $CE_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
13. WE is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ( $\overline{OE}$  Controlled) [10, 13, 14]



Write Cycle No. 1 ( $\overline{WE}$  Controlled) [11, 15, 16, 17]

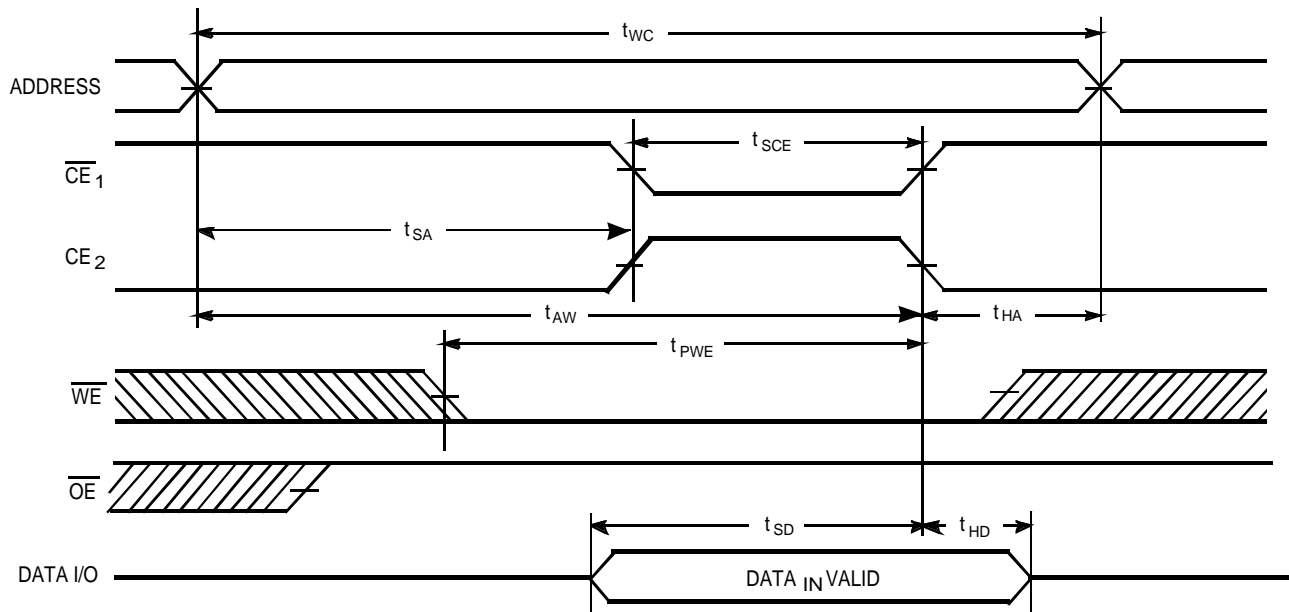


Notes:

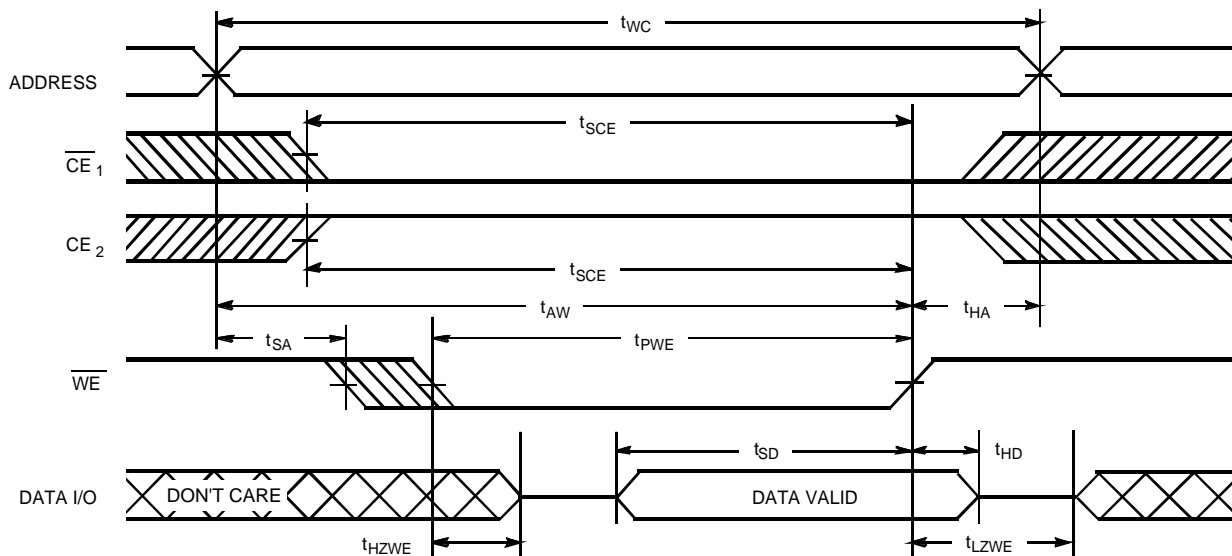
14. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
15. Data I/O is high-impedance if  $OE = V_{IH}$ .
16. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
17. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{CE}_{1</>1</>}$  or  $\overline{CE}_{2</>2</>}$  Controlled)** [11, 15, 16, 17]



**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [10, 16, 17]



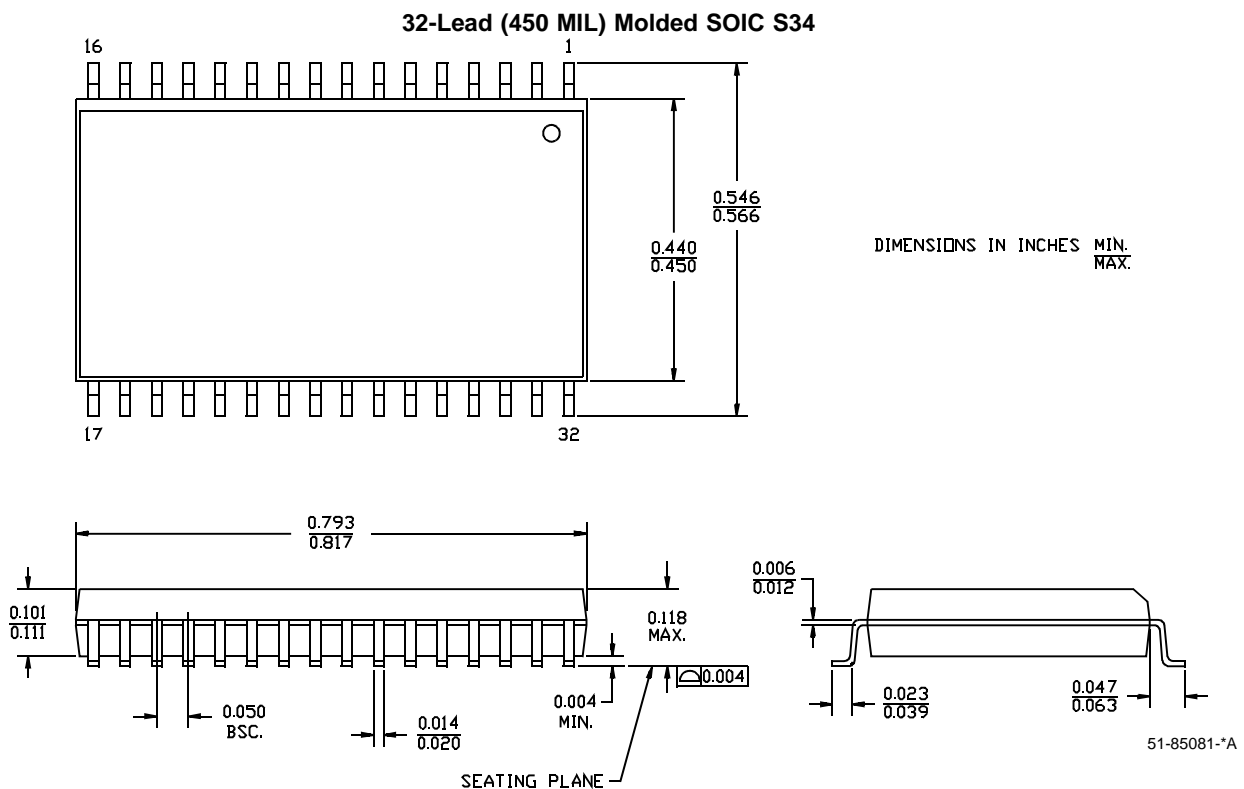
**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	Data In	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128DV30L-55SI	S34	32-lead SOIC	Industrial
	CY62128DV30LL-55SI	S34	32-lead SOIC	
	CY62128DV30L-55ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30LL-55ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30L-55ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30LL-55ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30L-55ZRI	ZR32	32-lead Reverse TSOP Type 1	
	CY62128DV30LL-55ZRI	ZR32	32-lead Reverse TSOP Type 1	
70	CY62128DV30L-70SI	S34	32-lead SOIC	Industrial
	CY62128DV30LL-70SI	S34	32-lead SOIC	
	CY62128DV30L-70ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30LL-70ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30L-70ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30LL-70ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30L-70ZRI	ZR32	32-lead Reverse TSOP Type 1	
	CY62128DV30LL-70ZRI	ZR32	32-lead Reverse TSOP Type 1	

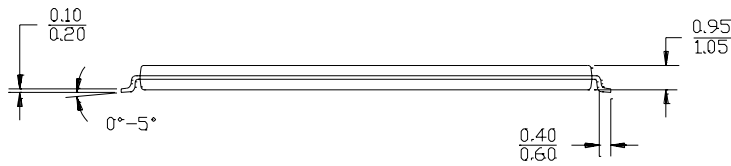
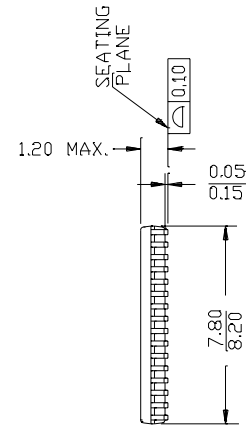
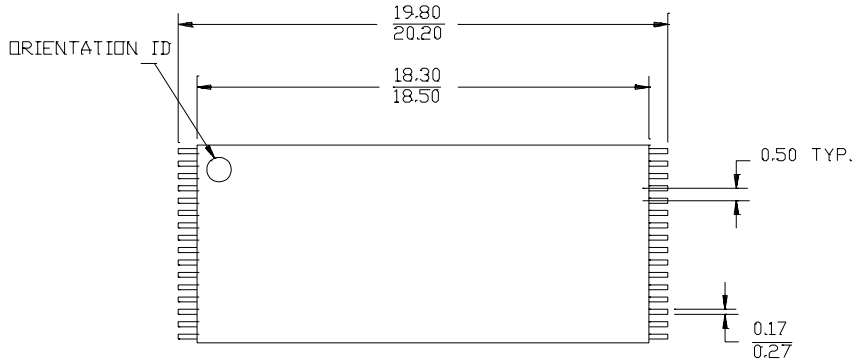
**Package Diagrams**





**32-Lead Thin Small Outline Package Type I (8 x 20 mm) Z32**

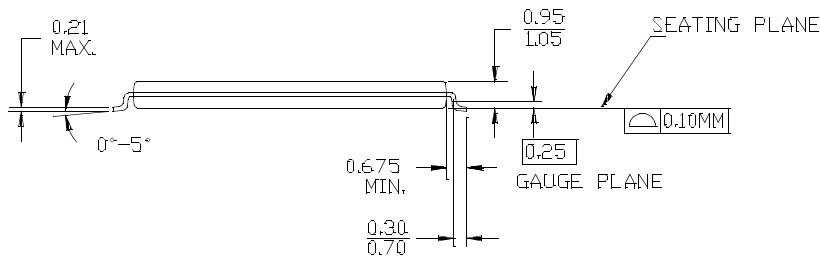
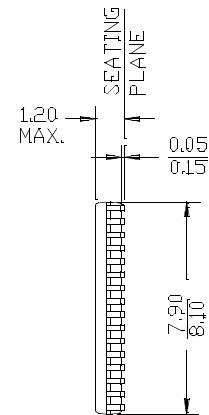
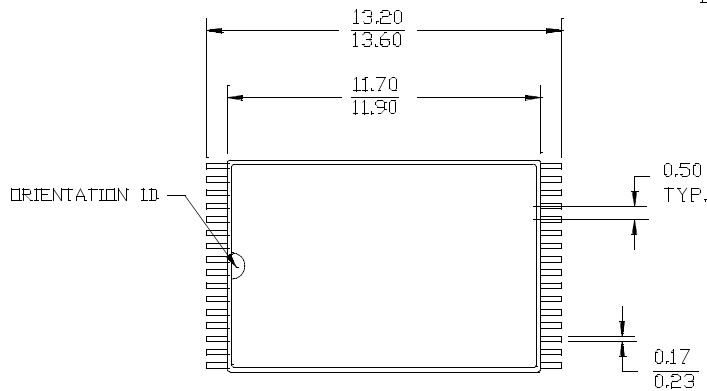
DIMENSION IN MM  
MIN.  
MAX.



51-85056-\*D

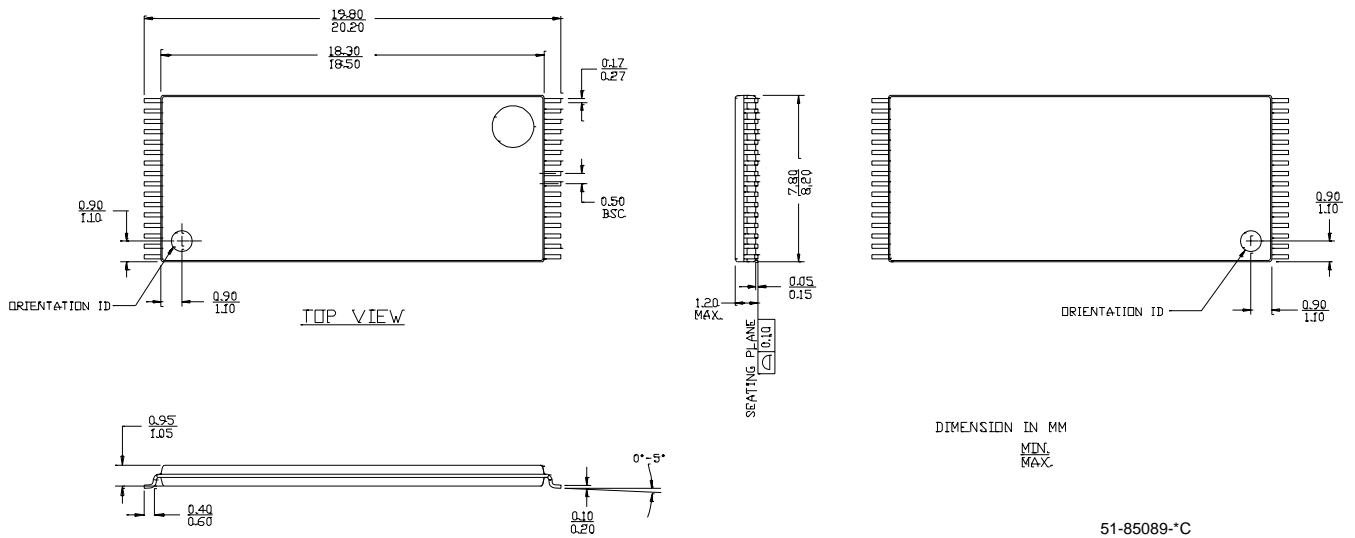
**32-Lead Shrunk Thin Small Outline Package (8 x 13.4 mm) ZA32**

DIMENSION IN MM  
MIN.  
MAX.



51-85094-\*D

32-Lead Reverse Thin Small Outline Package ZR32



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Document History Page

Document Title: CY62128DV30 MoBL® 1 Mb (128K x 8) Static RAM				
Document Number: 38-05231				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117691	08/27/02	JUI	New Data Sheet
*A	127314	5/27/03	MPR	Changed from Advance Information to Preliminary Changed Isb2 to 5 uA (L), 4 uA (LL) Changed lccdr to 4 uA (L), 3 uA (LL) Changed Cin from 6 pF to 8 pF
*B	128342	07/23/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129002	08/29/03	CDY	Changed lcc 1 MHz typ from 0.5 mA to 0.85 mA