

## 16-Bit Registered Transceivers

### Features

- FCT-E speed at 3.7 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

#### CY74FCT16952T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162952T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162H952T Features:

- Bus hold retains last active state

- Eliminates the need for external pull-up or pull-down resistors

### Functional Description

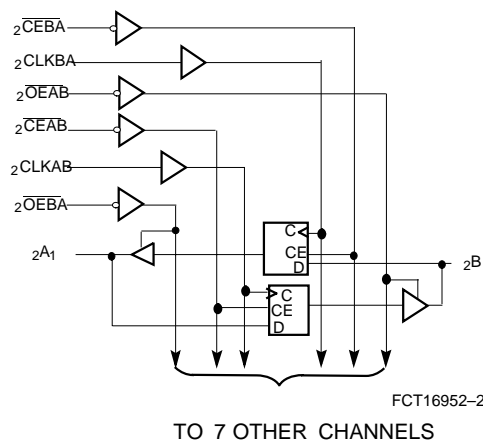
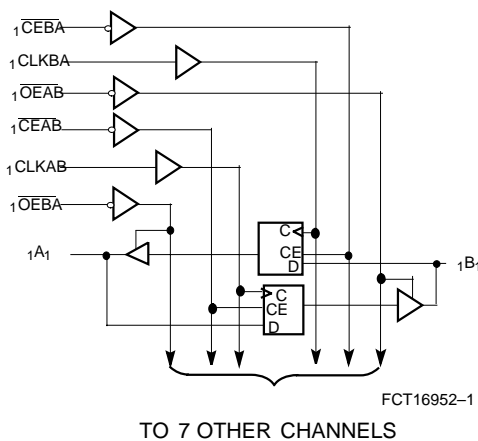
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B,  $\overline{CEAB}$  must be LOW to allow data to be stored when  $\text{CLKAB}$  transitions from LOW-to-HIGH. The stored data will be present on the output when  $\overline{OEAB}$  is LOW. Control of data from B-to-A is similar and is controlled by using the  $\overline{CEBA}$ ,  $\text{CLKBA}$ , and  $\overline{OEBA}$  inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

### Logic Block Diagrams



### Pin Configuration SSOP/TSSOP Top View

1 OEAB	1	56	1 OEBA
1 CLKBA	2	55	1 CLKBA
1 CEAB	3	54	1 CEBA
GND	4	53	GND
1A <sub>1</sub>	5	52	1B <sub>1</sub>
1A <sub>2</sub>	6	51	1B <sub>2</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A <sub>3</sub>	8	49	1B <sub>3</sub>
1A <sub>4</sub>	9	48	1B <sub>4</sub>
1A <sub>5</sub>	10	47	1B <sub>5</sub>
GND	11	46	GND
1A <sub>6</sub>	12	45	1B <sub>6</sub>
1A <sub>7</sub>	13	44	1B <sub>7</sub>
1A <sub>8</sub>	14	43	1B <sub>8</sub>
2A <sub>1</sub>	15	42	2B <sub>1</sub>
2A <sub>2</sub>	16	41	2B <sub>2</sub>
2A <sub>3</sub>	17	40	2B <sub>3</sub>
GND	18	39	GND
2A <sub>4</sub>	19	38	2B <sub>4</sub>
2A <sub>5</sub>	20	37	2B <sub>5</sub>
2A <sub>6</sub>	21	36	2B <sub>6</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A <sub>7</sub>	23	34	2B <sub>7</sub>
2A <sub>8</sub>	24	33	2B <sub>8</sub>
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

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**Pin Description**

Name	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Clock Enable Input (Active LOW)
CEBA	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs <sup>[1]</sup>
B	B-to-A Data Inputs or A-to-B Three-State Outputs <sup>[1]</sup>

**Function Table<sup>[2, 3]</sup>**

For A-to-B (Symmetric with B-to-A)

Inputs				Outputs
CEAB	CLKAB	OEAB	A	B
H	X	L	X	B <sup>[4]</sup>
X	L	L	X	B <sup>[4]</sup>
L	┌	L	L	L
L	└	L	H	H
X	X	H	X	Z

**Notes:**

- On the CY74FCT162H952T these pins have bus hold.
- A-to-B data flow is shown; B-to-A data flow is similar but uses, CEBA, CLKBA, and OEBA.
- H = HIGH Voltage Level.  
L = LOW Voltage Level.  
X = Don't Care.  
┌ = LOW-to-HIGH Transition.  
└ = HIGH Impedance.
- Level of B before the indicated steady-state input conditions were established.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

**Maximum Ratings<sup>[5, 6]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-55°C to +125°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage.....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....	-60 to +120 mA
Power Dissipation .....	1.0W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[8]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>		±1	μA
		Bus Hold			±100	
I <sub>IL</sub>	Input LOW Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =GND		±1	μA
		Bus Hold			±100	μA
I <sub>BBH</sub> I <sub>BBL</sub>	Bus Hold Sustain Current on Bus Hold Input <sup>[9]</sup>	V <sub>CC</sub> =Min.	V <sub>I</sub> =2.0V	-50		μA
			V <sub>I</sub> =0.8V	+50		μA
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus Hold Overdrive Current on Bus Hold Input <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>I</sub> =1.5V			TBD	mA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[10]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[10]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[11]</sup>			±1	μA

**Output Drive Characteristics for CY74FCT16952T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[10]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[10]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Capacitance<sup>[8]</sup>** (T<sub>A</sub> = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Note:**

7. Typical values are at V<sub>CC</sub>= 5.0V, T<sub>A</sub>= +25°C ambient.
8. This parameter is specified but not tested.
9. Pins with bus hold are described in the Pin Description.
10. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
11. Tested at +25°C.

**Power Supply Characteristics**

Parameter	Description	Test Conditions <sup>[12]</sup>		Typ. <sup>[7]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$	$V_{IN}\leq 0.2V$ $V_{IN}\geq V_{CC}-0.2V$	5	500	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$	$V_{IN}=3.4V$ <sup>[13]</sup>	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[14]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB or OEBA=GND	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	75	120	$\mu A/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[15]</sup>	$V_{CC}=\text{Max.}$ , $F_1=5\text{ MHz}$ , $F_0=10\text{ MHz}$ (CLKAB) OEAB = CEAB = GND OEBA = $V_{CC}$ 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.8	1.7	mA
			$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	1.3	3.2	
		$V_{CC}=\text{Max.}$ , $f_0=10\text{ MHz}$ (CLKAB) $f_1=2.5\text{ MHz}$ , OEAB = CEAB = GND OEBA = $V_{CC}$ 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	3.8	6.5 <sup>[16]</sup>	
			$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	8.3	20.0 <sup>[16]</sup>	

**Notes:**

12. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
13. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[17]</sup>

Parameter	Description	CY74FCT16952AT CY74FCT162952AT CY74FCT162H952AT		CY74FCT162952BT		Unit	Fig. No. <sup>[18]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKAB, CLKBA to B, A	2.0	10.0	2.0	7.5	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA, OEAB to A, B	1.5	10.5	1.5	8.0	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA, OEAB to A, B	1.5	10.0	1.5	7.5	ns	1, 7, 8
t <sub>SU</sub>	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA	2.5	—	2.5	—	ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA	2.0	—	1.5	—	ns	4
t <sub>SU</sub>	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	3.0	—	3.0	—	ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	2.0	—	2.0	—	ns	4
t <sub>W</sub>	Pulse Width HIGH or LOW CLKAB or CLKBA <sup>[19]</sup>	3.0	—	3.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[20]</sup>	—	0.5	—	0.5	ns	—

Parameter	Description	CY74FCT16952CT CY74FCT162H952CT		CY74FCT16952ET CY74FCT162952ET CY74FCT162H952ET		Unit	Fig. No. <sup>[18]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CLKAB, CLKBA to B, A	2.0	6.3	1.5	3.7	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA, OEAB to A, B	1.5	7.0	1.5	4.4	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA, OEAB to A, B	1.5	6.5	1.5	3.6	ns	1, 7, 8
t <sub>SU</sub>	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA	2.5	—	1.5	—	ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA	1.5	—	0	—	ns	4
t <sub>SU</sub>	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	3.0	—	2.0	—	ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	2.0	—	0	—	ns	4
t <sub>W</sub>	Pulse Width HIGH or LOW CLKAB or CLKBA <sup>[19]</sup>	3.0	—	3.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[20]</sup>	—	0.5	—	0.5	ns	—

**Notes:**

17. Minimum limits are specified but not tested on Propagation Delays.
18. See "Parameter Measurement Information" in the General Information section.
19. This parameter is specified but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16952**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.7	CY74FCT16952ETPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.3	CY74FCT16952CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
10.0	CY74FCT16952ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

**Ordering Information CY74FCT162952**

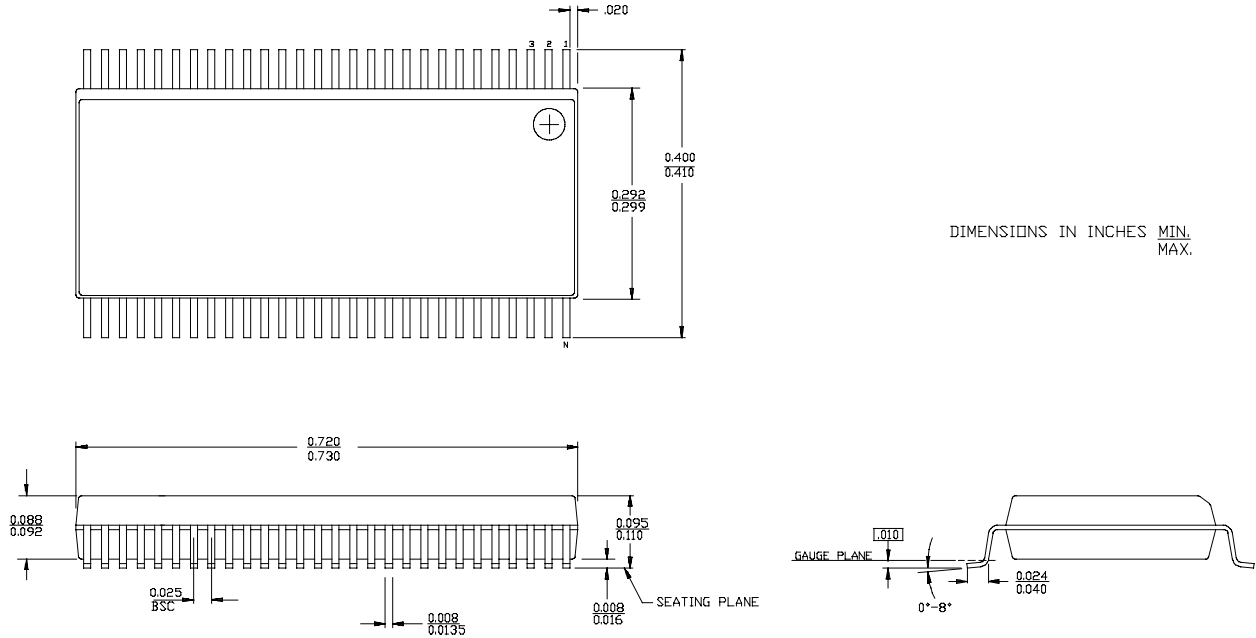
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.7	74FCT162952ETPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162952ETPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162952ETPVCT	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162952BTPVCT	O56	56-Lead (300-Mil) SSOP	
10.0	74FCT162952ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

**Ordering Information CY74FCT162H952**

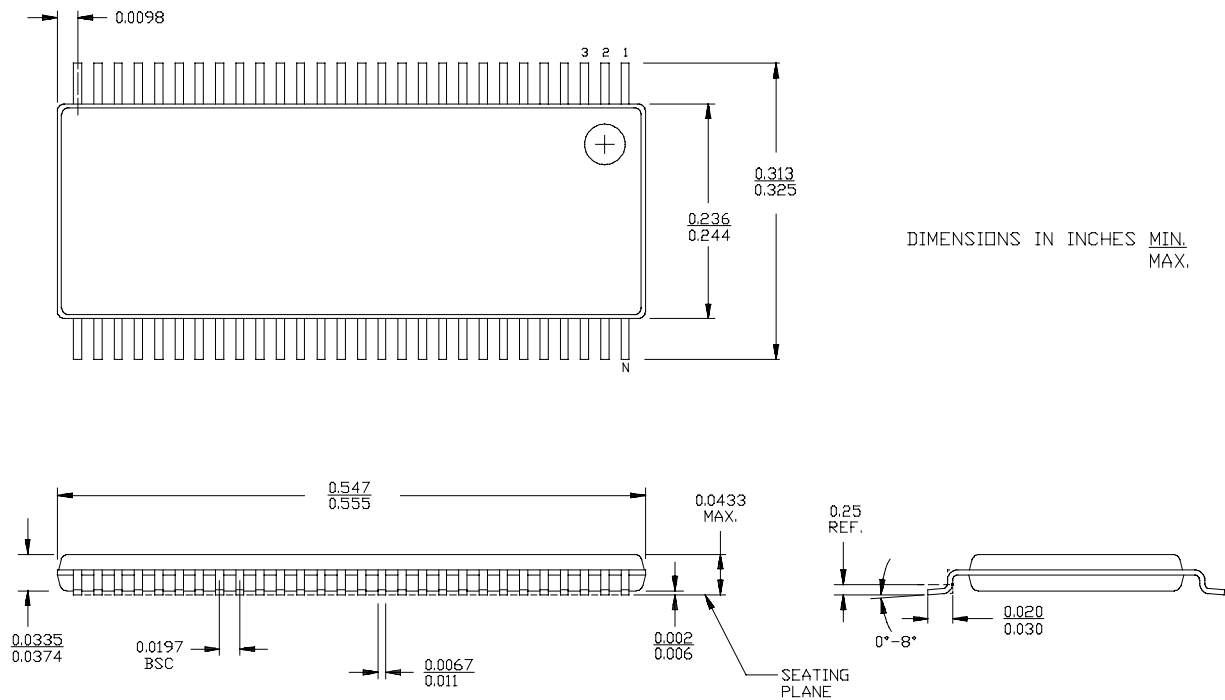
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.7	74FCT162H952ETPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
6.3	74FCT162H952CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
10.0	74FCT162H952ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

**Package Diagrams**

**56-Lead Shrunken Small Outline Package O56**



**56-Lead Thin Shrunken Small Outline Package Z56**



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