CY7C194B
CY7C195B

256 Kb (64K x 4) Static RAM

Features

- **Fast access time: 12 ns, 15 ns, and 25 ns**
- **Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Available in 24 DIP, 24 SOJ, 28 DIP, and 28 SOJ**

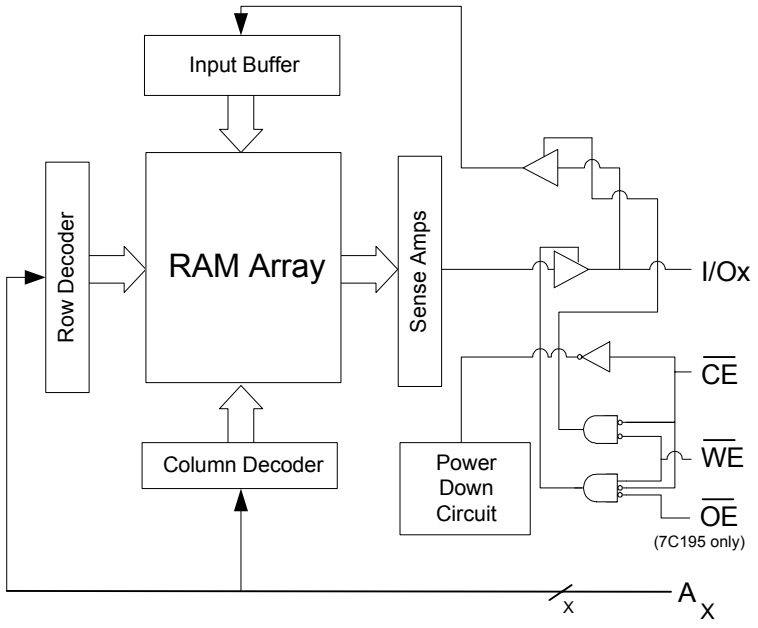
General Description[1]

The CY7C194B-CY7C195B is a high-performance CMOS Asynchronous SRAM organized as 64K × 4 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected. Output enable ($\overline{OE}$) is supported only in CY7C195B.[2]

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C194B-CY7C195B is available in 24 DIP, 24 SOJ, 28 DIP, and 28 SOJ package(s).

Logic Block Diagram



Product Portfolio

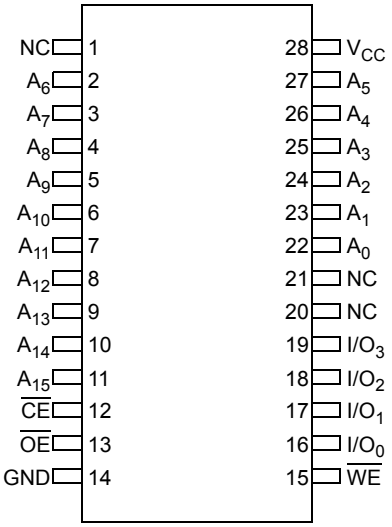
	12 ns	15 ns	25 ns	Unit
Maximum Access Time	12	15	25	ns
Maximum Operating Current	90	80	80	mA
Maximum CMOS Standby Current	10	10	10	mA

Notes:

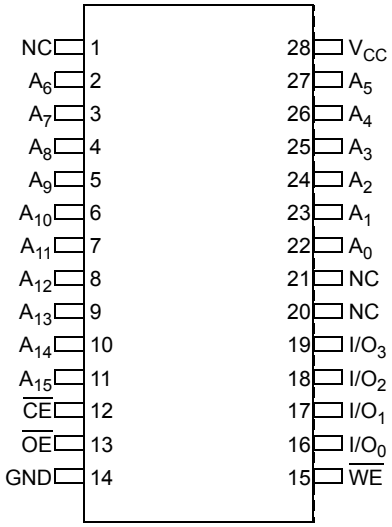
1. For best-practice recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.
2. All $\overline{OE}$-specific descriptions and parameters in this datasheet pertain to CY7C195 only.

Pin Layout and Specifications

CY7C195B 28 DIP (6.9 × 35.6 × 3.5 mm) – P21

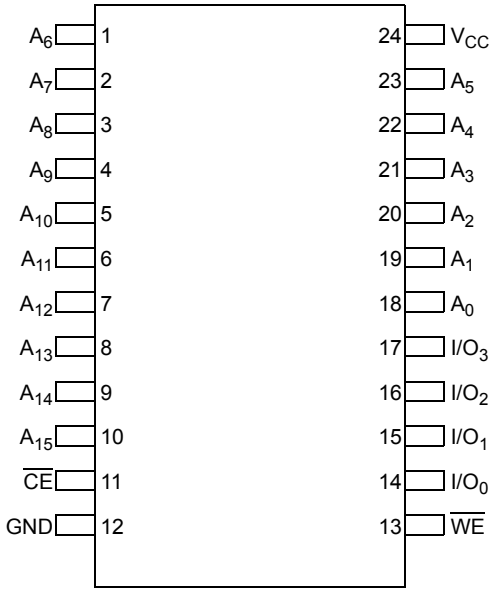


CY7C195B 28 SOJ (8 × 18 × 3.5 mm) – V21

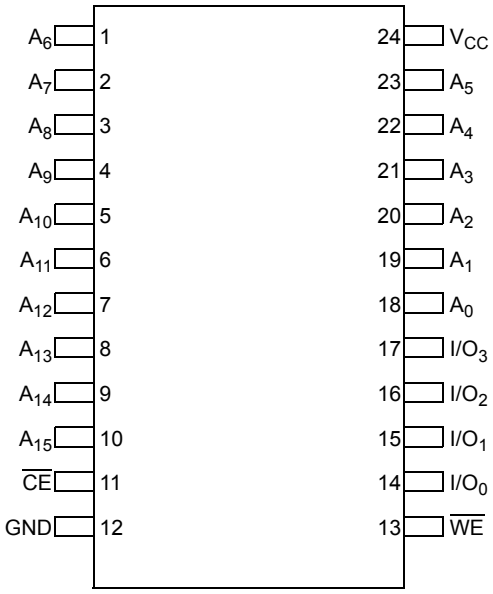


Pin Layout and Specifications (continued)

CY7C194B 24 SOJ (8 × 15 × 3.5 mm) – V13



CY7C194B 24 DIP (6.6 × 31.8 × 3.5 mm) – P13



Pin Description

Pin	Type	Description	28 DIP	24 DIP	24 SOJ	28 SOJ
A_X	Input	**Address Inputs**.	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 22, 23, 24, 25, 26, 27	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 22, 23, 24, 25, 26, 27
$\overline{CE}$	Control	**Chip Enable**.	12	11	11	12
I/O_X	Input or Output	**Data Input/Outputs**.	16, 17, 18, 19	14, 15, 16, 17	14, 15, 16, 17	16, 17, 18, 19
NC	–	**No Connect**. Pins are not internally connected to the die.	1, 20, 21	–	–	1, 20, 21
$\overline{OE}$	Control	**Output Enable (CY7C195 only)**.	13	–	–	13
V_{CC}	Supply	**Power (5.0V)**.	28	24	24	28
$\overline{WE}$	Control	**Write Enable**.	15	13	13	15

CY7C195B Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	X	High Z	Deselect / Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

CY7C194B Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_{AMB}	Ambient Temperature with Power Applied (i.e. case temperature)	–55 to +125	°C
V_{CC}	Core Supply Voltage Relative to V_{SS}	–0.5 to +7.0	V
V_{CC}	DC Voltage Applied to any Pin Relative to V_{SS}	–0.5 to V_{CC} + null	V
I_{OUT}	Output Short-Circuit Current	20	mA
V_{ESD}	Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0°C to 70°C	5.0V ± 10%

DC Electrical Characteristics[3]

Parameter	Description	Condition	12 ns		15 ns		25 ns		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.8	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., Ioh = -4.0 ma	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., Iol = 8.0 ma	–	0.4	–	0.4	–	0.4	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = 1 / t_{RC}	–	90	–	80	–	80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current TTL Inputs	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	30	–	30	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current CMOS Inputs	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ - 0.3v, $V_{IN} > V_{CC}$ - 0.3v or $V_{IN} \leq 0.3$,f = 0 Commercial	–	10	–	10	–	10	mA
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	–5	+5	uA
I_{IX}	Input Load Current	GND ≤ Vi ≤ V_{CC}	–5	+5	–5	+5	–5	+5	uA

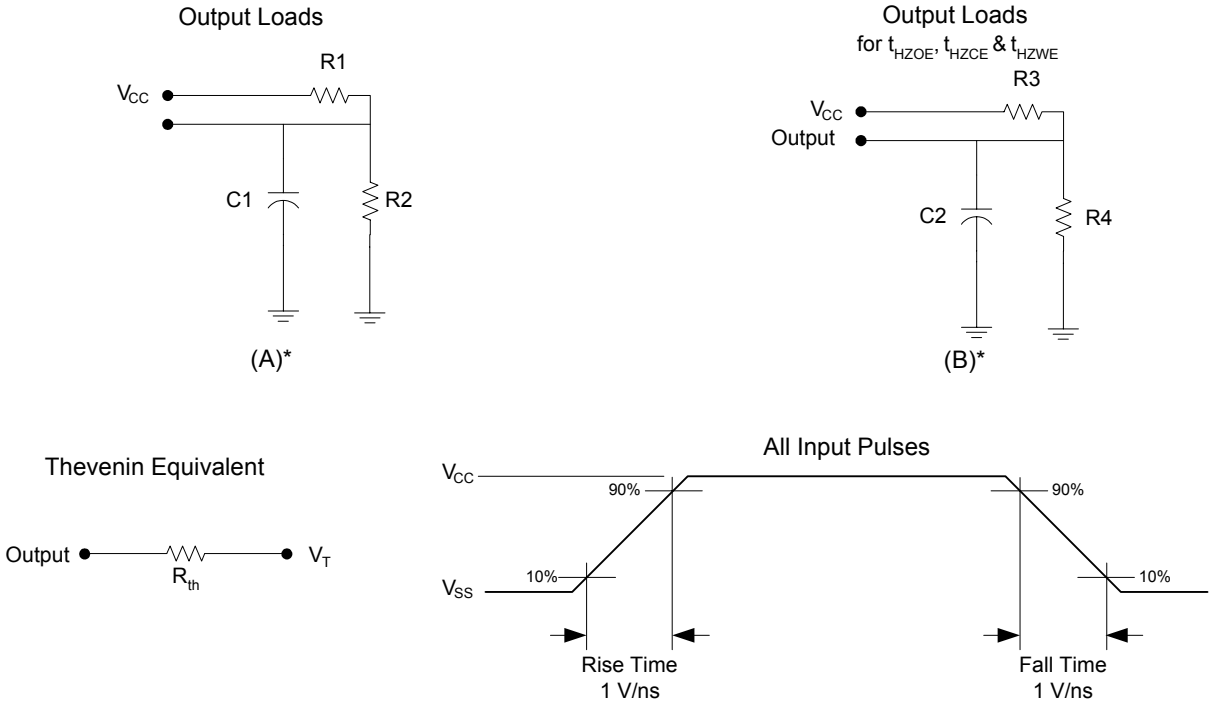
Capacitance[4]

Parameter	Description	Conditions	Max	Unit
			ALL - PACKAGES	
C_{IN}	Input Capacitance	T_A = 25C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		10	

Notes:

3. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Thermal Resistance[5]

Parameter	Description	Conditions	28 SOJ	24 SOJ	28 DIP	24 DIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	69	TBD	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		29.84	TBD	TBD	TBD	

Notes:

5. Test Conditions assume a transition time of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

AC Electrical Characteristics[2 6 7 8]

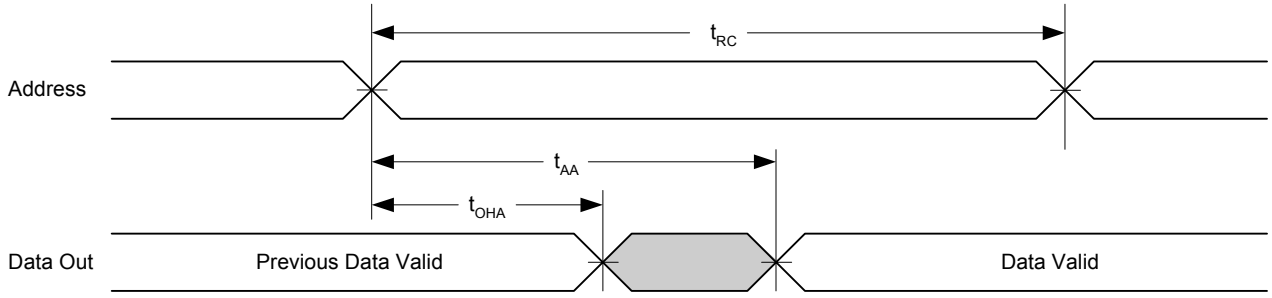
Parameter	Description	12 ns		15 ns		25 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12	–	15	–	25	–	ns
t_{AA}	Address to Data Valid	–	12	–	15	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	12	–	15	–	25	ns
t_{DOE}	$\overline{OE}$ to Data Valid	–	6	–	7	–	10	ns
t_{LZOE}	$\overline{OE}$ to Low Z	0	–	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ to High Z	–	5	–	7	–	10	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	7	–	10	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	12	–	15	–	25	ns
t_{WC}	Write Cycle Time	12	–	15	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	10	–	18	–	ns
t_{AW}	Address Set-up to Write End	9	–	10	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	8	–	9	–	18	–	ns
t_{SD}	Data Set-Up to Write End	7	–	8	–	10	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	6	–	7	-	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	3	–	3	–	ns

Notes:

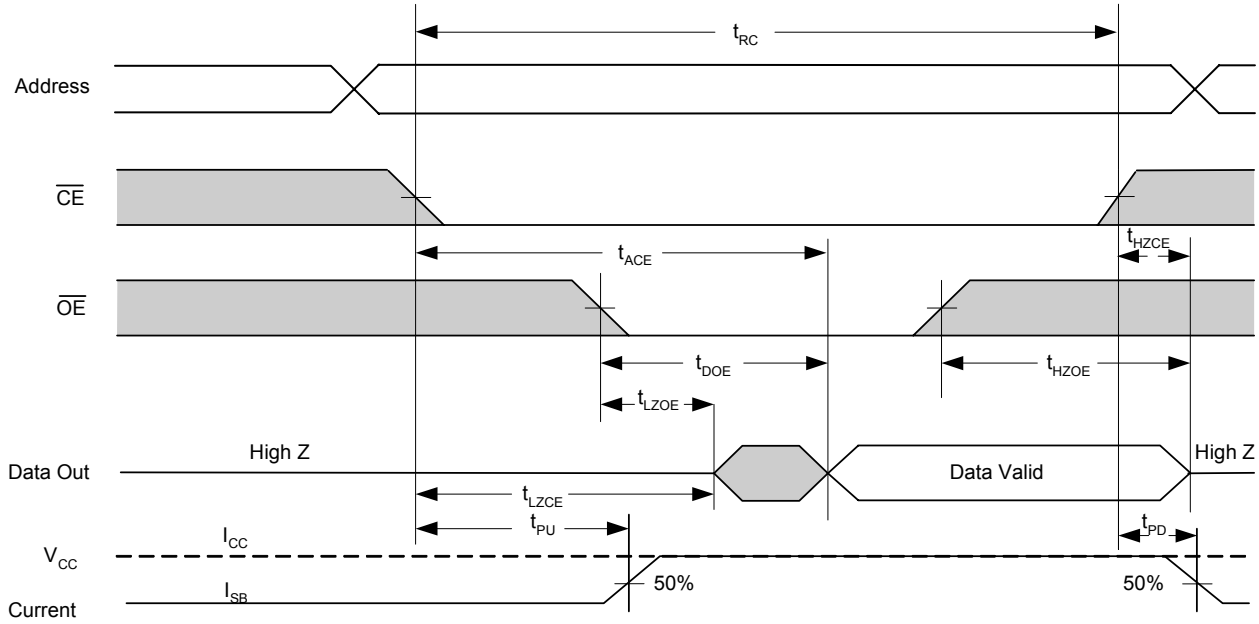
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage

Timing Waveforms

Read Cycle No. 1 [9, 10]



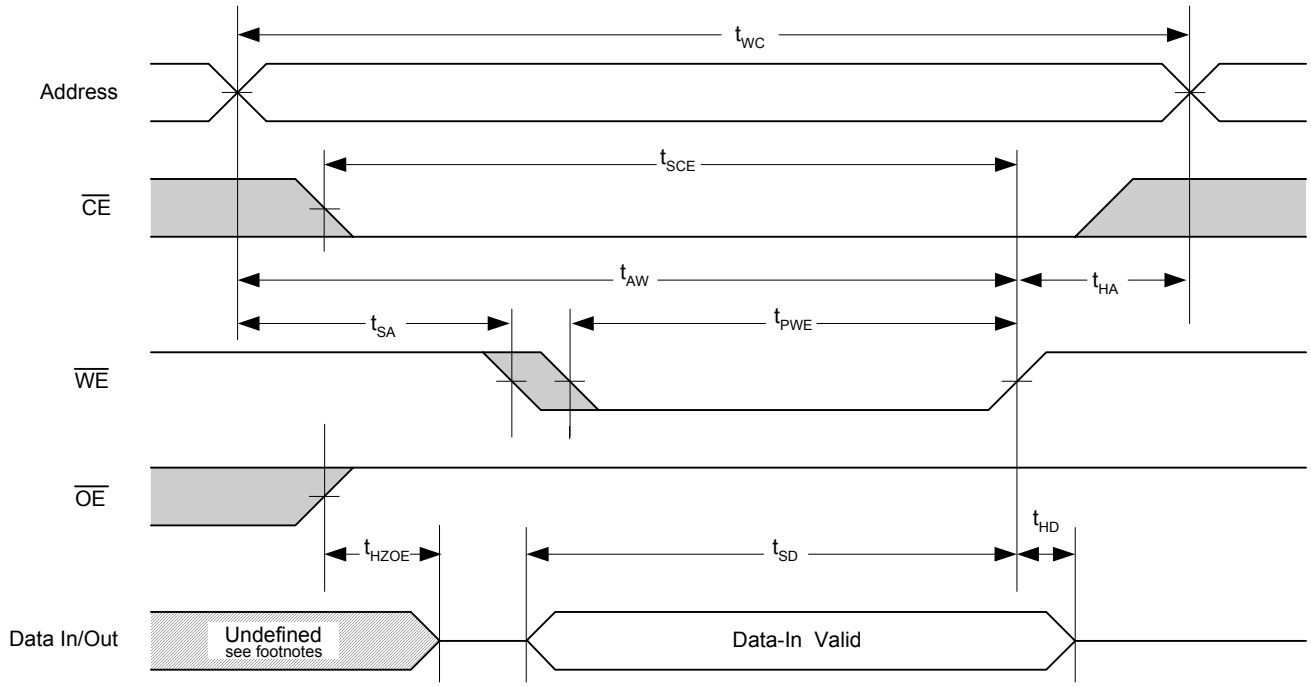
Read Cycle No. 2 [2, 11, 12]



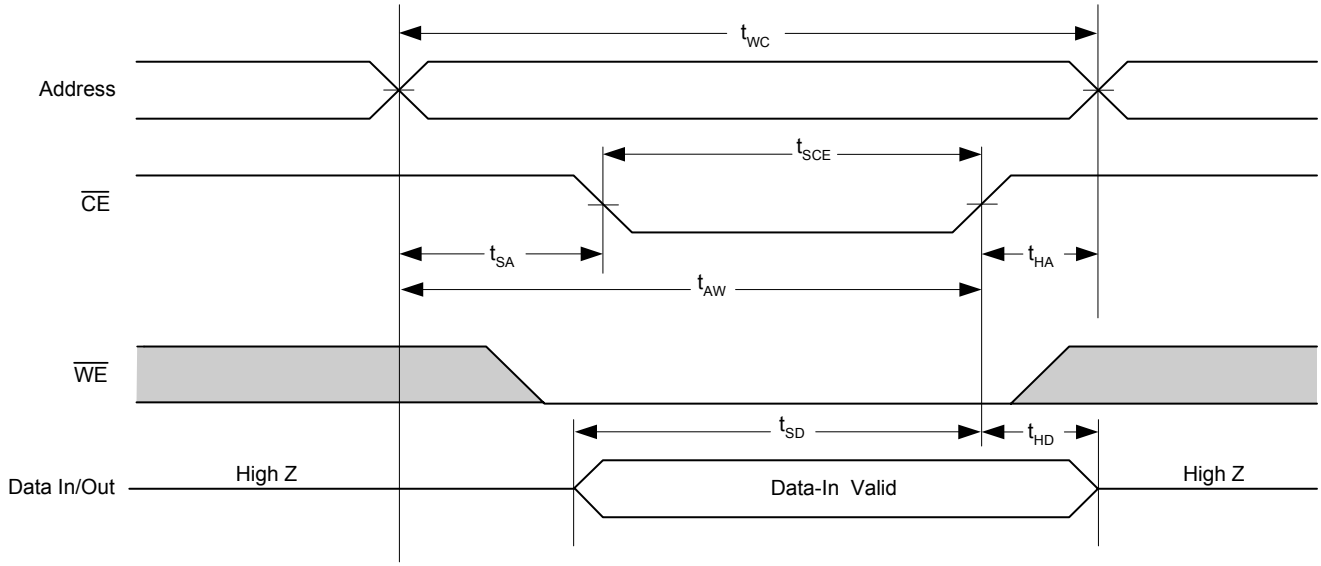
Notes:

9. Device is continuously selected. $\overline{OE}$ = V_{IL} = $\overline{CE}$.
10. $\overline{WE}$ is HIGH for Read Cycle.
11. This cycle is $\overline{OE}$ Controlled and $\overline{WE}$ is HIGH read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Write Cycle No. 1 ($\overline{WE}$ Controlled) [2, 13, 14, 15]



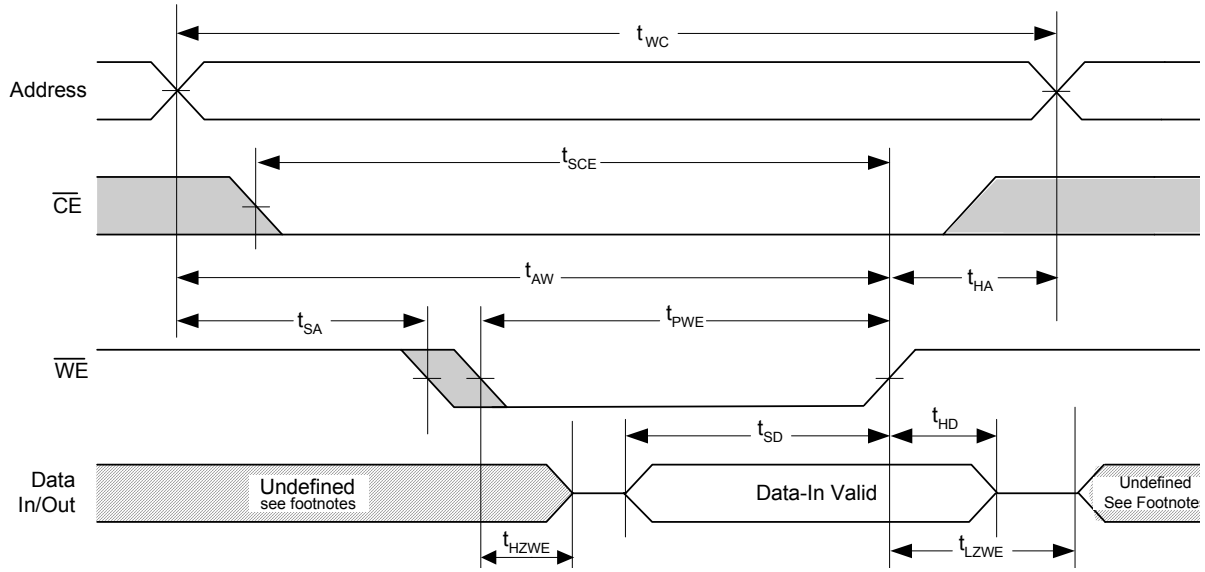
Write Cycle No. 2 ($\overline{CE}$ Controlled) [16, 17, 18]



Notes:

13. This cycle is $\overline{WE}$ controlled, $\overline{OE}$ is HIGH during write.
14. Data In/Out is high impedance if $\overline{OE}$ = V_{IH}.
15. During this period the I/Os are in output state and input signals should not be applied.
16. This cycle is $\overline{CE}$ controlled.
17. Data In/Out is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) [2, 19]



Ordering Information

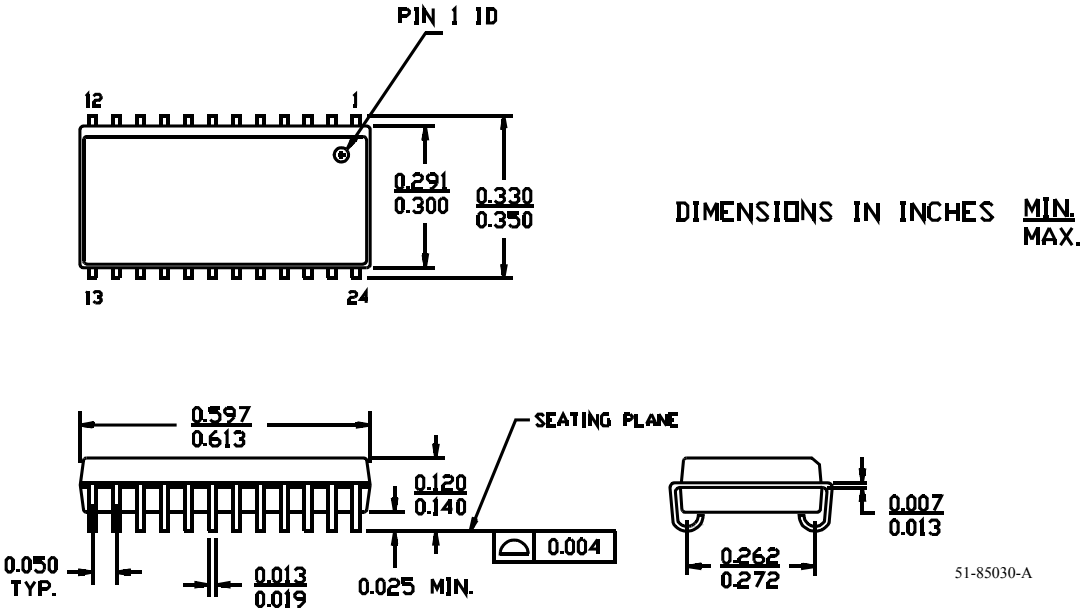
Speed	Ordering Code	Package Name	Package Type	Power Option	Operating Range
12 ns	CY7C195B-12VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Commercial
15 ns	CY7C194B-15PC	P13	24 DIP (6.6 x 31.8 x 3.5 mm)	Standard	Commercial
15 ns	CY7C194B-15VC	V13	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial
15 ns	CY7C195B-15VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Commercial
25 ns	CY7C194B-25VC	V13	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial
25 ns	CY7C195B-25PC	P21	28 DIP (6.9 x 35.6 x 3.5 mm)	Standard	Commercial

Notes:

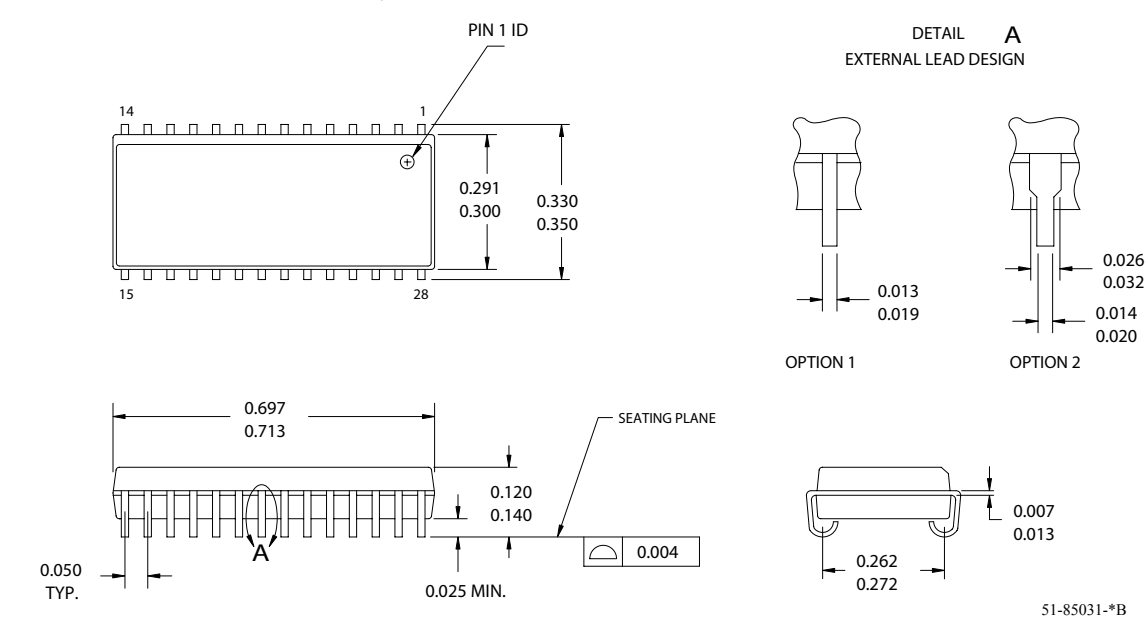
19. The cycle is $\overline{WE}$ controlled, $\overline{OE}$ low. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Package Diagram

24-Lead (300-Mil) Molded SOJ V13

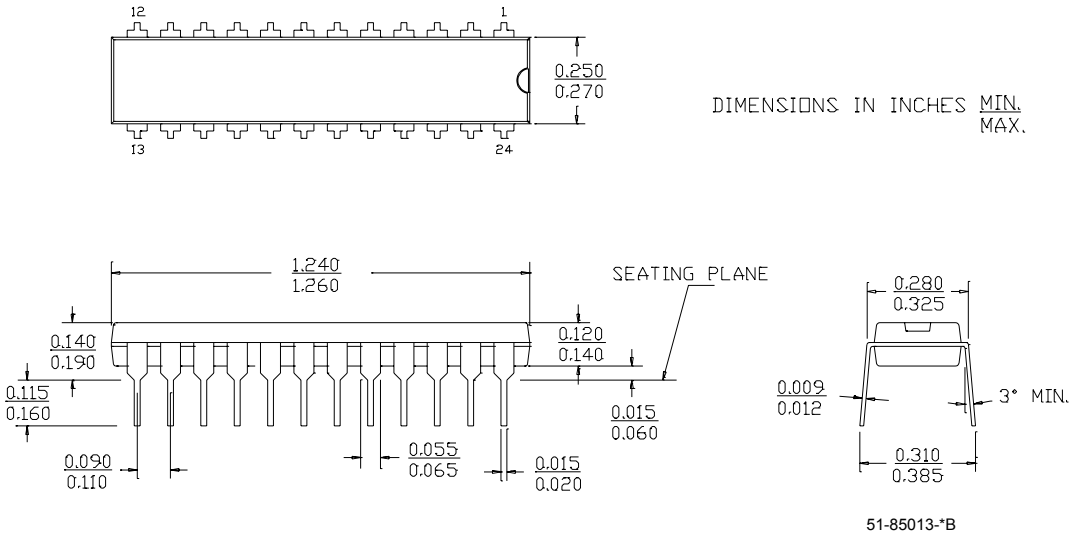


28-Lead (300-Mil) Molded SOJ V21



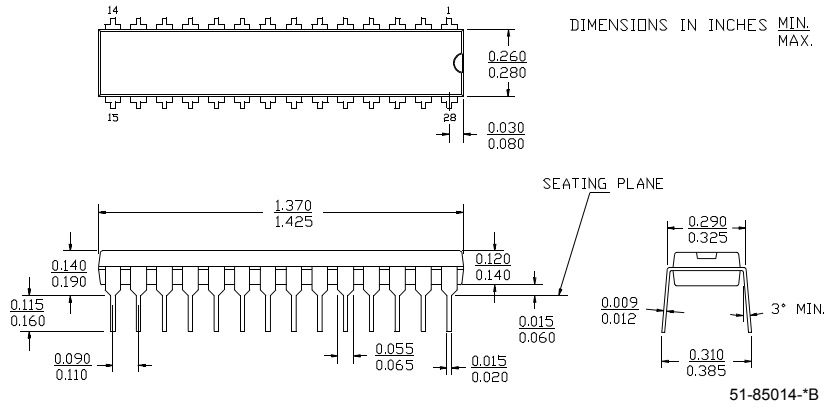
Package Diagram (continued)

24-Lead (300-Mil) PDIP P13



51-85013-*B

28-Lead (300-Mil) Molded DIP P21



51-85014-*B

Document History Page

Document Title: CY7C194B-CY7C195B 256 Kb (64K x 4) Static RAM Document Number: 38-05409				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129234	09/16/03	HGK	New Data Sheet
*A	129786	09/18/03	AJU	Found typos in AC Electrical Characteristics table. Modified the following: t_{SCE} from 10, 12 and 20 to 9, 10 and 18; t_{AW} from 10, 12 and 20 to 9, 10 and 20; t_{PWE} from 10, 12 and 20 to 8, 9 and 18.