

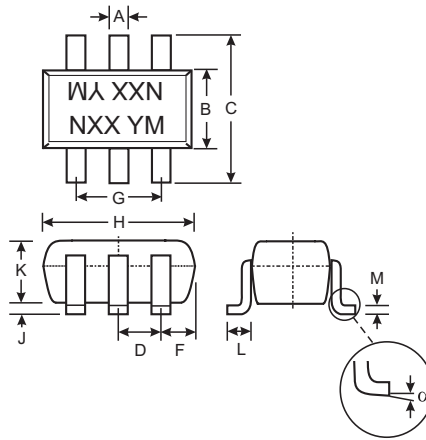
## NPN PRE-BIASED SMALL SIGNAL SOT-363 DUAL SURFACE MOUNT TRANSISTOR

### Features

- Epitaxial Planar Die Construction
- Complementary PNP Types Available (DDA)
- Built-In Biasing Resistors
- **Lead Free/RoHS Compliant (Note 3)**

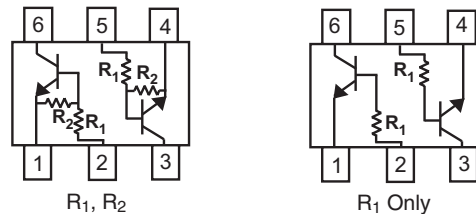
### Mechanical Data

- Case: SOT-363
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 3)
- Ordering Information (See Page 3)
- Weight: 0.006 grams (approximate)



SOT-363		
Dim	Min	Max
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	—	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
α	0°	8°
All Dimensions in mm		

P/N	R1	R2	MARKING
DDC124EU	22KΩ	22KΩ	N17
DDC144EU	47KΩ	47KΩ	N20
DDC114YU	10KΩ	47KΩ	N14
DDC123JU	2.2KΩ	47KΩ	N06
DDC114EU	10KΩ	10KΩ	N13
DDC113TU	1KΩ	—	N01
DDC143TU	4.7KΩ	—	N07
DDC114TU	10KΩ	—	N12



SCHEMATIC DIAGRAM

### Maximum Ratings @ T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage, (6) to (1) and (3) to (4)	V <sub>CC</sub>	50	V
Input Voltage, (2) to (1) and (5) to (4)	V <sub>IN</sub>	-10 to +40 -10 to +40 -6 to +40 -5 to +12 -10 to +40 -5 V <sub>max</sub> -5 V <sub>max</sub> -5 V <sub>max</sub>	V
Output Current	I <sub>O</sub>	30 30 70 100 50 100 100 100	mA
Output Current	I <sub>C</sub> (Max)	100	mA
Power Dissipation (Total)	P <sub>d</sub>	200	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R <sub>θJA</sub>	625	°C/W
Operating and Storage and Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.  
 2. 150mW per element must not be exceeded.  
 3. No purposefully added lead.

**Electrical Characteristics** @ T<sub>A</sub> = 25°C unless otherwise specified

Characteristic (DDC113TU & DDC143TU & DDC114TU only)	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV <sub>CBO</sub>	50	---	---	V	I <sub>C</sub> = 50μA
Collector-Emitter Breakdown Voltage	BV <sub>CEO</sub>	50	---	---	V	I <sub>C</sub> = 1mA
Emitter-Base Breakdown Voltage	BV <sub>EBO</sub>	5	---	---	V	I <sub>E</sub> = 50μA
Collector Cutoff Current	I <sub>CBO</sub>	---	---	0.5	μA	V <sub>CB</sub> = 50V
Emitter Cutoff Current	I <sub>EBO</sub>	---	---	0.5	μA	V <sub>EB</sub> = 4V
Collector-Emitter Saturation Voltage	V <sub>CE(sat)</sub>	---	---	0.3	V	I <sub>C</sub> /I <sub>B</sub> = 2.5mA / 0.25mA DDC143TU I <sub>C</sub> /I <sub>B</sub> = 1mA / 0.1mA DDC114TU I <sub>C</sub> /I <sub>B</sub> = 10mA / 1mA DDC113TU
DC Current Transfer Ratio	h <sub>FE</sub>	100	250	600	---	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V
Input Resistor (R <sub>1</sub> ) Tolerance	ΔR <sub>1</sub>	-30	---	+30	%	---
Gain-Bandwidth Product*	f <sub>T</sub>	---	250	---	MHz	V <sub>CE</sub> = 10V, I <sub>E</sub> = -5mA, f = 100MHz

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage	V <sub>I(off)</sub>	0.5	1.1	---	V	V <sub>CC</sub> = 5V, I <sub>O</sub> = 100μA
		0.5	1.1	---		
Input Voltage	V <sub>I(on)</sub>	0.3	---	---	V	V <sub>O</sub> = 0.3, I <sub>O</sub> = 5mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 2mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 1mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 5mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 10mA
		0.5	---	---		
Input Voltage	V <sub>I(on)</sub>	0.5	1.1	---	V	I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA I <sub>O</sub> /I <sub>I</sub> = 5mA / 0.25mA I <sub>O</sub> /I <sub>I</sub> = 5mA / 0.25mA I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA
		---	1.9	3.0		
Output Voltage	V <sub>O(on)</sub>	---	1.9	3.0	V	V <sub>O</sub> = 0.3, I <sub>O</sub> = 5mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 2mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 1mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 5mA V <sub>O</sub> = 0.3, I <sub>O</sub> = 10mA
		---	1.9	3.0		
Output Voltage	V <sub>O(on)</sub>	---	0.1	0.3	V	I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA I <sub>O</sub> /I <sub>I</sub> = 5mA / 0.25mA I <sub>O</sub> /I <sub>I</sub> = 5mA / 0.25mA I <sub>O</sub> /I <sub>I</sub> = 10mA / 0.5mA
		---	0.1	0.3		
Input Current	I <sub>I</sub>	---	---	0.36 0.18 0.88 3.6 0.88	mA	V <sub>I</sub> = 5V
Output Current	I <sub>O(off)</sub>	---	---	0.5	μA	V <sub>CC</sub> = 50V, V <sub>I</sub> = 0V
DC Current Gain	G <sub>I</sub>	56 68 68 80 30	---	---	---	V <sub>O</sub> = 5V, I <sub>O</sub> = 5mA V <sub>O</sub> = 5V, I <sub>O</sub> = 5mA V <sub>O</sub> = 5V, I <sub>O</sub> = 10mA V <sub>O</sub> = 5V, I <sub>O</sub> = 10mA V <sub>O</sub> = 5V, I <sub>O</sub> = 5mA
Input Resistor (R <sub>1</sub> ) Tolerance	ΔR <sub>1</sub>	-30	---	+30	%	---
Resistance Ratio Tolerance	R <sub>2</sub> /R <sub>1</sub>	-20	---	+20	%	---
Gain-Bandwidth Product*	f <sub>T</sub>	---	250	---	MHz	V <sub>CE</sub> = 10V, I <sub>E</sub> = 5mA, f = 100MHz

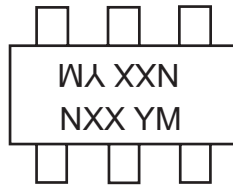
\* Transistor - For Reference Only

**Ordering Information** (Note 4)

Device	Packaging	Shipping
DDC124EU-7-F	SOT-363	3000/Tape & Reel
DDC144EU-7-F	SOT-363	3000/Tape & Reel
DDC114YU-7-F	SOT-363	3000/Tape & Reel
DDC123JU-7-F	SOT-363	3000/Tape & Reel
DDC114EU-7-F	SOT-363	3000/Tape & Reel
DDC113TU-7-F	SOT-363	3000/Tape & Reel
DDC143TU-7-F	SOT-363	3000/Tape & Reel
DDC114TU-7-F	SOT-363	3000/Tape & Reel

Notes: 4. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

**Marking Information**



NXX = Product Type Marking Code  
See Sheet 1 Diagrams  
YM = Date Code Marking  
Y = Year ex: T = 2006  
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
Code	N	P	R	S	T	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**TYPICAL CURVES - DDC123JK**  
**ONE SECTION**

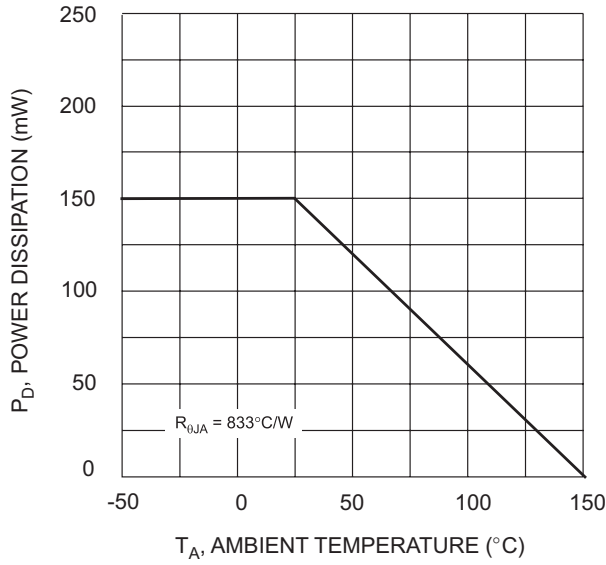


Fig. 1 Derating Curve

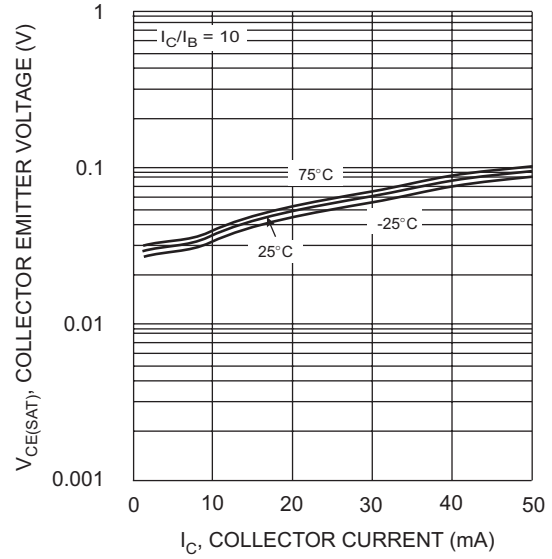


Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$

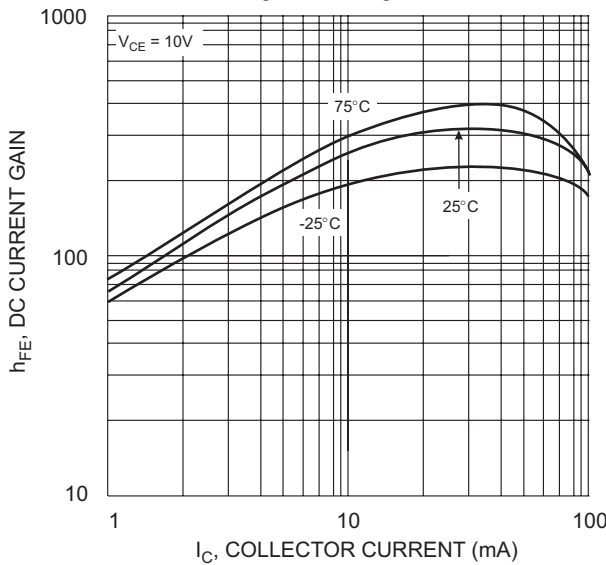


Fig. 3 DC Current Gain

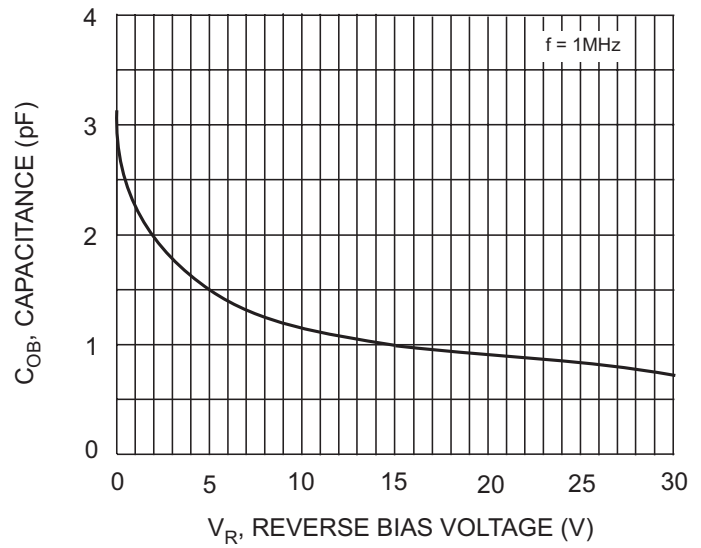


Fig. 4 Output Capacitance

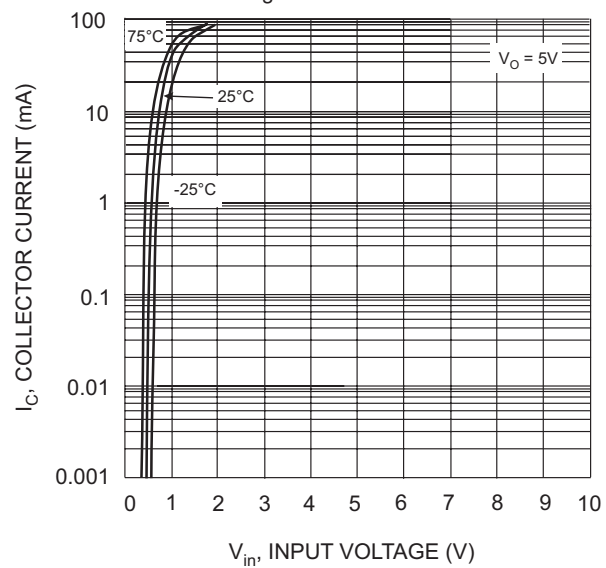


Fig. 5 Collector Current Vs. Input Voltage

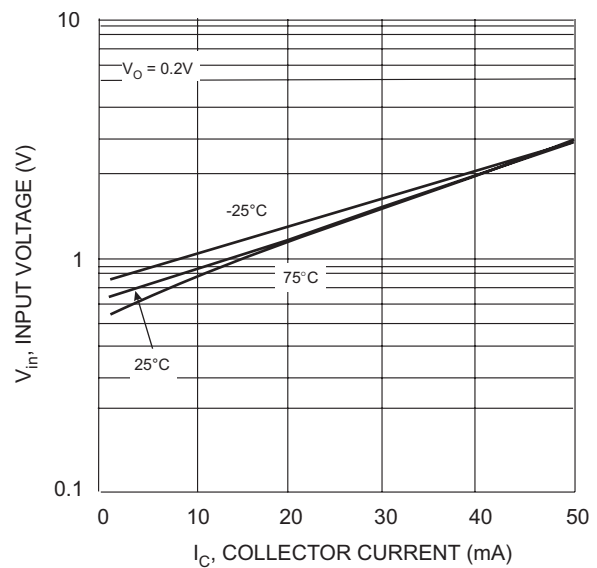


Fig. 6 Input Voltage vs. Collector Current

**TYPICAL CURVES - DDC114TK**

**ONE SECTION**

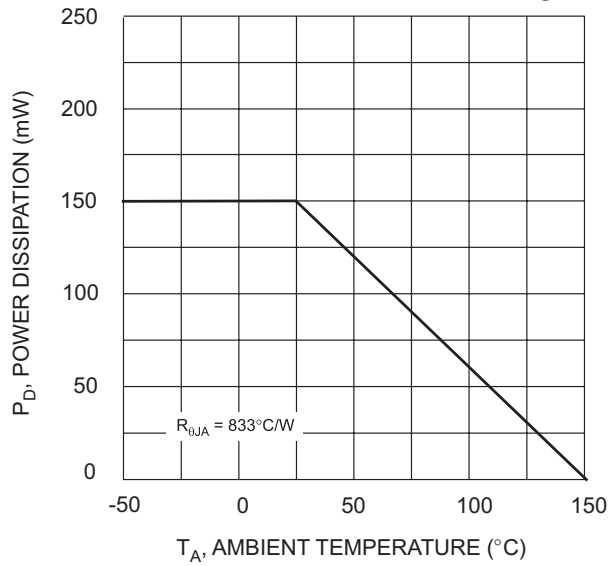


Fig. 1 Derating Curve

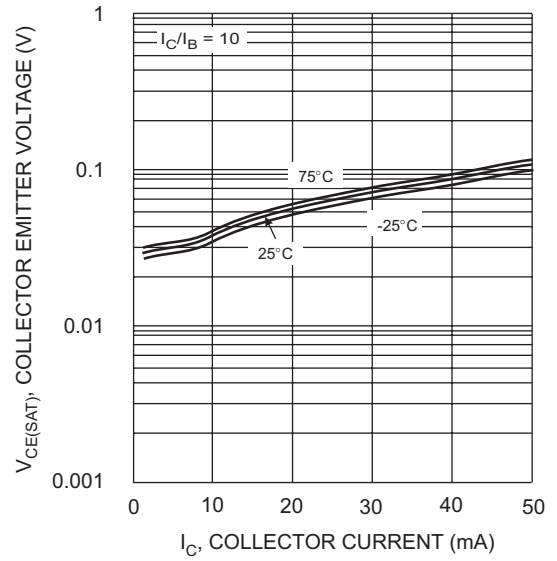


Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$

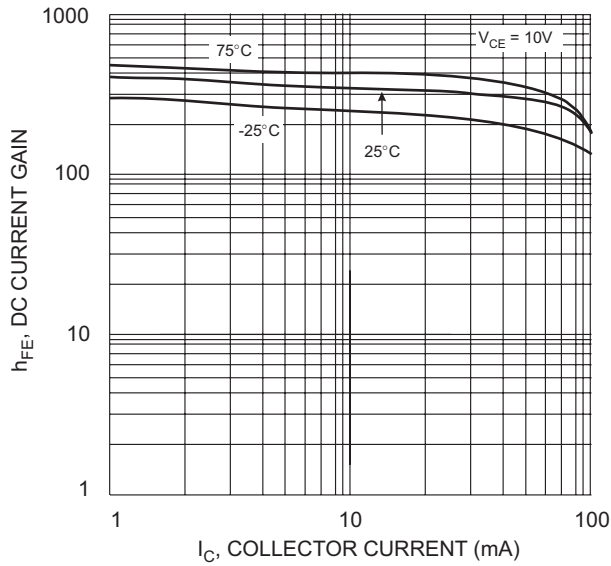


Fig. 3 DC Current Gain

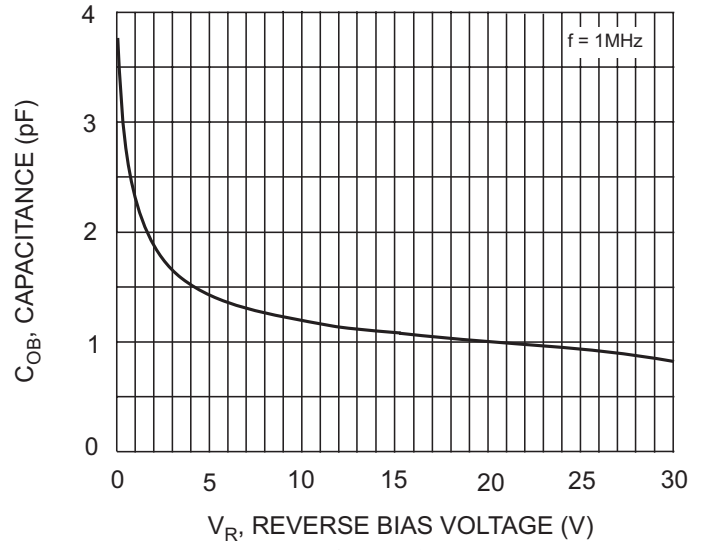


Fig. 4 Output Capacitance

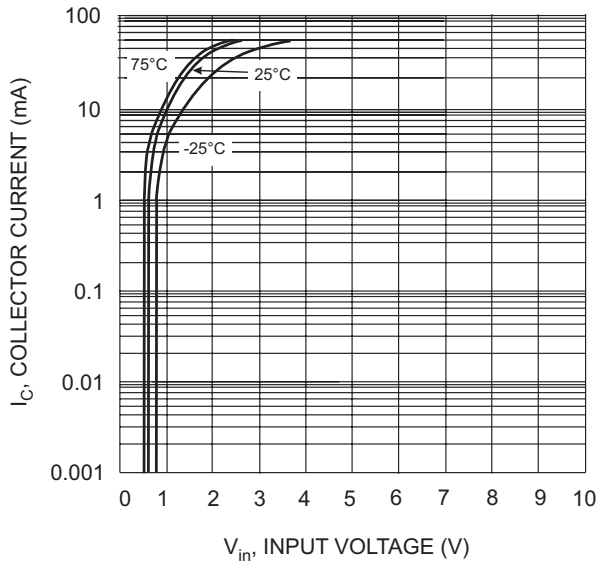


Fig. 7 Collector Current Vs. Input Voltage

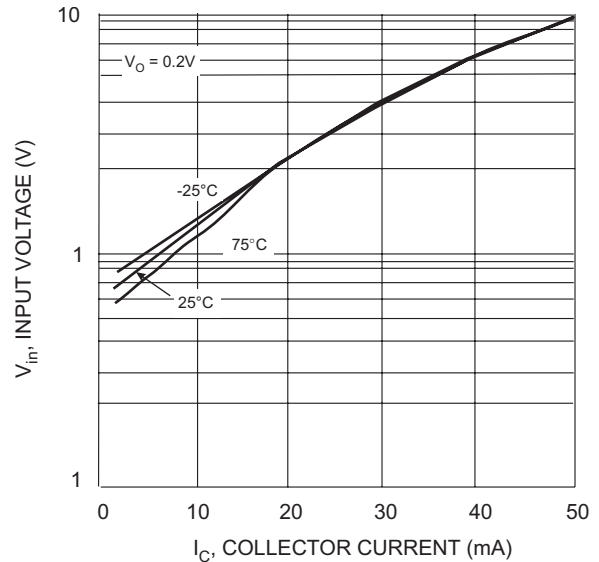


Fig. 6 Input Voltage vs. Collector Current

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