32-Channel, Current-Input Analog-to-Digital Converter

FEATURES

- **SINGLE-CHIP SOLUTION TO DIRECTLY MEASURE 32 LOW-LEVEL CURRENTS**
- **HIGH-PRECISION, TRUE INTEGRATING FUNCTION**
- **INTEGRAL LINEARITY: ±0.025% of Reading ±1.0ppm of FSR**
- **VERY LOW NOISE: 5.3ppm of FSR**
- **LOW POWER: 7mW/channel**
- **ADJUSTABLE FULL-SCALE RANGE**
- **ADJUSTABLE DATA RATE: Up to 6kSPS**
  - **Integration Times Down to 166.5μs**
- **DAISY-CHAINABLE SERIAL INTERFACE**

APPLICATIONS

- **CT SCANNER DAS**
- **PHOTODIODE SENSORS**
- **X-RAY DETECTION SYSTEMS**

Protected by US Patent #5841310

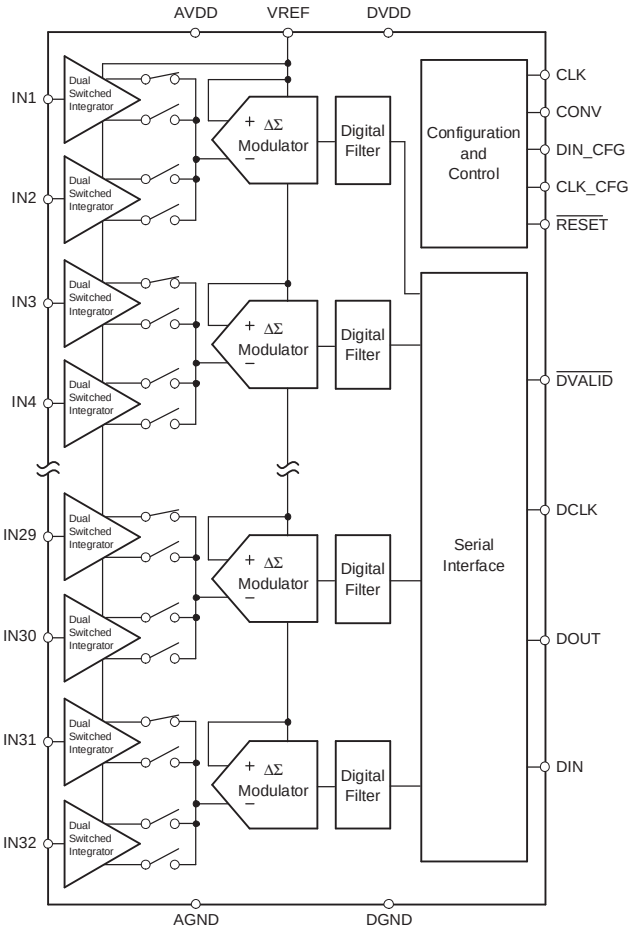
DESCRIPTION

The DDC232 is a 20-bit, 32-channel, current-input analog-to-digital (A/D) converter. It combines both current-to-voltage and A/D conversion so that 32 separate low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

For each of the 32 inputs, the DDC232 provides a dual-switched integrator front-end. This configuration allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable integration times range from 166μs to 1s, allowing currents from fAs to μAs to be continuously measured with outstanding precision.

The DDC232 has a serial interface designed for daisy-chaining in multi-device systems. Simply connect the output of one device to the input of the next to create the chain. Common clocking feeds all the devices in the chain so that the digital overhead in a multi-DDC232 system is minimal.

The DDC232 uses a +5V analog supply and a +2.7V to +3.6V digital supply. Operating over the temperature range of 0°C to +70°C, the DDC232 is offered in a BGA-64 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document.

ABSOLUTE MAXIMUM RATINGS(1)

AVDD to AGND	–0.3V to +6V
DVDD to DGND	–0.3V to +3.6V
AGND to DGND	±0.2V
VREF Input to AGND	2.0V to AVDD + 0.3V
Analog Input to AGND	–0.3V to +0.7V
Digital Input Voltage to DGND	–0.3V to DVDD + 0.3V
Digital Output Voltage to DGND	–0.3V to AVDD + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	–60°C to +150°C
Junction Temperature (T_J)	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3.0V, VREF = +4.096V, t_{INT} = 333µs in Low-Power mode (CLK = 5MHz), Range = 7, and continuous mode operation, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC232C			DDC232CK			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT RANGE								
Range 1		45	50	55	45	50	55	pC
Range 2		90	100	110	90	100	110	pC
Range 3		135	150	165	135	150	165	pC
Range 4		180	200	220	180	200	220	pC
Range 5		225	250	275	225	250	275	pC
Range 6		270	300	330	270	300	330	pC
Range 7		315	350	385	315	350	385	pC
Negative Full-Scale Range		–0.4% of Positive Full-Scale Range			–0.4% of Positive Full-Scale Range			pC
DYNAMIC CHARACTERISTICS								
Data Rate	Low-Power Mode		3	3.125		3	3.125	kSPS
	High-Speed Mode	Not Supported				6	6.2	kSPS
Integration Time, t_{INT}	Continuous Mode, Low-Power Mode	320		1,000,000	320		1,000,000	µs
	Continuous Mode, High-Speed Mode	Not Supported			162		1,000,000	µs
	Non-Continuous Mode	50			50			µs
System Clock (CLK)	Low-Power Mode, Clk_4x = 0	1		5	1		5	MHz
	High-Speed Mode, Clk_4x = 0	1		10	1		10	MHz
	Low-Power Mode, Clk_4x = 1	4		20	4		20	MHz
	High-Speed Mode, Clk_4x = 1	4		40	4		40	MHz
Data Clock (DCLK)				20			20	MHz
Configuration Clock (CLK_CFG)				20			20	MHz
ACCURACY								
Noise, Low-Level Input(1)	C_{SENSOR}(2) = 50pF		5.3	7				ppm of FSR(3), rms
Integral Linearity Error(4)		±0.025% Reading ± 1.0ppm FSR, typ						
		±0.05% Reading ± 1.5ppm FSR, max						
Resolution	Format = 1	20			20			Bits
	Format = 0	16			16			Bits
Input Bias Current			±0.1	±10		±0.1	±10	pA
Range Error Match(5)			0.1	0.5		0.1	0.5	% of FSR
Range Sensitivity to VREF	VREF = 4.096 ±0.1V		1:1			1:1		
Offset Error			±200	±1000		±200	±1000	ppm of FSR
Offset Error Match(5)			±100			±100		ppm of FSR
DC Bias Voltage(6)	Low-Level Input (< 1% FSR)		±0.1	±2		±0.1	±2	mV
Power-Supply Rejection Ratio	at DC		100	±800		100	±800	ppm of FSR/V

(1) Input is less than 1% of full-scale.
(2) C_{SENSOR} is the capacitance seen at the DDC232 inputs from wiring, photodiode, etc.
(3) FSR is Full-Scale Range.
(4) A best-fit line is used in measuring nonlinearity.
(5) Matching between side A and side B of the same input.
(6) Voltage produced by the DDC232 at its input that is applied to the sensor.

ELECTRICAL CHARACTERISTICS (continued)

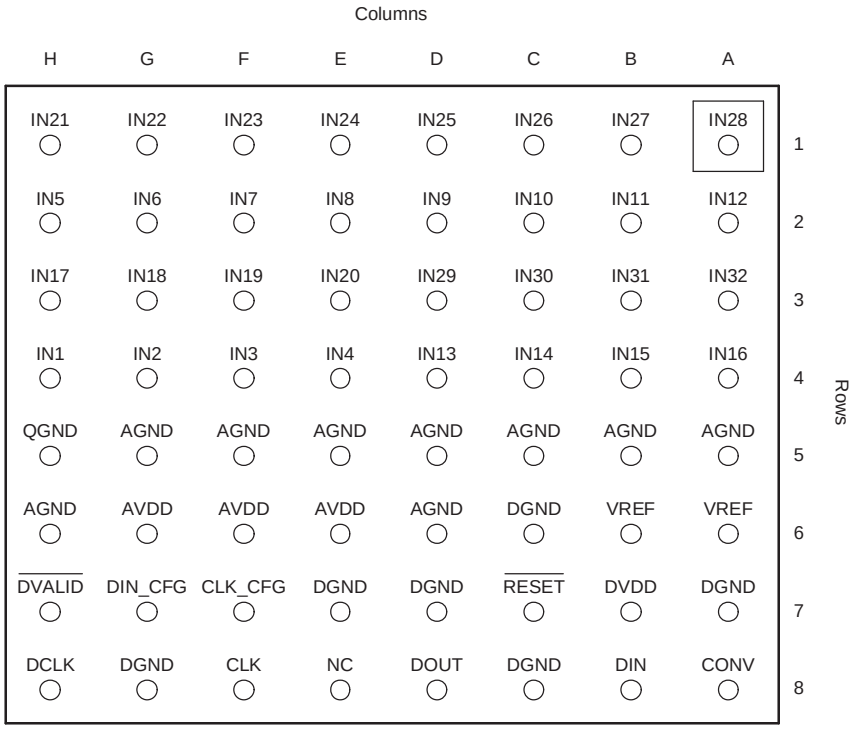
At T_A = +25°C, AVDD = +5V, DVDD = +3.0V, VREF = +4.096V, t_{INT} = 333µs in Low-Power mode (CLK = 5MHz), Range = 7, and continuous mode operation, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC232C			DDC232CK			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
PERFORMANCE OVER TEMPERATURE								
Offset Drift			±0.5	5(7)		±0.5	5(7)	ppm of FSR/°C
Offset Drift Stability			±0.2	2(7)		±0.2	2(7)	ppm of FSR/minute
DC Bias Voltage Drift(8)			±3			±3		µV/°C
Input Bias Current Drift	T_A = +25°C to +45°C		0.01	1(7)		0.01	1(7)	pA/°C
Range Drift(9)			25	50		25	50	ppm/°C
Range Drift Match(10)			±5			±5		ppm/°C
REFERENCE								
Voltage		4.000	4.096	4.200	4.000	4.096	4.200	V
Input Current(11)	Average Value with t_{INT} = 333µs		325			325		µA
	Average Value with t_{INT} = 166.5µs		650			650		µA
DIGITAL INPUT/OUTPUT								
Logic Levels								
V_{IH}		(0.8)DVDD		DVDD + 0.1	(0.8)DVDD		DVDD + 0.1	V
V_{IL}		–0.1		(0.2)DVDD	–0.1		(0.2)DVDD	V
V_{OH}	I_{OH} = –500µA	DVDD – 0.4			DVDD – 0.4			V
V_{OL}	I_{OL} = 500µA			0.4			0.4	V
Input Current (I_{IN})	0 < V_{IN} < DVDD			±10			±10	µA
Data Format(12)		Straight Binary			Straight Binary			
POWER-SUPPLY REQUIREMENTS								
Analog Power-Supply Voltage (AVDD)		4.75	5.0	5.25	4.75	5.0	5.25	V
Digital Power-Supply Voltage (DVDD)		2.7	3.0	3.6	2.7	3.0	3.6	V
Supply Current								
Analog Current	Low-Power Mode		41			41		mA
	High-Speed Mode		Not Supported			60		mA
Digital Current	Low-Power Mode		3.7			3.7		mA
	High-Speed Mode		Not Supported			7.0		mA
Total Power Dissipation	Low-Power Mode		224	288		224	288	mW
	High-Speed Mode		Not Supported			320		mW
Per Channel Power Dissipation	Low-Power Mode		7	9		7	9	mW/Channel
	High-Speed Mode		Not Supported			10		mW/Channel

(7) Ensured by design, not production tested.
(8) Voltage produced by the DDC232 at its input that is applied to the sensor.
(9) Range drift does not include external reference drift.
(10) Matching between side A and side B of the same input.
(11) Input reference current decreases with increasing t_{INT} (see the *Voltage Reference* section, page 10).
(12) Data format is Straight Binary with a small offset. The number of bits in the output word is controlled by the Format bit.

PIN CONFIGURATION

Top View **BGA**



PIN DESCRIPTIONS

PIN	LOCATION	FUNCTION	DESCRIPTION
IN1–32	Rows 1–4	Analog Input	Analog Inputs for Channels 1 to 32
QGND	H5	Analog	Quiet Analog Ground
AGND	G5, F5, E5, D5, C5, B5, A5, D6, H6	Analog	Analog Ground
DGND	A7, C6, D7, E7, C8, G8	Digital	Digital Ground
AVDD	E6, F6, G6	Analog	Analog Power Supply, +5V Nominal
VREF	A6, B6	Analog Input	External Voltage Reference Input, +4.096V Nominal
$\overline{\text{DVALID}}$	H7	Digital Output	Data Valid Output, Active Low
DIN_CFG	G7	Digital Input	Configuration Register Data Input
CLK_CFG	F7	Digital Input	Configuration Register Clock Input
$\overline{\text{RESET}}$	C7	Digital Input	Digital Reset, Active Low
DVDD	B7	Digital	Digital Power Supply, 3.3V Nominal
CONV	A8	Digital Input	Conversion Control Input; 0 = Integrate on Side B, 1 = Integrate on Side A
DIN	B8	Digital Input	Serial Data Input
DOUT	D8	Digital Output	Serial Data Output
NC	E8	No Connect	Do not connect; must be left floating.
CLK	F8	Digital Input	Master Clock Input
DCLK	H8	Digital Input	Serial Data Clock Input

TYPICAL CHARACTERISTICS

At T_A = 25°C, unless otherwise indicated.

NOISE vs C_{SENSOR}

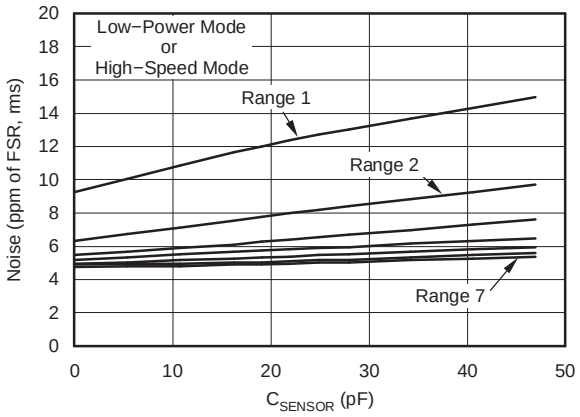


Figure 1.

NOISE vs C_{SENSOR}

C_{SENSOR} (pF)	Noise (ppm of FSR, rms)						
	Range 1	Range 2	Range 3	Range 4	Range 5	Range 6	Range 7
0	9.3	6.3	5.5	5.2	5.0	4.9	4.8
22	12.4	8.0	6.4	5.8	5.4	5.1	5.0
47	15.0	9.7	7.6	6.5	6.0	5.6	5.3

THEORY OF OPERATION

The block diagram of the DDC232 is shown in Figure 2. The device contains 32 identical input channels that perform the function of current-to-voltage integration followed by a multiplexed A/D conversion. Each input has two integrators so that the current-to-voltage integration can be continuous in time. The output of the 64 integrators are switched to 16 delta-sigma (ΔΣ) converters via multiplexers. With the DDC232 in the continuous integration mode, the output of the integrators from one side of the inputs will be digitized while the other 32 integrators are in the integration mode. This integration and A/D conversion process is controlled by the system clock, CLK. The results from side A and side B of each signal input are stored in a serial output shift register. The $\overline{\text{DVALID}}$ output goes low when the shift register contains valid data.

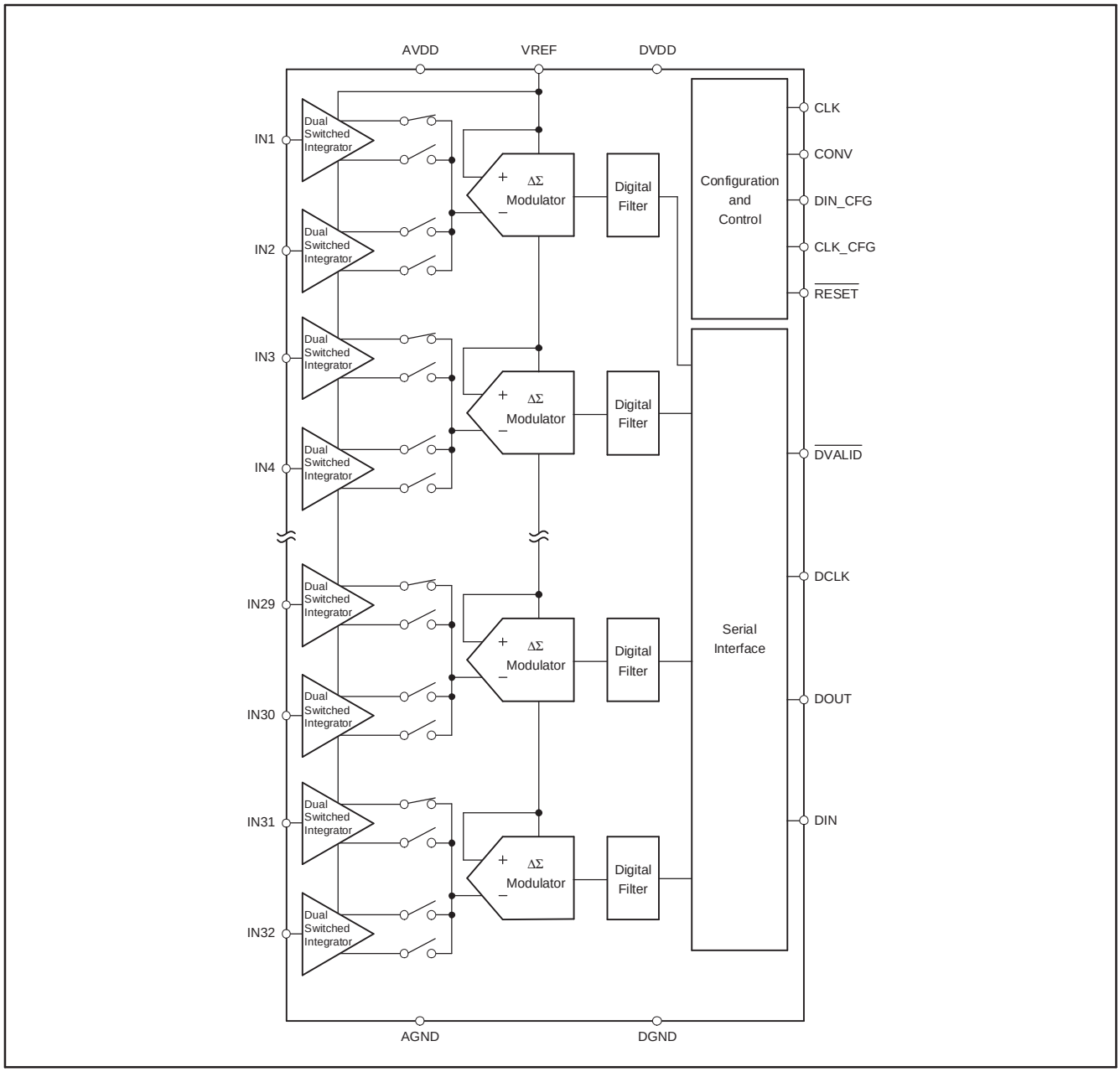


Figure 2. DDC232 Block Diagram

DEVICE OPERATION

Basic Integration Cycle

The topology of the front end of the DDC232 is an analog integrator as shown in Figure 3. In this diagram, only input IN1 is shown. The input stage consists of an operational amplifier, a selectable feedback capacitor network (C_F), and several switches that implement the integration cycle. The timing relationships of all of the switches shown in Figure 3 are illustrated in Figure 4. Figure 4 conceptualizes the operation of the integrator input stage of the DDC232 and should not be used as an exact timing tool for design.

See Figure 5 for the block diagrams of the reset, integrate, wait, and convert states of the integrator section of the DDC232. This internal switching network is controlled externally with the convert pin (CONV), and the system clock (CLK). For the best noise performance, CONV must be synchronized with the rising edge of CLK. It is recommended that CONV toggle within ±10ns of the rising edge of CLK.

The noninverting inputs of the integrators are connected to ground. Consequently, the DDC232 analog ground should be as clean as possible. The internal and external capacitors (C_F), are shown in parallel between the inverting input and output of the operational amplifier. At the beginning of a conversion, the switches $S_{A/D}$, S_{INTA}, S_{INTB}, S_{REF1}, S_{REF2}, and S_{RESET} are set (see Figure 4).

At the completion of an A/D conversion, the charge on the integration capacitor (C_F) is reset with S_{REF1} and S_{RESET} (see Figure 4 and Figure 5a). This is done during reset. In this manner, the selected capacitor is charged to the reference voltage, VREF. Once the integration capacitor is charged, S_{REF1} and S_{RESET} are switched so that VREF is no longer connected to the amplifier circuit while it waits to begin integrating (see Figure 5b). With the rising edge of CONV, S_{INTA} closes, which begins the integration of side A. This process puts the integrator stage into its integrate mode (see Figure 5c).

Charge from the input signal is collected on the integration capacitor, causing the voltage output of the amplifier to decrease. The falling edge of CONV stops the integration by switching the input signal from side A to side B (S_{INTA} and S_{INTB}). Prior to the falling edge of CONV, the signal on side B was converted by the A/D converter and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. At this point, the output voltage of the side A operational amplifier is presented to the input of the ΔΣ A/D converter (see Figure 5d).

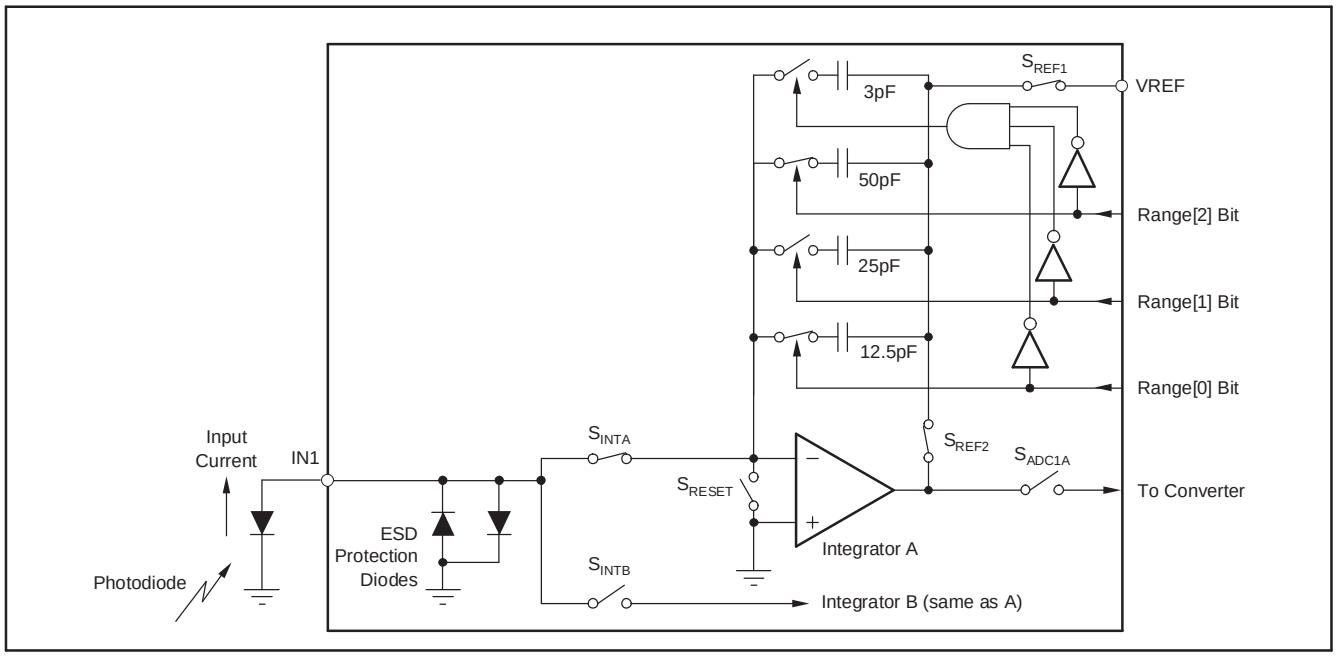


Figure 3. Basic Integration Configuration for Input 1

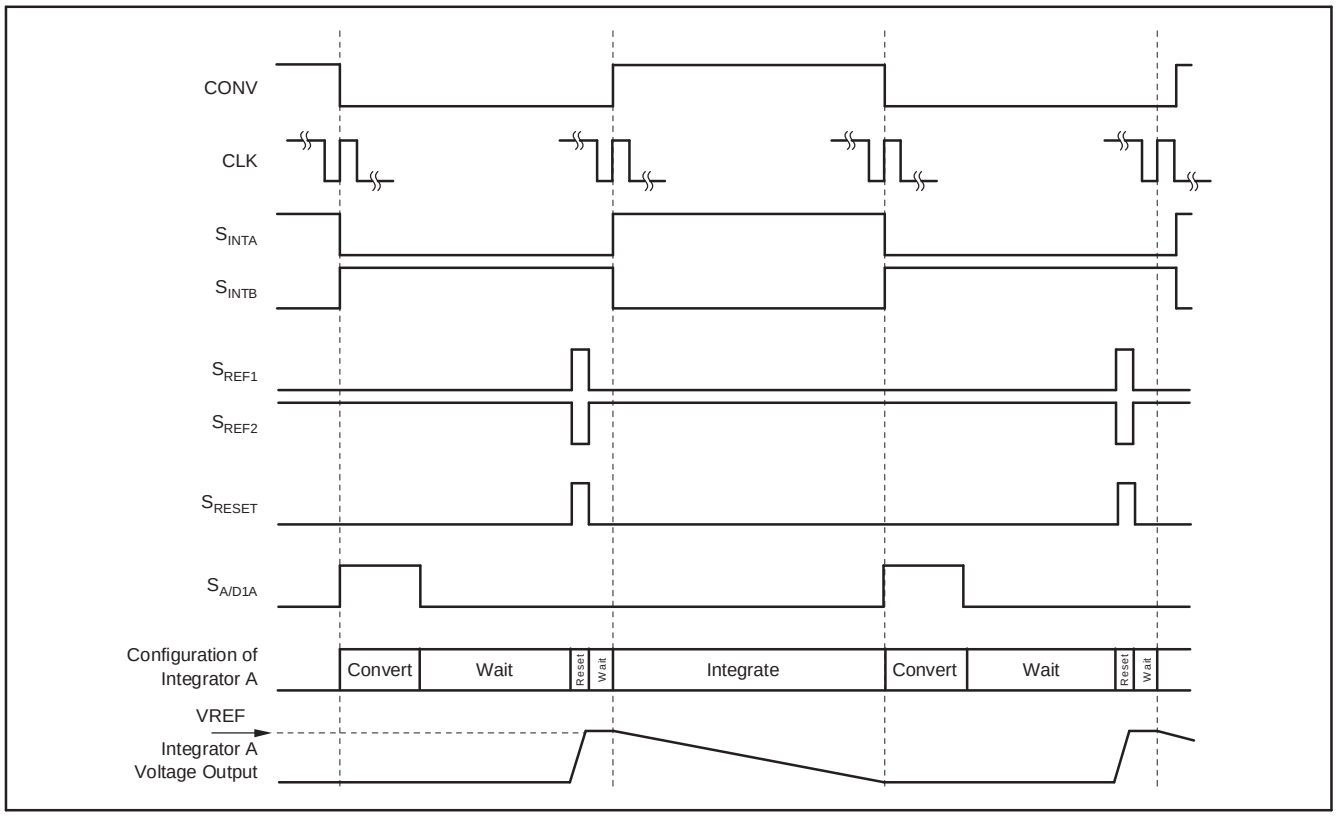


Figure 4. Integration Timing Diagram (see Figure 3)

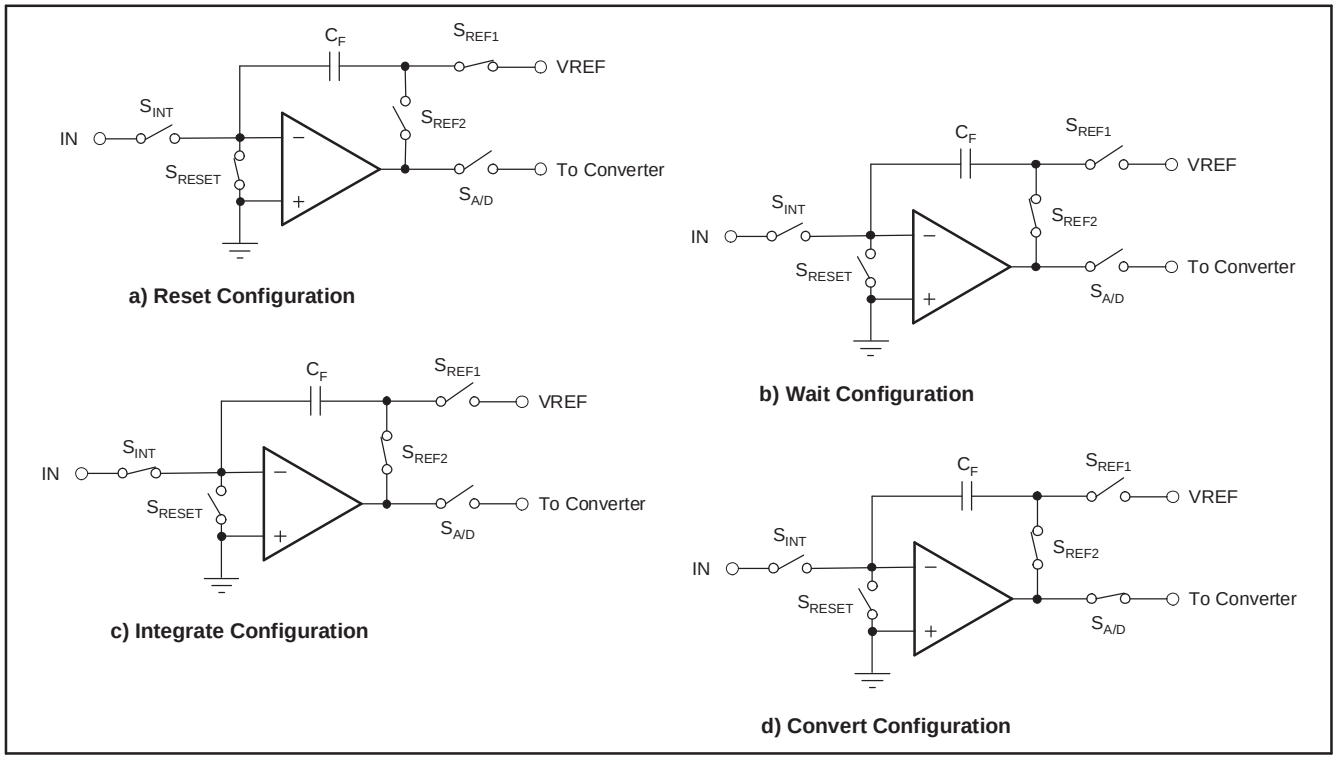


Figure 5. Diagrams for the Four Configurations of the Front-End Integrators

Integration Capacitors

There are seven different capacitors available on-chip for both sides of every channel in the DDC232. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC232. The range control bits (Range[2:0]) change the capacitor value for all integrators. Consequently, all inputs and both sides of each input will always have the same full-scale range. Table 1 shows the capacitor value selected for each range selection.

Table 1. Range Selection

Range[2]	Range[1]	Range[0]	C_F (pF, typ)	INPUT RANGE (pC, typ)
0	0	0	3	–0.04 to 12.5
0	0	1	12.5	–0.2 to 50
0	1	0	25	–0.4 to 100
0	1	1	37.5	–0.6 to 150
1	0	0	50	–0.8 to 200
1	0	1	62.5	–0.1 to 250
1	1	0	75	–1.2 to 300
1	1	1	87.5	–1.4 to 350

Voltage Reference

The external voltage reference is used to reset the integration capacitors before an integration cycle begins. It is also used by the ΔΣ converter while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply the charge needed by the ΔΣ converter. For an integration time of 333µs, this charge translates to an average VREF current of approximately 325µA. The amount of charge needed by the ΔΣ converter is independent of the integration time; therefore, increasing the integration time lowers the average current. For example, an integration time of 800µs lowers the average VREF current to **TBD**µA.

It is critical that VREF be stable during the different modes of operation (see Figure 5). The ΔΣ converter measures the voltage on the integrator with respect to VREF. Since the integrator capacitors are initially reset to VREF, any drop in VREF from the time the capacitors are reset to the time when the converter measures the integrator output will introduce an offset. It is also important that VREF be stable over longer periods of time because changes in VREF correspond directly to changes in the full-scale range. Finally, VREF should introduce as little additional noise as possible.

For these reasons, it is strongly recommended that the external reference source be buffered with an operational amplifier, as shown in Figure 6. In this circuit, the voltage reference is generated by a +4.096V reference. A low-pass filter to reduce noise connects the reference to an operational amplifier configured as a buffer. This amplifier should have low noise and input/output common-mode ranges that support VREF. Even though the circuit in Figure 6 might appear to be unstable due to the large output capacitors, it works well for most operational amplifiers. It is ***not*** recommended that series resistance be placed in the output lead to improve stability since this can cause a drop in VREF, which produces large offsets.

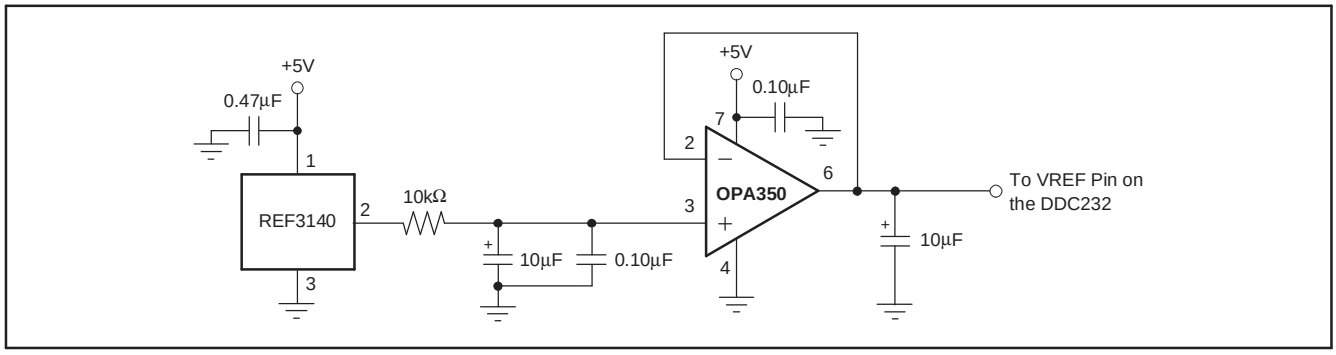


Figure 6. Recommended External Voltage Reference Circuit for Best Low-Noise Operation

Frequency Response

The frequency response of the DDC232 is set by the front end integrators and is that of a traditional continuous time integrator, as shown in Figure 7. By adjusting t_{INT}, the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the ΔΣ converter that follows the front end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the ΔΣ converter is always a DC signal. Since the output of the front end integrators are sampled, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal will fold back down to lower frequencies.

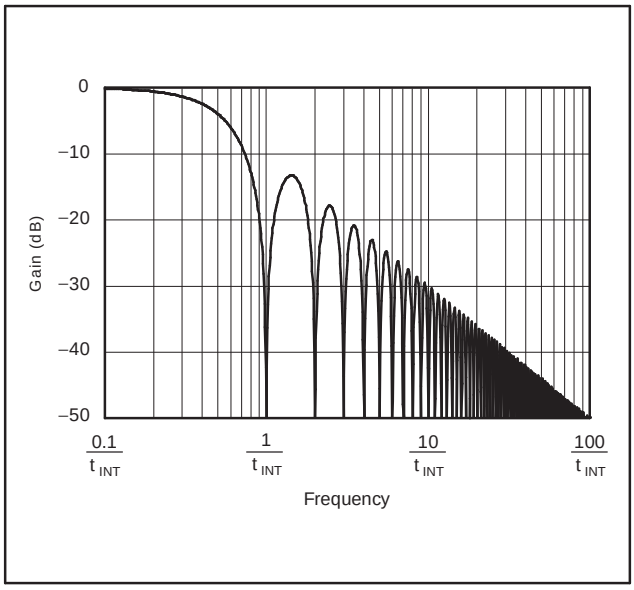


Figure 7. TFrequency Response

CONFIGURATION REGISTER

Some aspects of device operation are controlled by the onboard configuration register. The DIN_CFG, CLK_CFG, and $\overline{\text{RESET}}$ pins are used to write to this register. When beginning a write operation, hold CONV low and strobe $\overline{\text{RESET}}$; see Figure 8. Then begin shifting in the configuration data on DIN_CFG. Data is written to the configuration register most significant bit first. The data is internally latched on the falling edge of CLK_CFG. Partial writes to the configuration register are not allowed—make sure to send all 12 bits when updating the register.

Optional readback of the configuration register is available immediately after the write sequence. During readback, the 12-bit configuration data followed by a 4-bit revision id and the test pattern are shifted out on the DOUT pin on the rising edge of DCLK.

NOTE: with Format = 1, the test pattern is 304 bits with only the last 72 bits non-zero. This sequence of outputs is repeated twice for each DDC232 and daisy-chaining is supported in configuration readback. Table 2 shows the test pattern configuration during readback. Table 3 shows the timing for the configuration register read and write operations. Strobe CONV to begin normal operation.

Table 2. Test Pattern During Readback

Format BIT	TEST PATTERN (Hex)	TOTAL READBACK BITS
0	30F066012480F6h	512
1	30F066012480F69055h	640

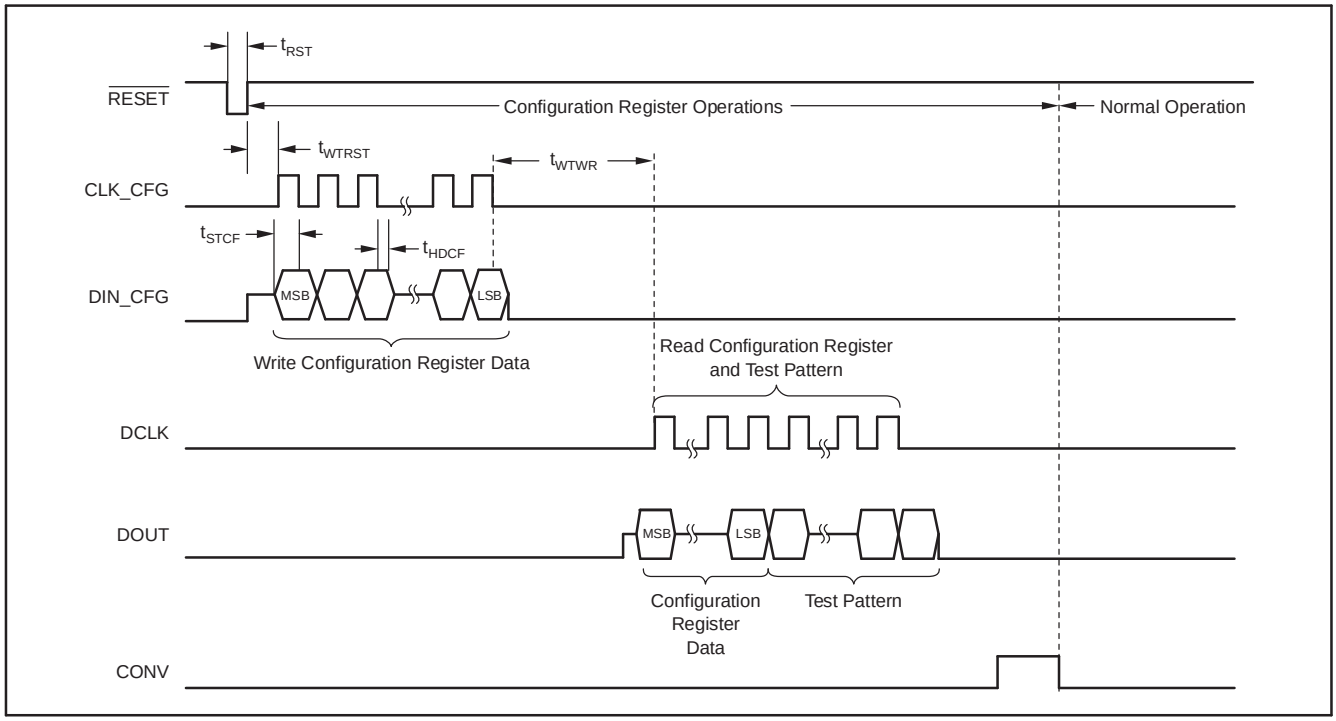


Figure 8. Configuration Register Write and Read Operations

Table 3. Timing for the Configuration Register Read/Write

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WTRST}	Wait Required from Reset High to First Rising Edge of CLK_CFG	2			µs
t_{WTWR}	Wait Required from Last CLK-CFG of Write Operation to First CLK_CFG of Read Operation	2			µs
t_{STCF}	Set-Up Time from DIN_CFG to Falling Edge of CLK_CFG	10			ns
t_{HDCF}	Hold Time for DIN_CFG After Falling Edge of CLK_CFG	10			ns
t_{RST}	Pulse Width for $\overline{\text{RESET}}$ Active	1			µs

Configuration Register

Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Range[2]	Range[1]	Range[0]	Format	Pwr/Spd	Clk_4x	0	0	0	0	0	Test

Bits 11–9 Range[2:0] Analog Input Range

000: 12.5pC
001: 50pC
010: 100pC
011: 150pC
100: 200pC
101: 250pC
110: 300pC
111: 350pC (default)

Bit 8 Format
0 = 16-Bit Output
1 = 20-Bit Output (default)

Format selects how many bits are used in the data output word.

Bit 7 Pwr/Spd
0 = Low-Power Mode (default)
1 = High-Speed Mode (DDC232CK Only)

Pwr/Spd BIT	MODE	TYPICAL POWER/CHANNEL (mW)	MAXIMUM CLK FREQUENCY (MHz)(1)	MAXIMUM DATA RATE (kHz)
0	Low-Power	7	5	3.125
1(2)	High-Speed(2)	10	10	6

(1) Assumes Clk_4x = 0.
(2) Only the DDC232CK supports High-Speed mode.

Bit 6 Clk_4x (System Clock Divider)
0 = Internal Clock Divider = 1 (default)
1 = Internal Clock Divider = 4

The Clk_4x input enables an internal divider on the system clock. When Clk_4x = 1, the system clock is divided by 4. This allows a 4X faster system clock, which in turn provides a finer quantization of the integration time because the CONV signal needs to be synchronized with the system clock for the best performance.

Clk_4x BIT	CLK DIVIDER VALUE	CLK FREQUENCY	INTERNAL CLOCK FREQUENCY
0	1	5MHz	5MHz
1	4	20MHz	5MHz

Bits 5–1 00000

Bit 0 Test Mode
0 = Test Mode Off (default)
1 = Test Mode On

When Test Mode is used, the inputs (IN1 through IN32) are disconnected from the DDC232 integrators to enable the user to measure a zero input signal regardless of the current supplied to the inputs. The test mode works with both the continuous and non-continuous modes.

DIGITAL INTERFACE

The digital interface of the DDC232 outputs the digital results via a synchronous serial interface consisting of a data clock (DCLK), a valid data pin ($\overline{\text{DVALID}}$), a serial data output pin (DOUT), and a serial data input pin (DIN). The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK and DCLK frequencies need not be the same, though for best performance, it is highly recommended that they be derived from the same clocking source to keep their phase relationship constant. DIN is only used when multiple converters are cascaded and should be tied to DGND otherwise. Depending on t_{INT}, CLK, and DCLK, it is possible to daisy-chain multiple converters. This greatly simplifies the interconnection and routing of the digital outputs in those applications where a large number of converters are needed. Configuration of the DDC232 is set by a dedicated register addressed using the DIN_CFG and CLK_CFG pins.

System and Data Clocks (CLK and CONV)

The system clock is supplied to CLK and the data clock is supplied to DCLK. Make sure the clock signals are clean—avoid overshoot or ringing. For best performance, generate both clocks from the same clock source. DCLK should be disabled by taking it low after the data has been shifted out or while CONV is transitioning.

When using multiple DDC232s, pay close attention to the DCLK distribution on the printed circuit board (PCB). In particular, make sure to minimize skew in the DCLK signal because this can lead to timing violations in the serial interface specifications. See the *Cascading Multiple Converters* section for more details.

Data Valid ($\overline{\text{DVALID}}$)

The $\overline{\text{DVALID}}$ signal indicates that data is ready. Data retrieval may begin after $\overline{\text{DVALID}}$ goes low. This signal is generated using an internal clock divided down from the system clock, CLK. The phase relationship between this internal clock and CLK is set when power is first applied and is random. Since the user must synchronize CONV with CLK, the $\overline{\text{DVALID}}$ signal will have a random phase relationship with CONV. This uncertainty is ± $1/f_{CLK}$. Polling $\overline{\text{DVALID}}$ eliminates any concern about this relationship. If data read back is timed from CONV, wait the maximum value of t_7 or t_8 to insure data is valid.

Reset ($\overline{\text{RESET}}$)

The DDC232 is reset asynchronously by taking the $\overline{\text{RESET}}$ input low, as shown in Figure 9. Make sure the release pulse is at least 1µs wide. After resetting the DDC232, wait at least four conversions before using the data. It is very important that $\overline{\text{RESET}}$ is glitch-free to avoid unintentional resets.

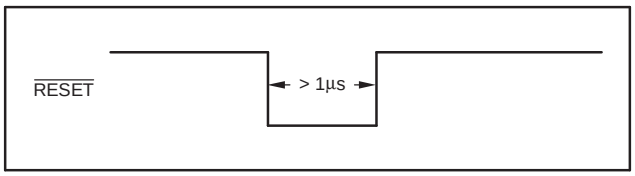


Figure 9. Reset Timing

Conversion Rate

The conversion rate of the DDC232 is set by a combination of the integration time (determined by the user) and the speed of the A/D conversion process. The A/D conversion time is primarily a function of the system clock (CLK) speed. One A/D conversion cycle encompasses the conversion of two signals (one side of each dual integrator feeding the modulator) and the reset time for each of the integrators involved in the two conversions. In most situations, the A/D conversion time is shorter than the integration time. If this condition exists, the DDC232 will operate in the continuous mode. When the DDC232 is in the continuous mode, the sensor output is continuously integrated by one of the two sides of each input.

In the event that the A/D conversion takes longer than the integration time, the DDC232 will switch into a non-continuous mode. In non-continuous mode, the A/D converter is not able to keep pace with the speed of the integration process. Consequently, the integration process is periodically halted until the digitizing process catches up. These two basic modes of operation for the DDC232—continuous and non-continuous modes—are described below.

Continuous and Non-Continuous Operational Modes

Figure 10 shows the state diagram of the DDC232. In all, there are eight states. Table 4 provides a brief explanation of each state.

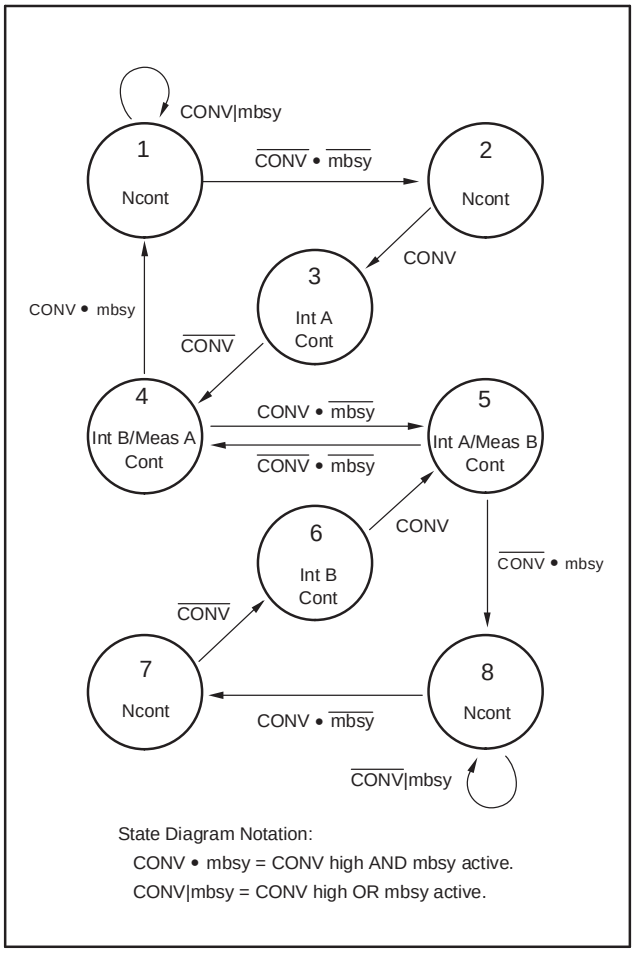


Figure 10. Integrate/Measure State Diagram

Four signals are used to control progression around the state diagram: CONV, mbsy, and their complements. The state machine uses the level as opposed to the edges of CONV to control the progression. mbsy is an internally-generated signal not available to the user. It is active whenever a measurement/reset/auto-zero (m/r/az) cycle is in progress.

During the continuous (cont) mode, mbsy is not active when CONV toggles. The non-integrating side is always ready to begin integrating when the other side finishes its integration. Consequently, monitoring the current status of CONV is all that is needed to know the current state. Cont mode operation corresponds to states 3–6. Two of the states, 3 and 6, only perform an integration (no m/r/az cycle).

mbsy becomes important when operating in the non-continuous (ncont) mode (states 1, 2, 7, and 8). Whenever CONV is toggled while mbsy is active, the DDC232 will enter or remain in either ncont state 1 (or 8). After mbsy goes inactive, state 2 (or 7) is entered. This state prepares the appropriate side for integration. In the ncont states, the inputs to the DDC232 are grounded.

One interesting observation from the state diagram is that the integrations always alternate between sides A and B. This relationship holds for any CONV pattern and is independent of the mode. States 2 and 7 insure this relationship during the ncont mode.

When power is first applied to the DDC232, the beginning state is either 1 or 8, depending on the initial level of CONV. For CONV held high at power-up, the beginning state is 1. Conversely, for CONV held low at power-up, the beginning state is 8. In general, there is a symmetry in the state diagram between states 1–8, 2–7, 3–6, and 4–5. Inverting CONV results in the states progressing through their symmetrical match.

Table 4. State Descriptions

STATE	MODE	DESCRIPTION
1	Ncont	Complete m/r/az of side A, then side B (if previous state is state 4). Initial power-up state when CONV is initially held High.
2	Ncont	Prepare side A for integration.
3	Cont	Integrate on side A.
4	Cont	Integrate on side B; m/r/az on side A.
5	Cont	Integrate on side A; m/r/az on side B.
6	Cont	Integrate on side B.
7	Ncont	Prepare side B for integration.
8	Ncont	Complete m/r/az of side B, then side A (if previous state is state 5). Initial power-up state when CONV is initially held Low.

TIMING EXAMPLES

Continuous Mode

A few timing diagrams help illustrate the operation of the integrate/measure state machine. These diagrams are shown in Figure 11 through Figure 16. Table 5 gives generalized timing specifications in units of CLK periods for Clk_4x = 0. If Clk_4x = 1, these values increase by a factor of 4 because of the internal clock divider. Values (in µs) for Table 5 can be easily found for a given CLK.

Figure 11 shows a few integration cycles beginning with initial power-up for a cont mode example. The top signal is CONV and is supplied by the user. The next line indicates the current state in the state diagram. The following two traces show when integrations and measurement cycles are underway. The internal signal mbsy is shown next. Finally, $\overline{\text{DVALID}}$ is given. As described in the data sheet, $\overline{\text{DVALID}}$ goes active low when data is ready to be retrieved from the DDC232. It stays low until DCLK is taken high and then back low by the user. The text below the $\overline{\text{DVALID}}$ pulse indicates the side of the data available to be read and arrows help match the data to the corresponding integration.

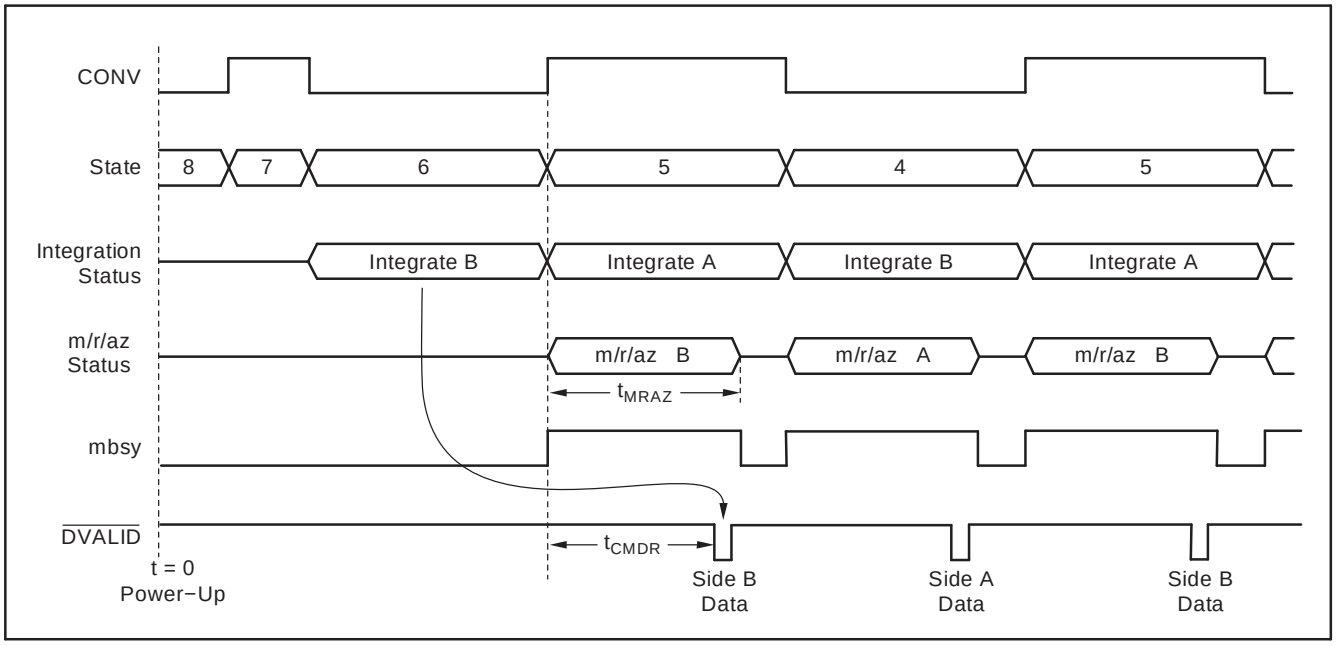


Figure 11. Continuous Mode Timing

Table 5. Timing Specifications Generalized in CLK Periods

SYMBOL	DESCRIPTION	VALUE (CLK periods with Clk_4x = 0)	
		Low-Power Mode	High-Speed Mode
t_{MRAZ}	Cont mode m/r/az cycle	1552 ± 2	1612 ± 2
t_{CMDR}	Cont mode data ready	1382 ± 2	1382 ± 2
t_{NCDR1}	1st ncont mode data ready	TBD	TBD
t_{NCDR2}	2nd ncont mode data ready	TBD	TBD
t_{NCMRAZ}	Ncont mode m/r/az cycle	TBD	TBD

In Figure 11, the first state is ncont state 8. The DDC232 always powers up in the ncont mode. In this case, the first state is 8 because CONV is initially low. After the first two states, cont mode operation is reached and the states begin toggling between 4 and 5. From now on, the input is being continuously integrated, either on side A or side B. The time needed for the m/r/az cycle, t_{MRAZ}, is the same time that determines the boundary between the cont and ncont modes described earlier in the Overview section. $\overline{DVALID}$ goes low after CONV toggles in time t_{CMDR}, indicating that data is ready to be retrieved.

See Figure 12 for the timing diagram of the internal operations occurring during continuous mode operation. Table 6 gives the timing specifications of the internal operations occurring during continuous mode operation.

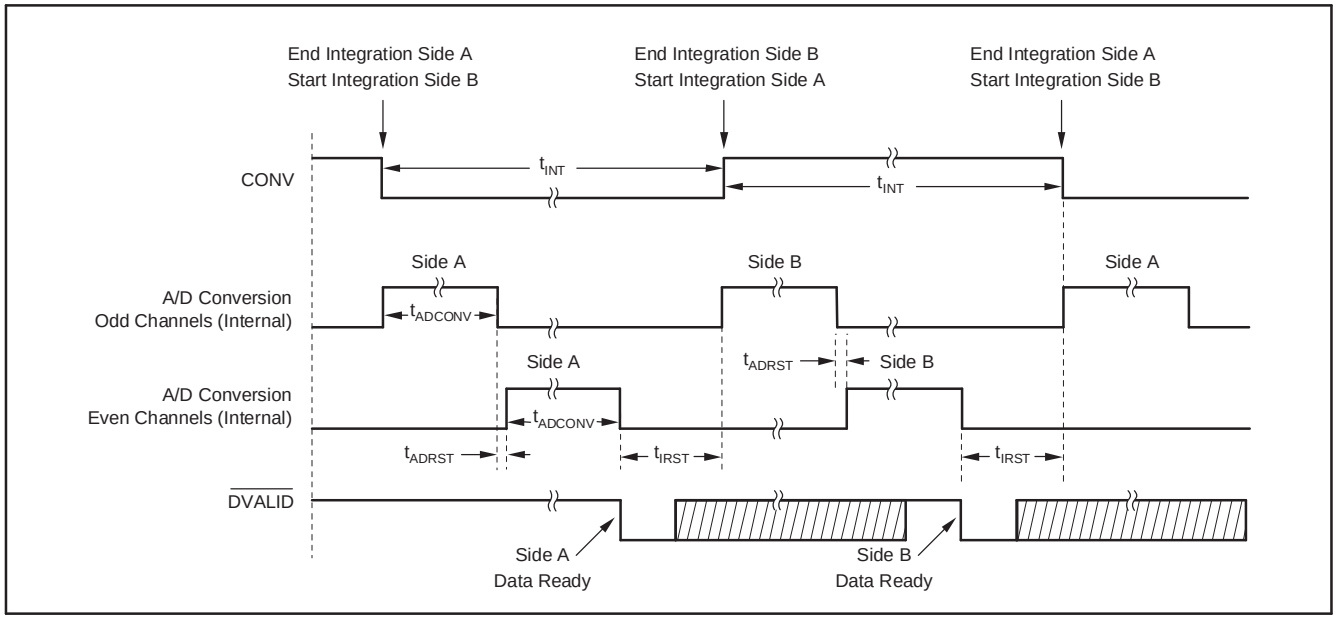


Figure 12. Timing Diagram for DDC232 Internal Operation in Continuous Mode

Table 6. Timing for the Internal Operation in Continuous Mode

SYMBOL	DESCRIPTION	Low-Power Mode (CLK = 5MHz)			High-Speed Mode (CLK = 9.6MHz)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{INT}	Integration Period (continuous mode)	320		1,000,000	162		1,000,000	µs
t_{ADCONV}	A/D Conversion Time (internally controlled)		135.6			TBD		µs
t_{ADRST}	A/D Conversion Reset Time (internally controlled)		3.2			TBD		µs
t_{IRST}	Integrator Reset Time (internally controlled)		36			TBD		µs

Non-Continuous Mode

Figure 13 and Figure 14 illustrate operation in non-continuous mode.

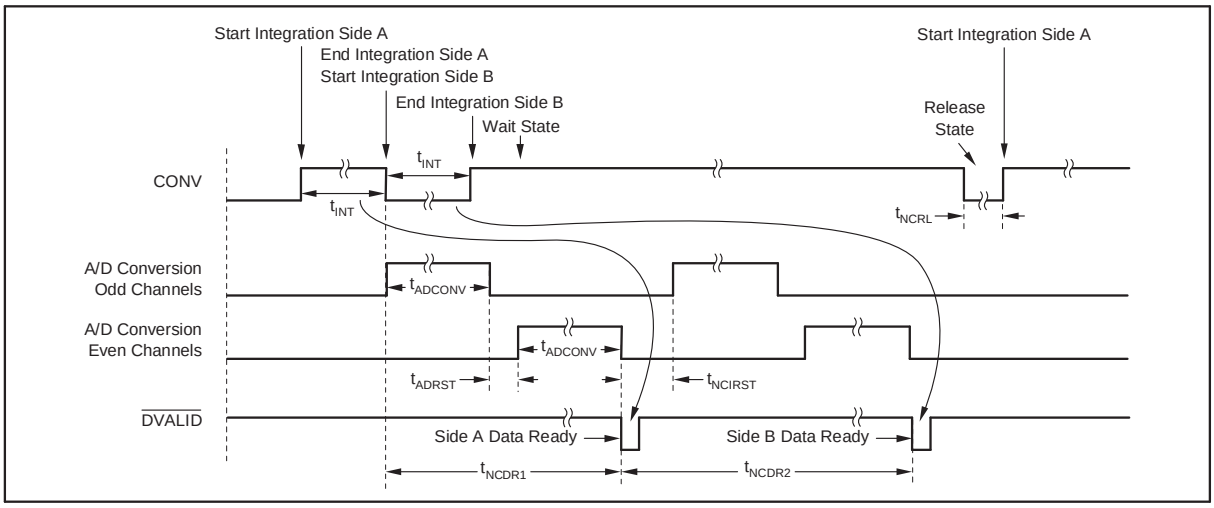


Figure 13. Conversion Detail for the Internal Operation of Non-Continuous Mode with Side A Integrated First

Table 7. DDC232 Internal Timing in Non-Continuous Mode

SYMBOL	DESCRIPTION	CLK = 5MHz, Clk_4x = 0			UNITS
		MIN	TYP	MAX	
t_{INT}	Integration Time (non-continuous mode)	TBD		1,000,000	µs
t_{ADCONV}	A/D Conversion Time (internally controlled)		135.6		µs
t_{ADRST}	A/D Conversion Reset Time (internally controlled)		3.2		µs
t_{NCIRST}	Non-Continuous Mode Integrator Reset Time (internally controlled)		TBD		µs
t_{NCRL}	Release Time	TBD			µs
t_{NCDR1}	1st Non-Continuous Mode Data Ready		TBD		
t_{NCDR2}	2nd Non-Continuous Mode Data Ready		TBD		

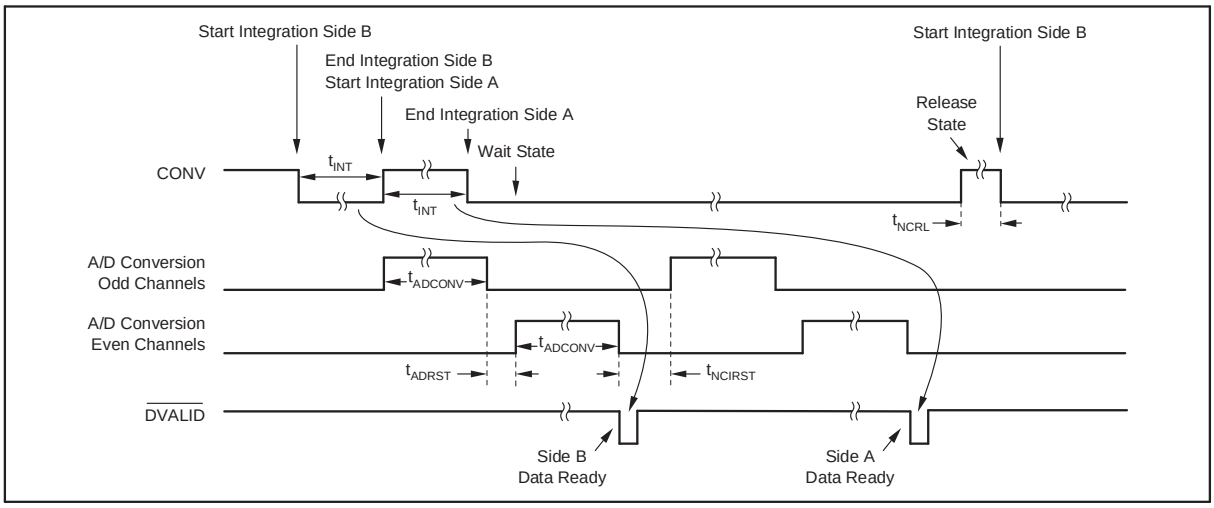


Figure 14. Internal Operation Timing Diagram Non-Continuous Mode with Side B Integrated First

Changing Between Modes

Changing from cont to ncont mode occurs whenever $t_{INT} < t_{MRAZ}$. Figure 15 shows an example of this transition. In this figure, cont mode is entered when the integration on side A is completed before the m/r/az cycle on side B is complete. The DDC232 completes the measurement on sides B and A during states 8 and 7 with the input signal shorted to ground. Ncont integration begins with state 6.

Changing from ncont to cont mode occurs when t_{INT} is increased so that t_{INT} is always $\geq t_{MRAZ}$ as shown in Figure 16 (see Figure 13 and Table 7, page 18). With a longer t_{INT}, the m/r/az cycle has enough time to finish before the next integration begins and continuous integration of the input signal is possible. For the special case of the very first integration when changing to the cont mode, t_{INT} can be $< t_{MRAZ}$. This is allowed because there is no simultaneous m/r/az cycle on the side B during state 3—therefore, there is no need to wait for it to finish before ending the integration on side A.

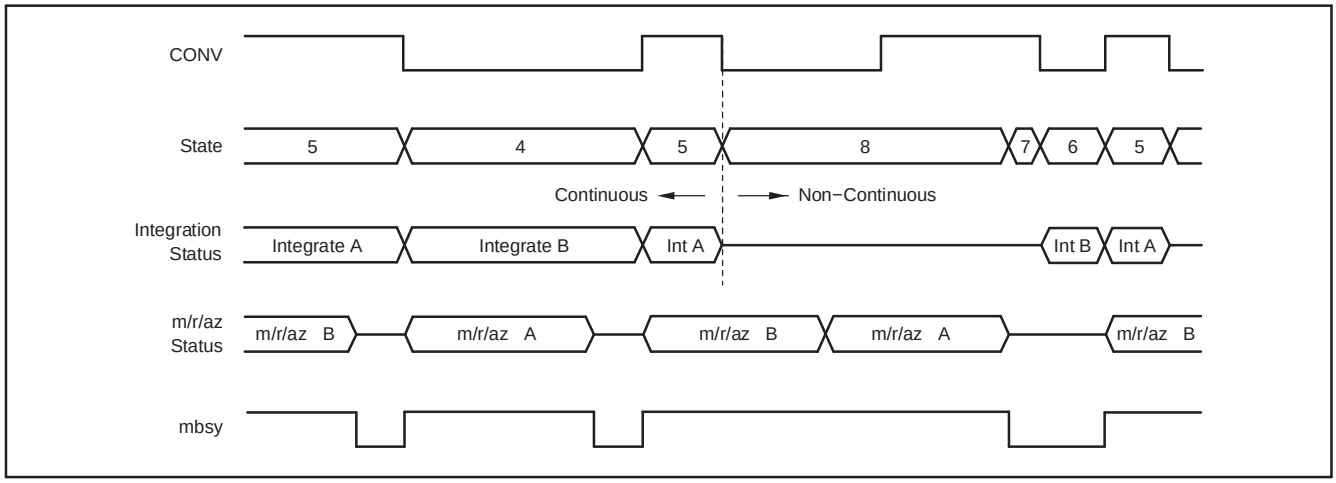


Figure 15. Changing from Continuous Mode to Non-Continuous Mode

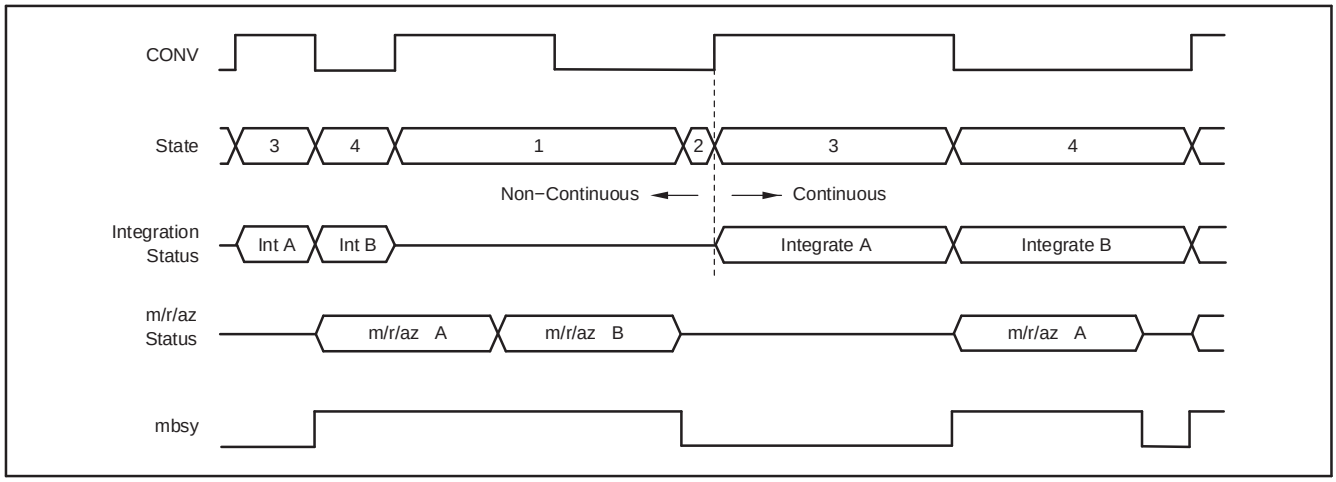


Figure 16. Changing from Non-Continuous Mode to Continuous Mode

DATA FORMAT

The serial output data is provided in an offset binary code as shown in Table 8. The Format bit in the configuration register selects how many bits are used in the output word. When Format = 1, 20 bits are used. When Format = 0, the lower 4 bits are truncated so that only 16 bits are used. Note that the LSB size is 16 times bigger when Format = 0. An offset is included in the output to allow slightly negative inputs (for example, from board leakages) from clipping the reading. This offset is approximately 0.4% of the positive full-scale.

Table 8. Ideal Output Code(1) vs Input Signal

INPUT SIGNAL	IDEAL OUTPUT CODE FORMAT = 1	IDEAL OUTPUT CODE FORMAT = 0
≥ 100% FS	1111 1111 1111 1111 1111	1111 1111 1111 1111
0.001531% FS	0000 0001 0000 0001 0000	0000 0001 0000 0001
0.001436% FS	0000 0001 0000 0000 1111	0000 0001 0000 0000
0.000191% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000096% FS	0000 0001 0000 0000 0001	0000 0001 0000 0000
0% FS	0000 0001 0000 0000 0000	0000 0001 0000 0000
–0.3955% FS	0000 0000 0000 0000 0000	0000 0000 0000 0000

(1) Excludes the effects of noise, INL, offset, and gain errors.

DATA RETRIEVAL

In both the continuous and non-continuous modes of operation, the data from the last conversion is available for retrieval on the falling edge of $\overline{\text{DVALID}}$ (see Figure 17 and Table 9). Data is shifted out on the falling edge of the data clock, DCLK.

Make sure not to retrieve data around changes in CONV because this can introduce noise. Stop activity on DCLK at least 10µs before or after a CONV transition.

Setting the Format bit = 0 (16-bit output word) will reduce the time needed to retrieve data by 20% since there are fewer bits to shift out. This can be useful in multichannel systems requiring only 16 bits of resolution.

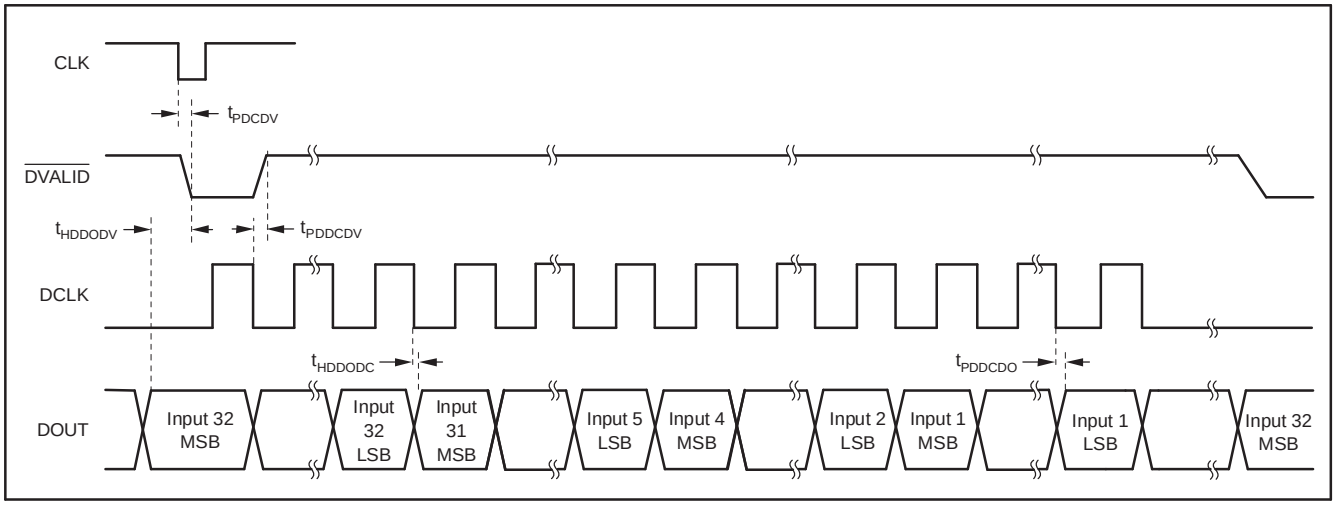


Figure 17. Digital Interface Timing Diagram for Data Retrieval From a Single DDC232

Table 9. Timing for DDC232 Data Retrieval

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PDCDV}	Propagation Delay from Falling Edge of CLK to $\overline{\text{DVALID}}$ Low	10			ns
t_{PDDCDV}	Propagation Delay from Falling Edge of DCLK to $\overline{\text{DVALID}}$ High	5			ns
t_{HDDODV}	Hold Time that DOUT is Valid Before the Falling Edge of $\overline{\text{DVALID}}$		400		ns
t_{HDDODC}	Hold Time that DOUT is Valid After Falling Edge of DCLK	4			ns
t_{PDDCDO} (1)	Propagation Delay from Falling Edge of DCLK to Valid DOUT			25	ns

(1) With a maximum load of one DDC232 (4pF typical) with an additional load of 5pF.

Cascading Multiple Converters

Multiple DDC232 units can be connected in serial configuration; see Figure 18.

DOUT can be used with DIN to daisy-chain multiple DDC232 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC232s; see Figure 18.

Figure 19 shows the timing diagram when the DIN input is used to daisy-chain several devices. Table 10 gives the timing specification for data retrieval using DIN.

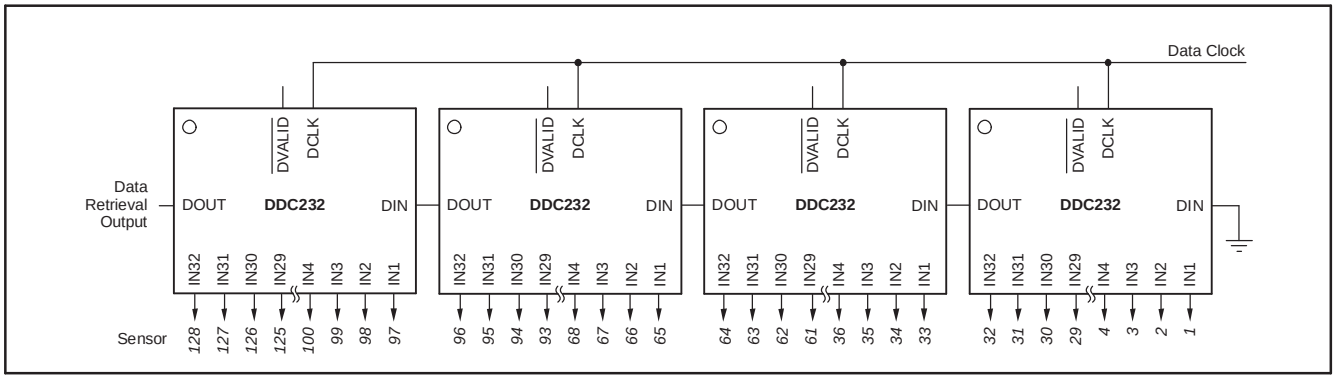


Figure 18. Daisy-Chained DDC232s

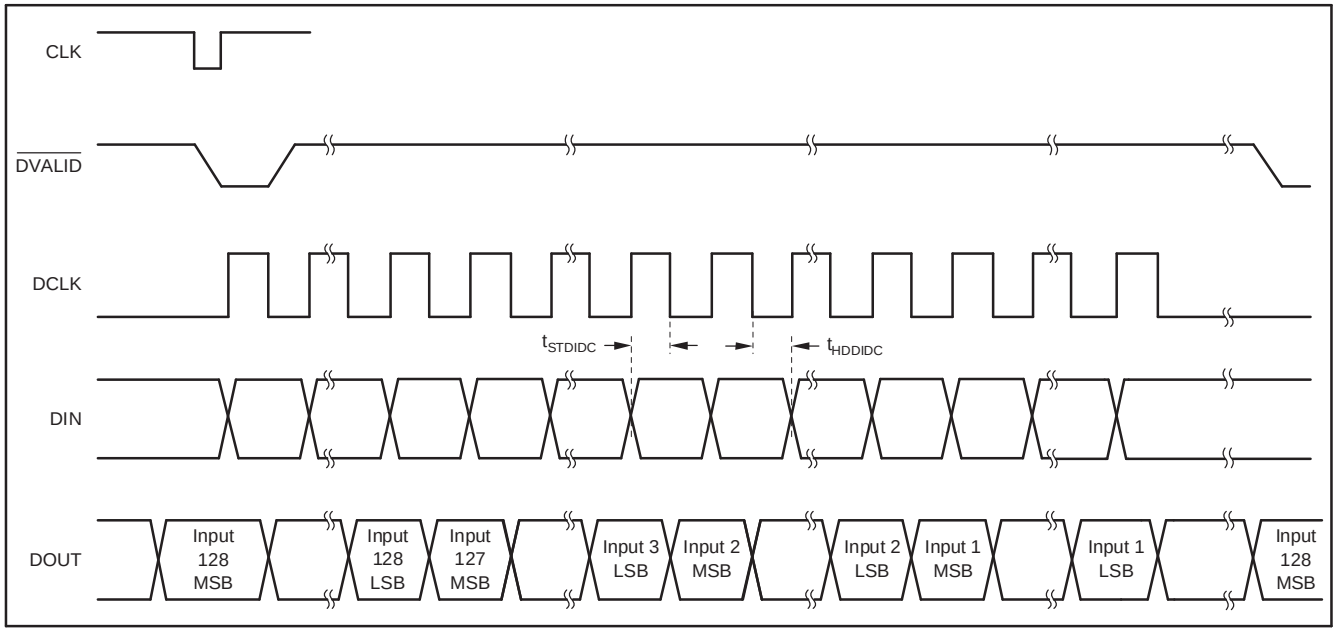


Figure 19. Timing Diagram When Using DDC232 DIN Function; See Figure 18

Table 10. Timing for DDC232 Data Retrieval Using DIN

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{STDIDC}	Set-Up Time from DIN to Falling Edge of DCLK	10			ns
t_{HDDIDC}	Hold Time for DIN After Falling Edge of DCLK	10			ns

RETRIEVAL *BEFORE* CONV TOGGLES (CONTINUOUS MODE)

Data retrieval before CONV toggles is the most straightforward method. Data retrieval begins soon after $\overline{\text{DVALID}}$ goes low and finishes before CONV toggles, as shown in Figure 20. For best performance, data retrieval must stop t_{SDCV} before CONV toggles. This method is most appropriate for longer integration times. The maximum time available for readback is $t_{INT} - t_{CMDR} - t_{SDCV}$. For DCLK = 10MHz and CLK = 5MHz, the maximum number of DDC232s that can be daisy-chained together (FORMAT = 1) is calculated by Equation 1:

$$\frac{t_{INT} - (t_{CMDR} + t_{SDCV})}{(20 \times 32)\tau_{DCLK}} \quad (1)$$

NOTE: $(16 \times 32)\tau_{DCLK}$ is used for FORMAT = 0, where t_{DCLK} is the period of the data clock. For example, if t_{INT} = 1000µs and DCLK = 10MHz, the maximum number of DDC232s with FORMAT = 1 is shown in Equation 2:

$$\frac{1000\mu s - 286.8\mu s}{(640)(100ns)} = 11.14 \rightarrow 11 \text{ DDC232} \quad (2)$$

(or 13 for FORMAT = 0)

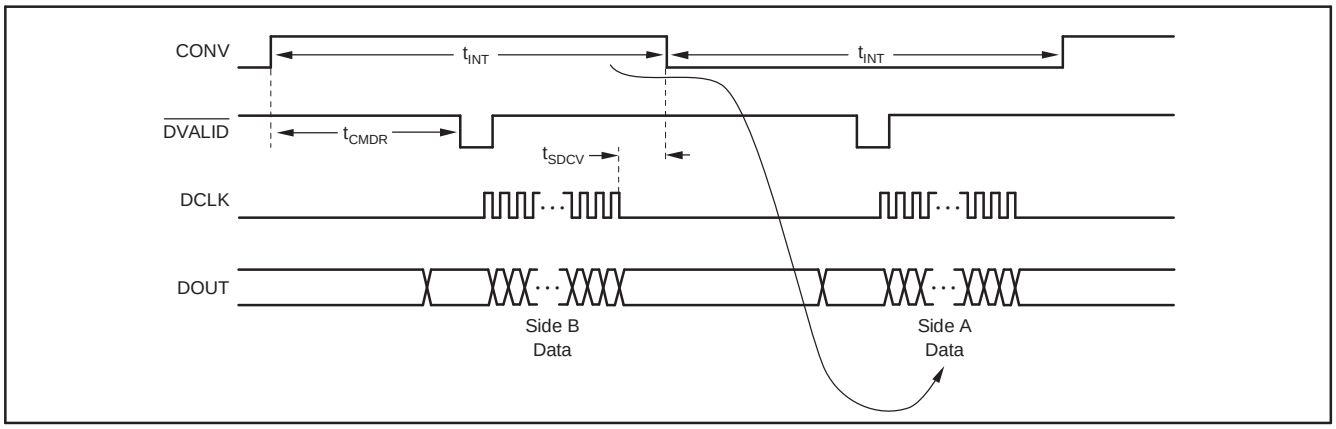


Figure 20. Readback *Before* CONV Toggles

Table 11. Timing for Readback

SYMBOL	DESCRIPTION	CLK = 5MHz, Clk_4x = 0			UNITS
		MIN	TYP	MAX	
t_{SDCV}	Data Retrieval Shutdown Before or After Edge of CONV	10			µs

RETRIEVAL *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data is ready. Data retrieval must wait t_{SDCV} after CONV toggles before beginning. See Figure 21 for an example of this. The maximum time available for retrieval is $t_{CMDR} - (t_{SDCV} + t_{HDDODV})$, regardless of t_{INT}. The maximum number of DDC232s that can be daisy-chained together with FORMAT = 1 is calculated by Equation 3:

$$\frac{266\mu s}{(20 \times 32)\tau_{DCLK}} \quad (3)$$

NOTE: $(16 \times 32)\tau_{DCLK}$ is for FORMAT = 0.

For DCLK = 10MHz, the maximum number of DDC232s is 4 (or 5 for FORMAT = 0).

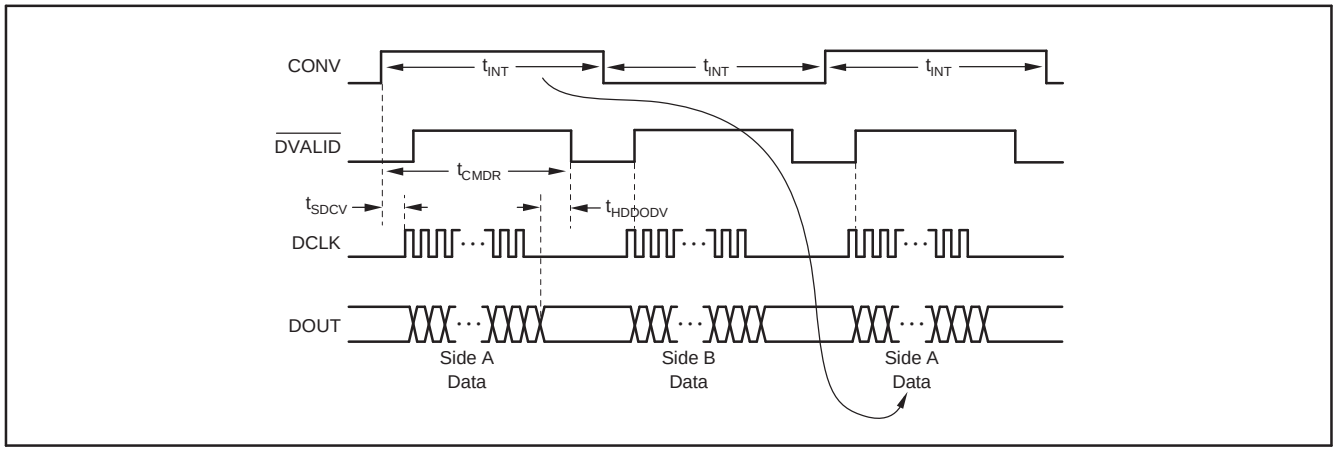


Figure 21. Readback *After* CONV Toggles

RETRIEVAL *BEFORE* AND *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For the absolute maximum time for data retrieval, data can be retrieved before and after CONV toggles. Nearly all of t_{INT} is available for data retrieval. Figure 22 illustrates how this is done by combining the two previous methods. Pause the retrieval during CONV toggling to prevent digital noise, as discussed previously, and finish before the next data is ready. The maximum number of DDC232s that can be daisy-chained together with FORMAT = 1 is:

$$\frac{t_{INT} - (t_{SDCV} + t_{SDCV} + t_{HDDODV})}{(20 \times 32)\tau_{DCLK}} \quad (4)$$

NOTE: $(16 \times 32)\tau_{DCLK}$ is used for FORMAT = 0.

For t_{INT} = 400µs and DCLK = 10MHz, the maximum number of DDC232s is 5 (or 7 for FORMAT = 0).

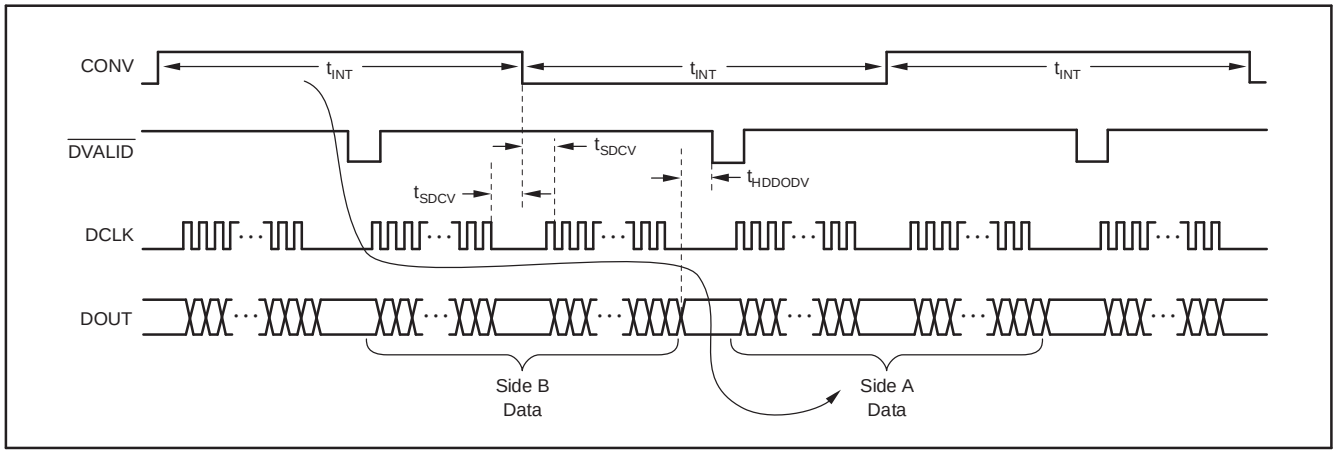


Figure 22. Readback *Before* and *After* CONV Toggles

RETRIEVAL: NON-CONTINUOUS MODE

Retrieving in non-continuous mode is slightly different as compared with the continuous mode. As illustrated in Figure 23, $\overline{\text{DVALID}}$ goes low in time t_{NCDR1} after the first integration completes. If t_{INT} is shorter than this time, all of t_{NCDR2} is available to retrieve data before the other side data is ready. For $t_{INT} > t_{NCDR1}$, the first integration data is ready before the second integration completes. Data retrieval must be delayed until the second integration completes, leaving less time available for retrieval. The time available is $t_{NCDR2} - (t_{INT} - t_{NCDR1})$. Data from the second integration must be retrieved before the next round of integration begins. This time is highly dependent on the pattern used to generate CONV. As with the continuous mode, data retrieval must halt before and after CONV toggles (t_{SDCV}) and be completed before new data is ready (t_{HDDODV}).

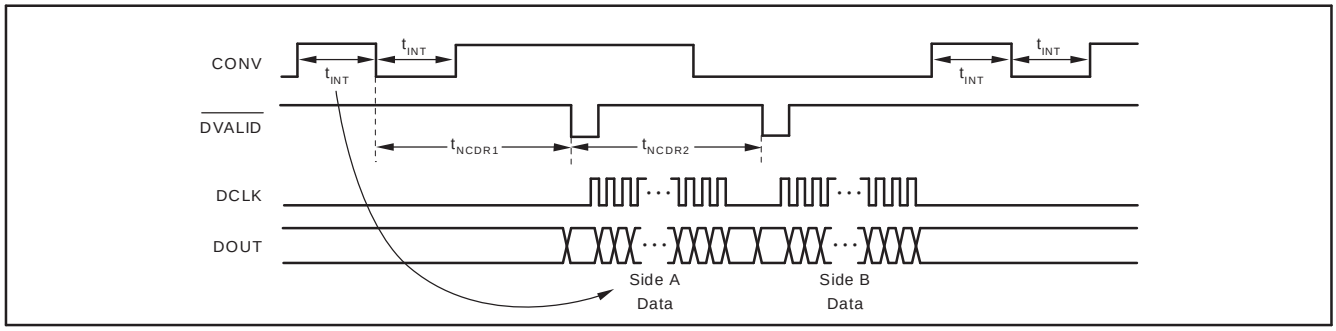


Figure 23. Readback in Non-Continuous Mode

POWER-UP SEQUENCING

Prior to power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 24. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then give a $\overline{RESET}$ pulse. After releasing $\overline{RESET}$, the configuration register must be programmed. Table 12 shows the timing for the power-up sequence.

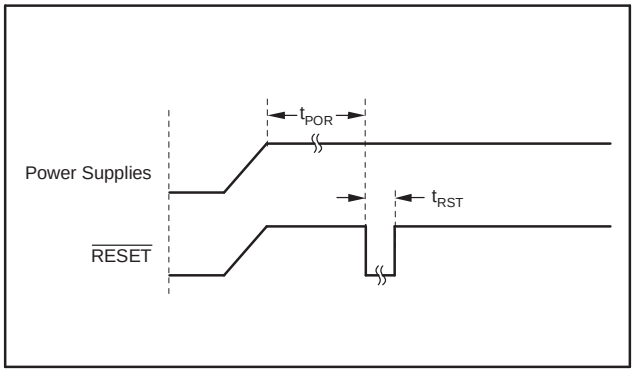


Figure 24. DDC232 Timing Diagram at Power-Up

Table 12. Timing for DDC232 Power-Up Sequence

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{POR}	Wait After Power-Up Until Reset	250			ms
t_{RST}	Reset Low Width	1			µs

LAYOUT

POWER SUPPLIES AND GROUNDING

Both AVDD and DVDD should be as quiet as possible. It is particularly important to eliminate noise from AVDD that is non-synchronous with the DDC232 operation. Figure 25 illustrates how to supply power to the DDC232. Each supply of the DDC232 should be bypassed with 10µF solid tantalum capacitors. It is recommended that both the analog and digital grounds (AGND and DGND) be connected to a single ground plane on the printed circuit board (PCB).

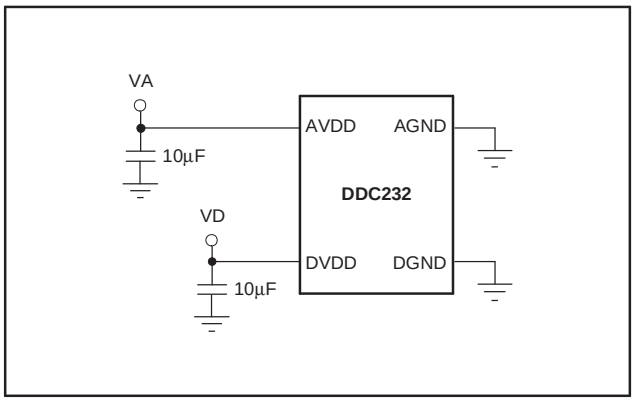


Figure 25. Power-Supply Connections

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout will ensure the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and QGND. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The QGND pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the DDC232 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DDC232CGXGR	ACTIVE	BGA	GXG	64	1000	TBD	SN/PB	Level-3-240C-168 HR
DDC232CGXGT	ACTIVE	BGA	GXG	64	250	TBD	SN/PB	Level-3-240C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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