0.25-Ω CMOS, 1.65-V to 4.3-V, Dual DPDT Analog Switch

FEATURES

- Low Voltage Operation (1.65 V to 4.3 V)
- Low On-Resistance - $r_{ON:}$ 0.25 Ω @ 2.7 V
- Fast Switching: t_{ON} = 28 ns
  t_{OFF} = 17 ns
- QFN-16 (3x3) Package
- Latch-Up Current >300 mA (JESD78)

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8-V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

DESCRIPTION

The DG2799 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2799 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

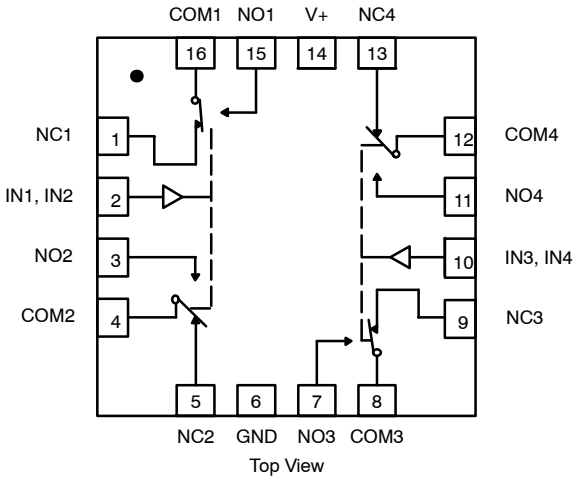
The DG2799 is built on Vishay Siliconix's low voltage process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured in QFN packages, the lead (Pb)-free "–E3/E4" suffix is being used as a designator. Lead (Pb)-free QFN products purchased at any time will have either a nickel-palladium-gold device termination or a 100% matte tin device termination. The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2799
QFN-16 (3 X 3)



Top View

NOTE:

Underside exposed pad has no device electrical connection. It is recommended that no electrical connection is made to it.

TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	16-Pin QFN (3 x 3 mm) Variation 2	DG2799DN-T1—E3/E4

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ . . . . . -0.3 to +5.0 V

IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)

Current (Any terminal except NO, NC or COM) . . . . . 30 mA

Continuous Current (NO, NC, or COM) . . . . . ±300 mA

Peak Current . . . . . ±500 mA

(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) . . . . . -65 to 150°C

Package Solder Reflow Conditions[d]

16-Pin QFN (3 x 3 mm) . . . . . 250°C

Power Dissipation (Packages)[b]

QFN-16[c] . . . . . 1385 mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 17.3 mW/°C above 70°C
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 1.8 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, V_{IN} = 0.4 or 1.1 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 1.8 V, V_{COM} = 0.2 V/0.9 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.47	1.3 1.4	Ω
Digital Control							
Input High Voltage	V_{INH}		Full	1.1			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room Full		62	94 97	ns
Turn-Off Time	t_{OFF}		Room Full		24	52 55	
Break-Before-Make Time	t_d		Full	8			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		66		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		−74		dB
Crosstalk[d]	X_{TALK}		Room		−74		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		108		pF
	$C_{NC(off)}$		Room		108		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		240		
	$C_{NC(on)}$		Room		240		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	µA

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.5 or 1.4 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.3	0.45 0.55	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.7 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.07	0.15	
r_{ON} Match[d]	Δr_{ON}		Room		0.05		
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3.0 V V_{COM} = 3.0 V/0.3 V	Room Full	−1 −10		1 10	nA
	$I_{COM(off)}$		Room Full	−1 −10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3.0 V	Room Full	−1 −10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	c_{in}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	μA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room Full		28	57 60	ns
Turn-Off Time	t_{OFF}		Room Full		17	45 47	
Break-Before-Make Time	t_d		Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		160		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		−75		dB
Crosstalk[d]	X_{TALK}		Room		−75		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		102		pF
	$C_{NC(off)}$		Room		102		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		234		
	$C_{NC(on)}$		Room		234		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	μA

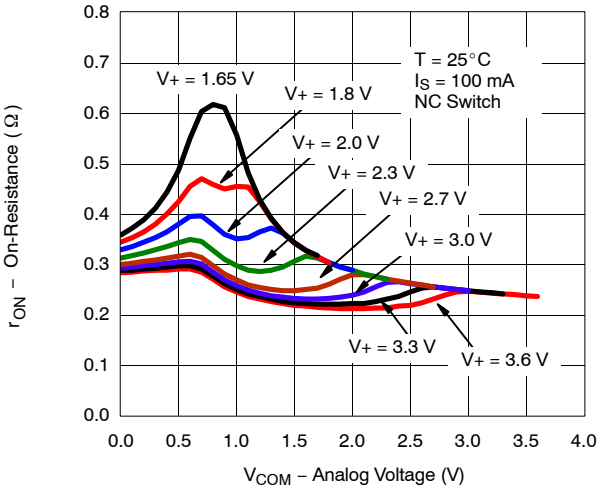
SPECIFICATIONS (V+ = 4.3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 4.3 V, V_{IN} = 0.5 or 1.6 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.3 V, V_{COM} = 0.5 V/2.1 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.29	0.43 0.53	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 4.3 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.07	0.15	
r_{ON} Match[d]	Δr_{ON}		Room		0.05		
Switch Off Leakage Current[d]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 4.3 V, V_{NO}, V_{NC} = 0.3 V/4.0 V V_{COM} = 4.0 V/0.3 V	Room Full	−10 −100		10 100	nA
	$I_{COM(off)}$		Room Full	−10 −100		10 100	
Channel-On Leakage Current[d]	$I_{COM(on)}$	V+ = 4.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/4.0 V	Room Full	−10 −100		10 100	
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	µA
Dynamic Characteristics							
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		320		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		−73		dB
Crosstalk[d]	X_{TALK}		Room		−73		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		100		pF
	$C_{NC(off)}$		Room		100		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		230		
	$C_{NC(on)}$		Room		230		
Power Supply							
Power Supply Range	V+					4.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	µA

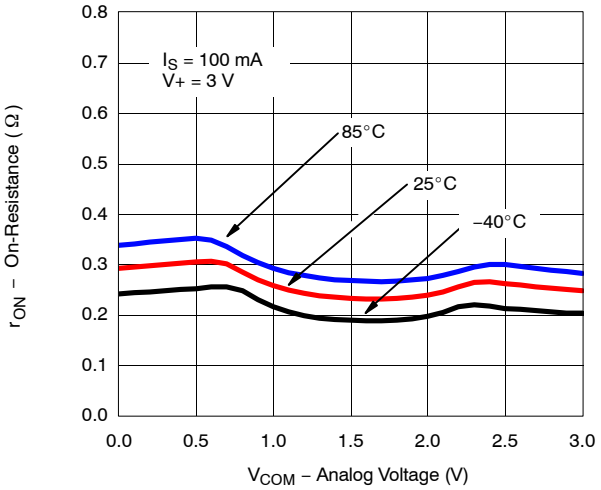
Notes:
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

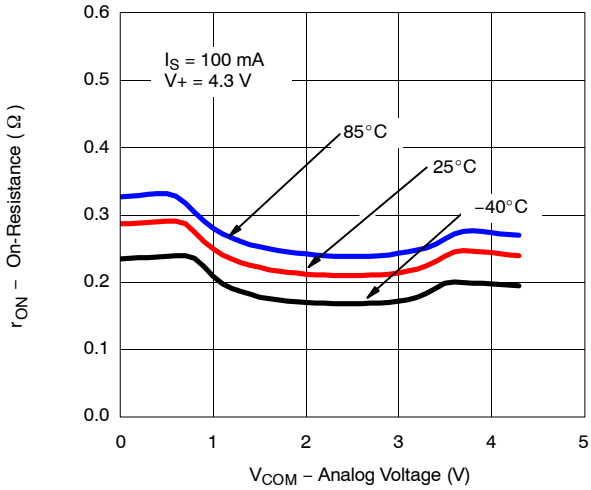
r_{ON} vs. V_{COM} and Supply Voltage



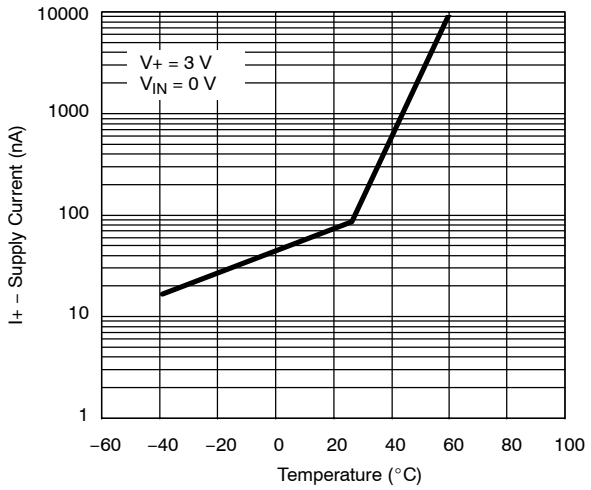
r_{ON} vs. Analog Voltage and Temperature



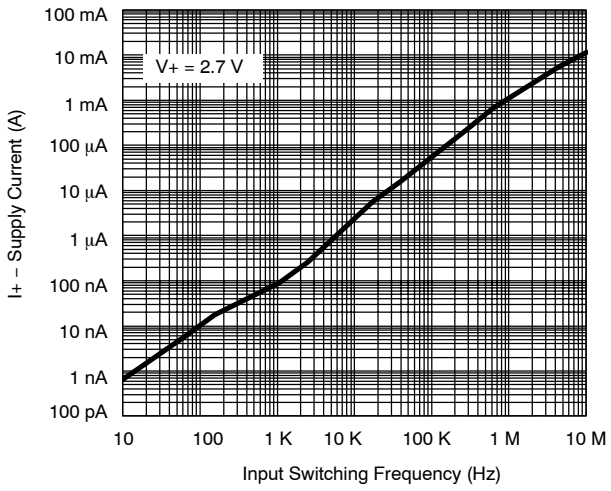
r_{ON} vs. Analog Voltage and Temperature



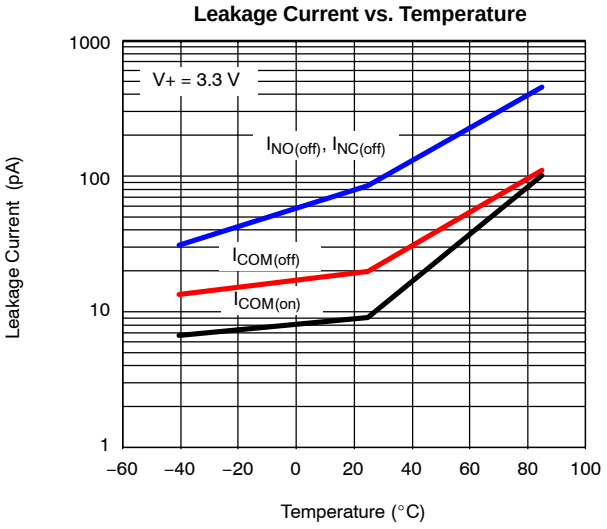
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

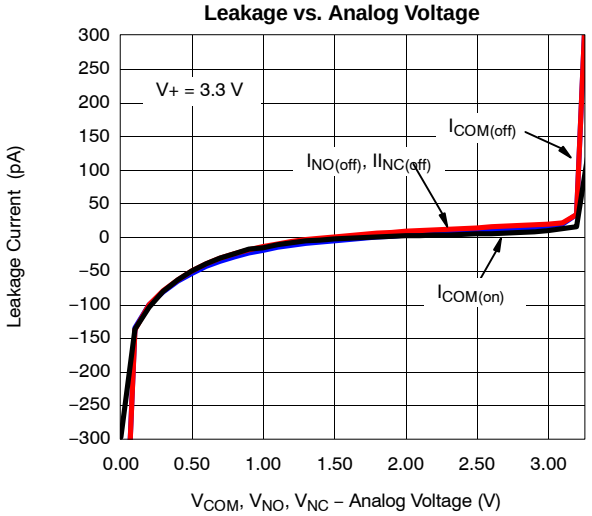


Leakage Current vs. Temperature

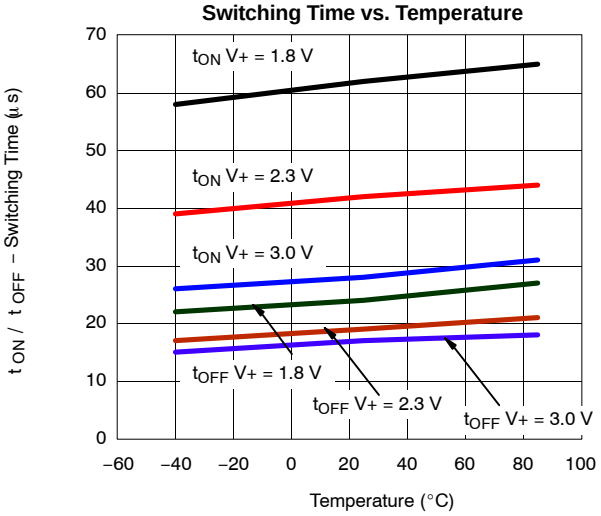


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

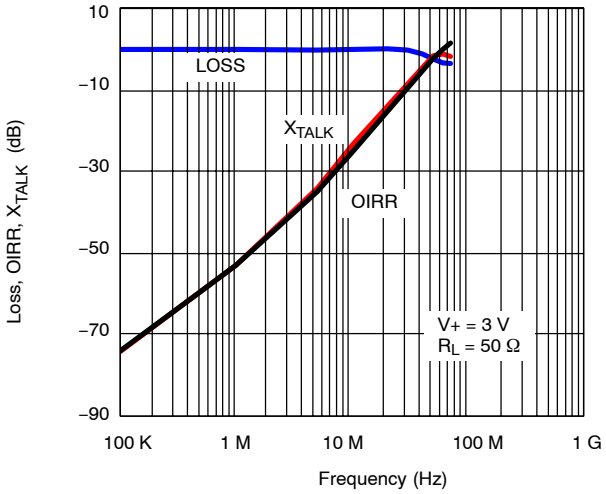
Leakage vs. Analog Voltage



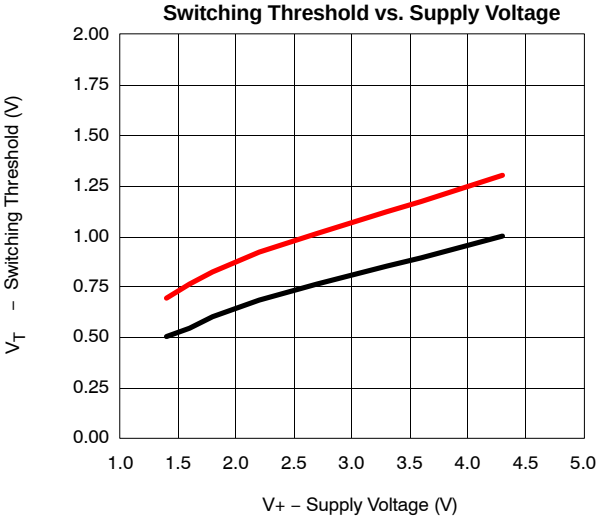
Switching Time vs. Temperature



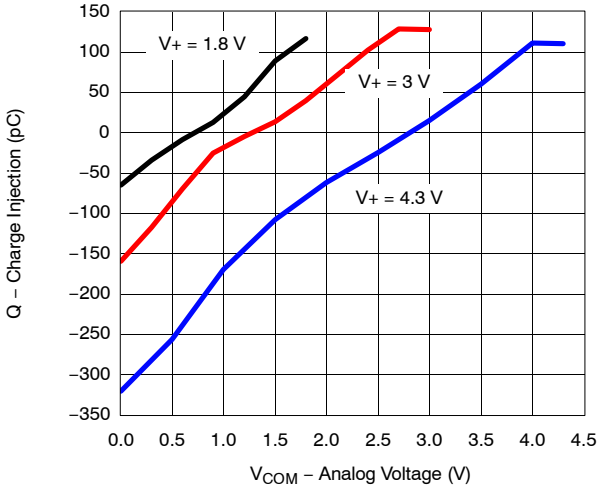
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



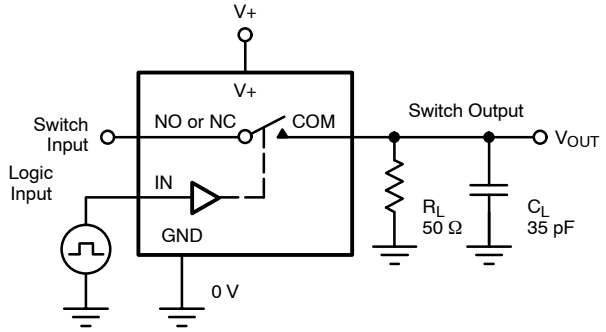
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

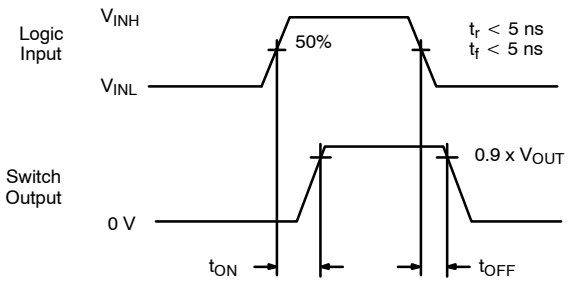


TEST CIRCUITS



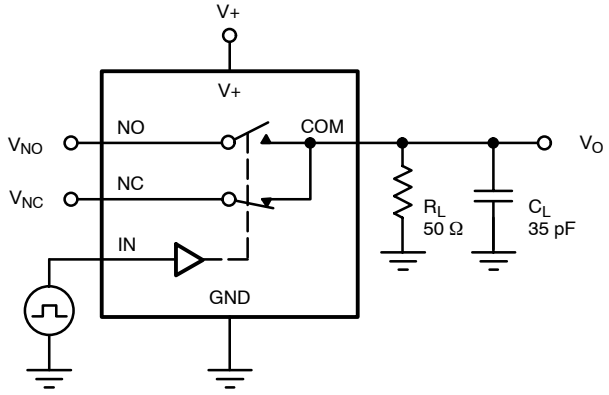
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

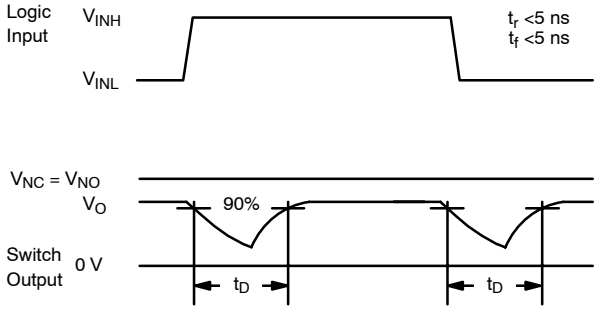
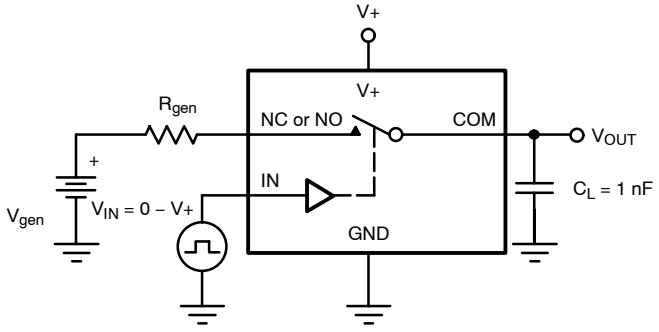
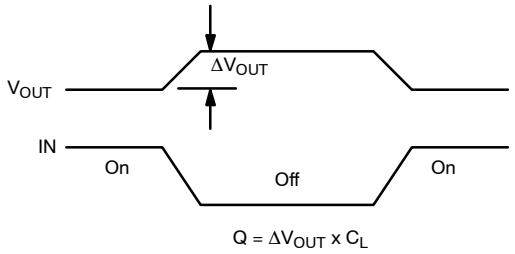


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

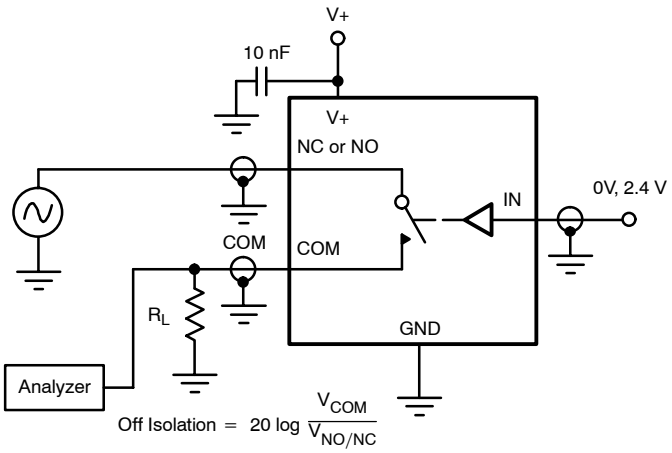


Figure 4. Off-Isolation

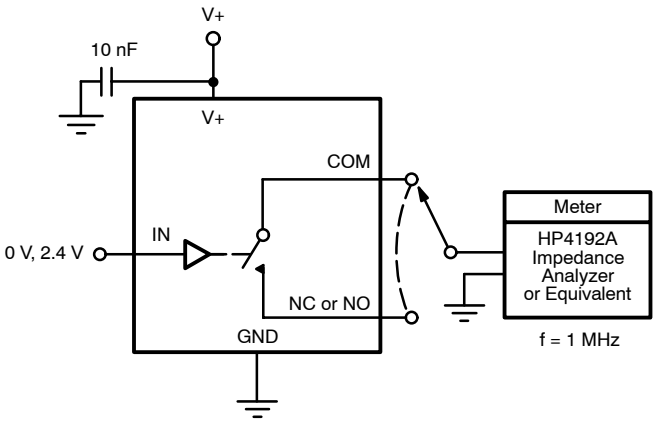


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73162.