

## CMOS Analog Switches

### FEATURES

- $\pm 15\text{-V}$  Input Range
- Fast Switching— $t_{ON}$ : 110 ns
- Low  $r_{DS(on)}$ : 30  $\Omega$
- Single Supply Operation
- CMOS Logic Levels
- Micropower: 30 nW

### BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

### APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

### DESCRIPTION

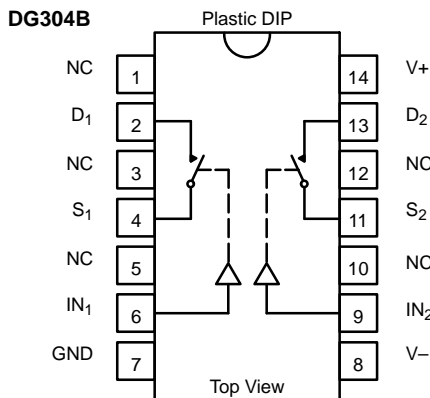
The DG304B, DG306B and DG307B monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat on-resistance over the entire analog range.

applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is allowed by connecting the  $V^-$  rail to 0 V.

Designed on the Vishay Siliconix PLUS-40 CMOS process to achieve low power consumption and excellent on/off switch performance, these switches are ideal for battery powered

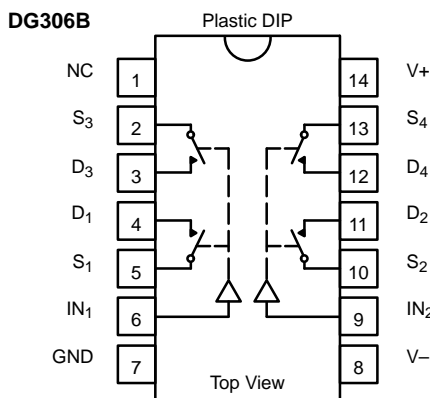
Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS input compatible.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

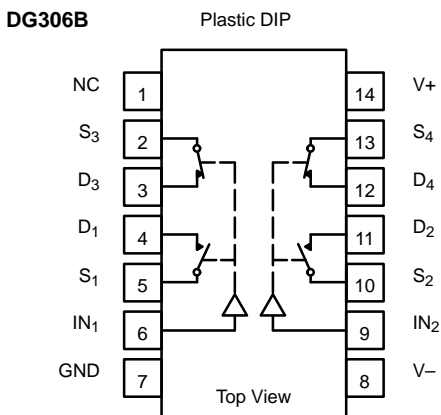
Logic "0"  $\leq 3.5\text{ V}$   
 Logic "1"  $\geq 11\text{ V}$



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Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 3.5\text{ V}$   
 Logic "1"  $\geq 11\text{ V}$

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four SPST Switches per Package

TRUTH TABLE		
Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V  
Logic "1" ≥ 11 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
<b>DG304B</b>		
-40 to 85°C	14-Pin Plastic DIP	DG304BDJ
<b>DG306B</b>		
-40 to 85°C	14-Pin Plastic DIP	DG306BDJ
<b>DG307B</b>		
-40 to 85°C	14-Pin Plastic DIP	DG307BDJ

### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2V or  
30 mA, whichever occurs first

Current, Any Terminal ..... 30 mA

Continuous Current, S or D  
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature ..... -65 to 150°C

Power Dissipation<sup>b</sup>  
14-Pin Plastic DIP<sup>c</sup> ..... 470 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 11 mW/°C above 75°C



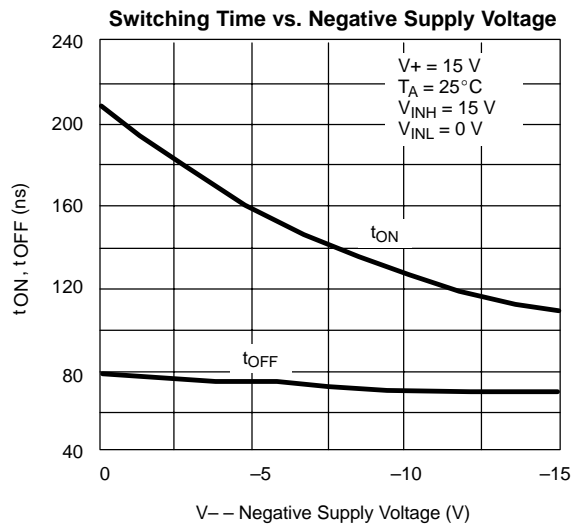
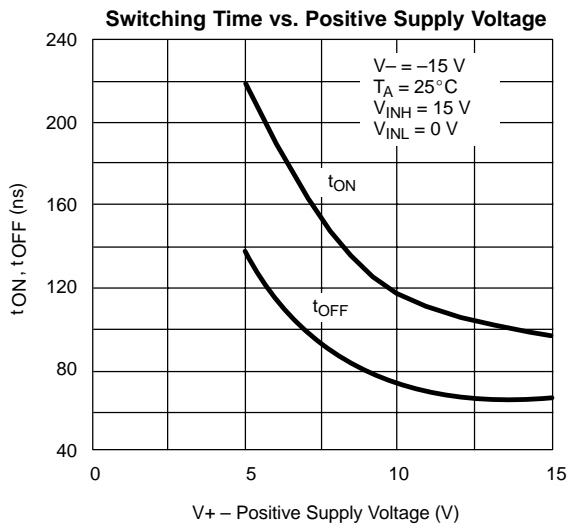
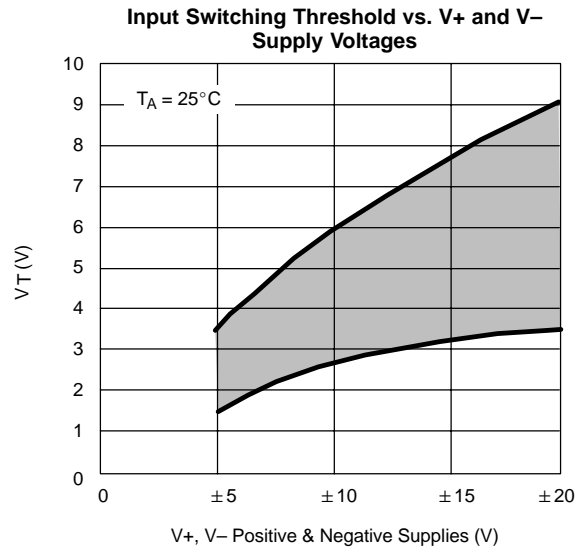
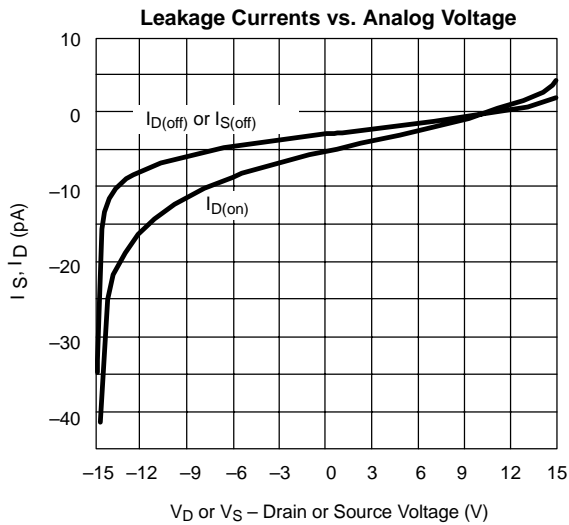
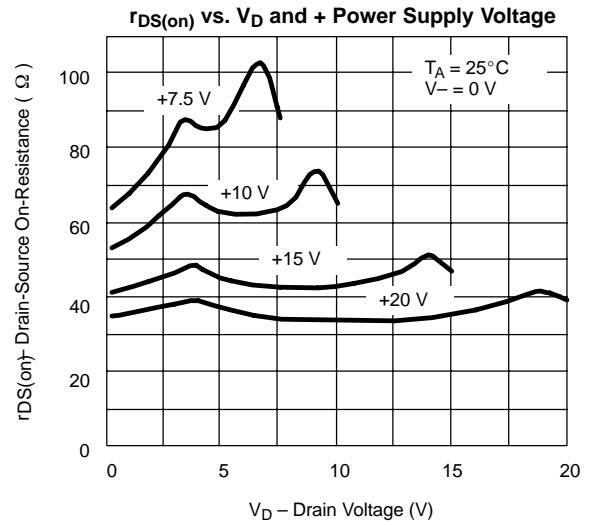
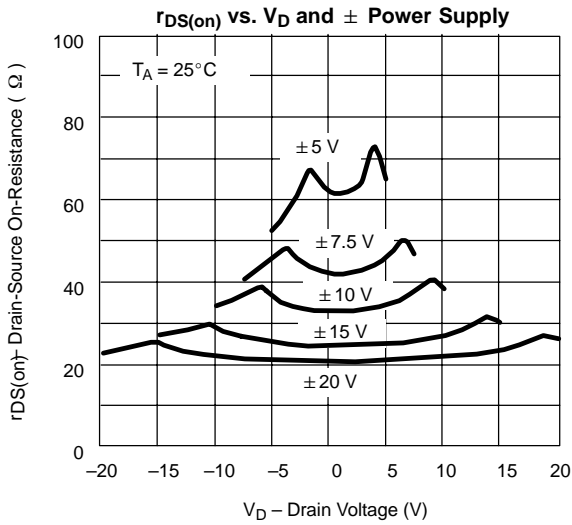
SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 3.5\text{ V}$ or $11\text{ V}^f$	Temp <sup>b</sup>	Limits -40 to 85°C			Unit
				Min <sup>d</sup>	Typ <sup>c</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = 10\text{ mA}$	Room Full		30	50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}$ $V_D = \mp 14\text{ V}$	Room Full	-5 -100	$\pm 0.1$	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 14\text{ V}$ $V_D = \mp 14\text{ V}$	Room Full	-5 -100	$\pm 0.1$	5 100	
Drain On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 14\text{ V}$	Room Full	-5 -200	$\pm 0.1$	5 200	
<b>Digital Control</b>							
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Full	-1	-0.001		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Room Full		0.001	1	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room Full	-1	-0.001		
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	See Figure 2	Room		110		ns
Turn-Off Time	$t_{OFF}$		Room		70		
Break-Before-Make Time	$t_{OPEN}$	DG305A/307A ONLY, See Figure 3	Room		50		
Charge Injection	Q	$C_L = 1\text{ nF}$ , $R_{gen} = 0$ , $V_{gen} = 0\text{ V}$ , See Figure 4	Room		30		pC
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$ $V_S, V_D = 0\text{ V}$	Room		14		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		14		
Channel-On Capacitance	$C_{D(on)}$		Room		40		
Input Capacitance	$C_{IN}$		$V_{IN} = 0\text{ V}$	Room		6	
		$V_{IN} = 15\text{ V}$	Room		7		
Off-Isolation	OIRR	$V_{IN} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$	Room		62		dB
Crosstalk (Channel-to-Channel)	$X_{TALK}$	$V_S = 1\text{ V}_{rms}$ , $f = 500\text{ kHz}$	Room		74		
<b>Power Supplies</b>							
Positive Supply Current	I+	$V_{IN} = 15\text{ V}$ or $0\text{ V}$ (All Inputs)	Room Full		0.001	100	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-100	-0.001		

Notes:

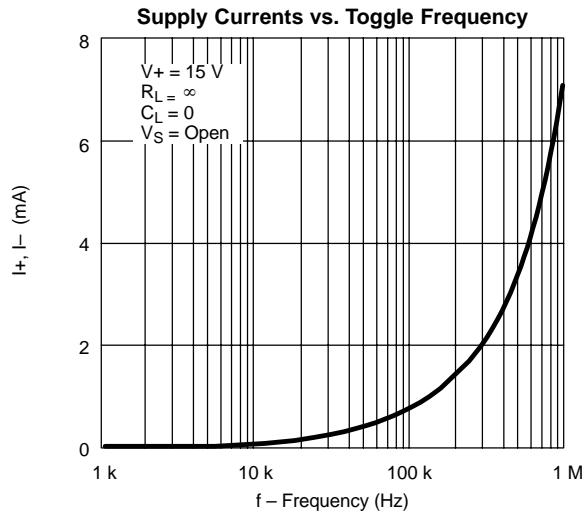
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



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**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

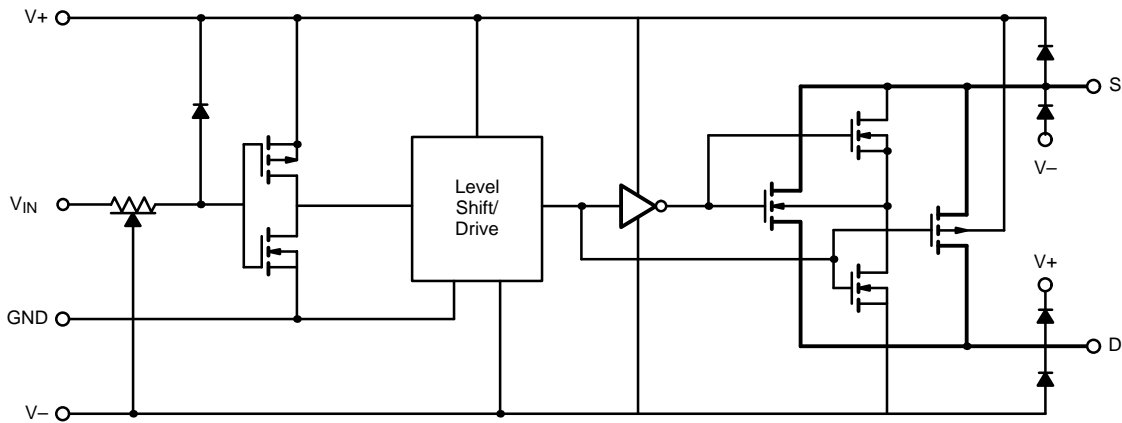


FIGURE 1.

**TEST CIRCUITS**

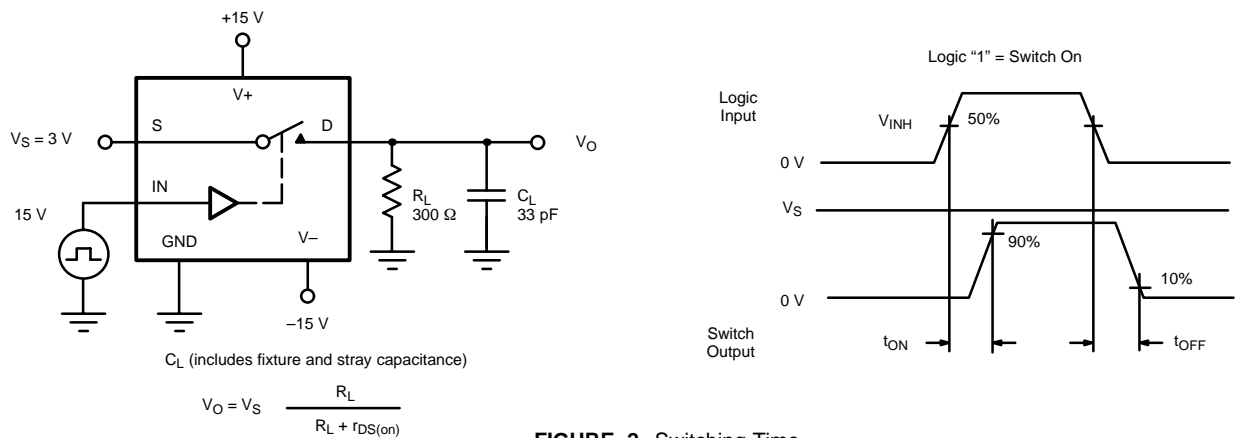
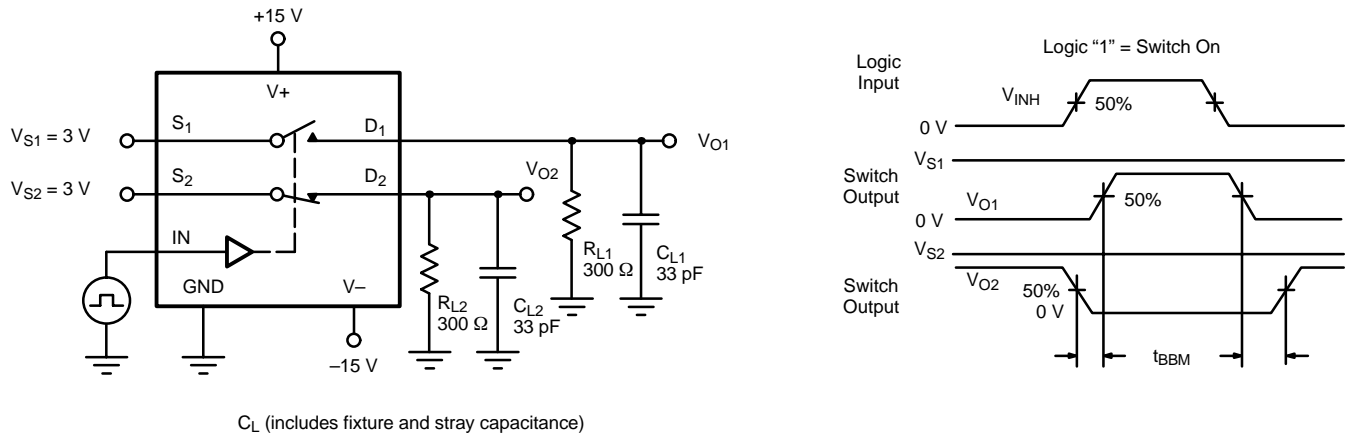
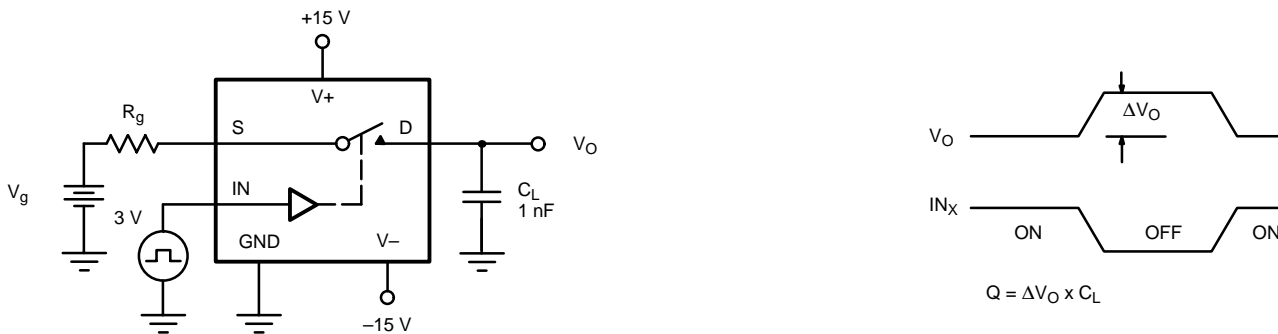


FIGURE 2. Switching Time

**TEST CIRCUITS**



**FIGURE 3.** Break-Before-Make SPDT (DG307B)

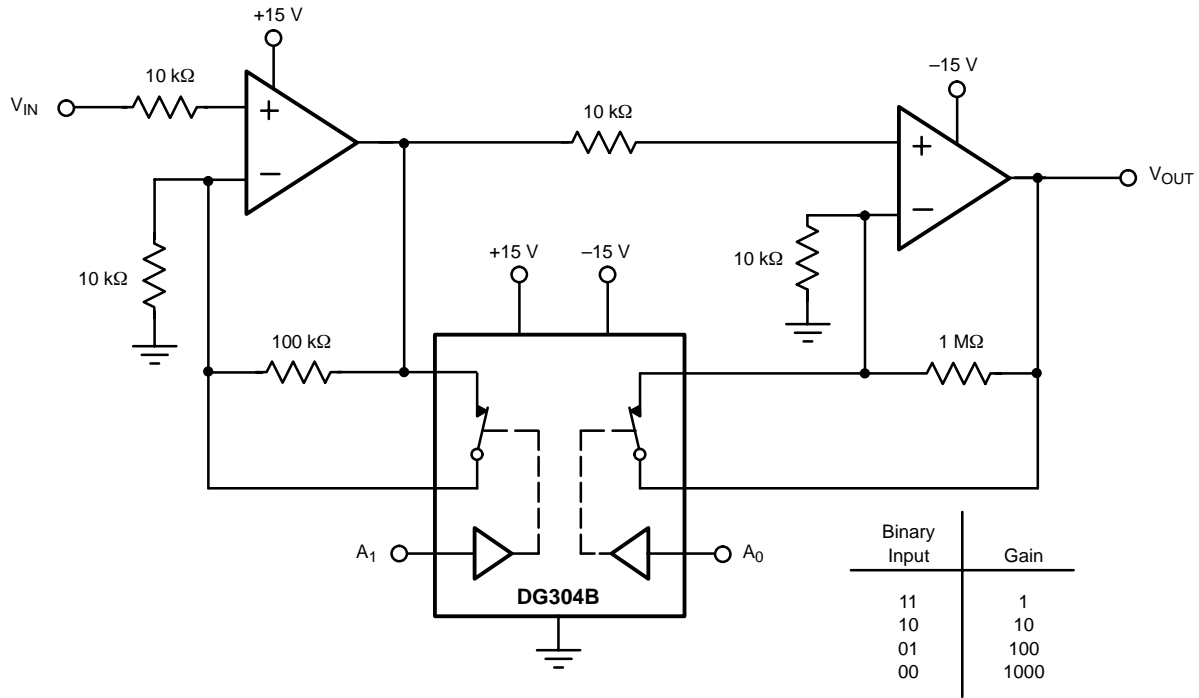
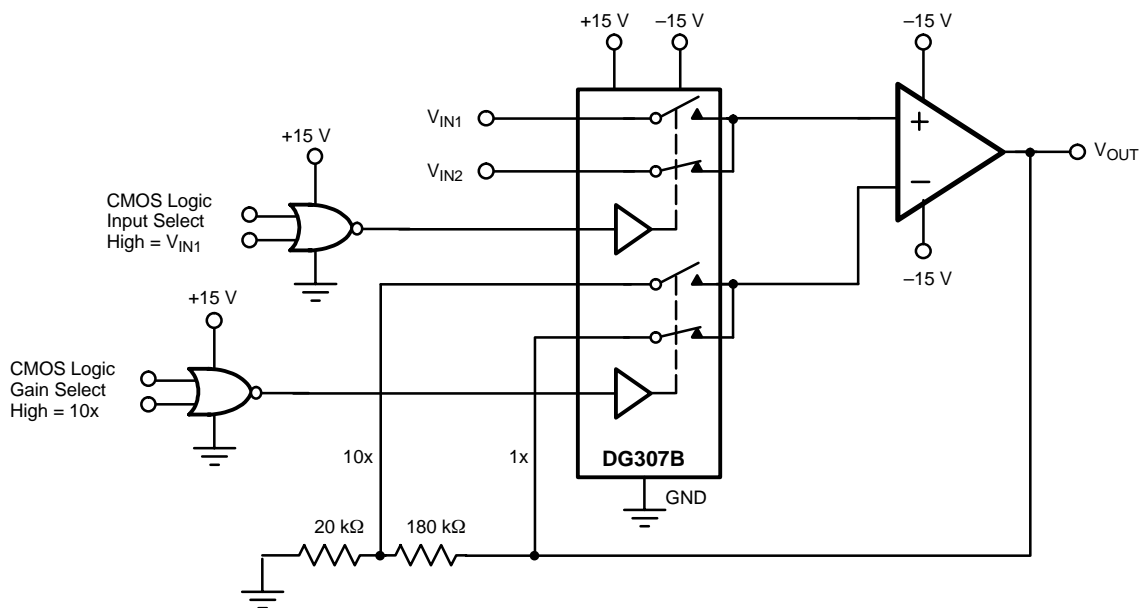


**FIGURE 4.** Charge Injection

<b>APPLICATION HINTS<sup>a</sup></b>				
<b>V+</b> Positive Supply Voltage (V)	<b>V-</b> Negative Supply Voltage (V)	<b>GND</b> Voltage (V)	<b>V<sub>IN</sub></b> Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	<b>V<sub>S</sub> or V<sub>D</sub></b> Analog Voltage Range (V)
15	-15	0	11/3.5	-15 to 15
20	-20	0	11/3.5	-20 to 20
15	0	0	11/3.5	0 to 15

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**APPLICATIONS**

**FIGURE 5. Low Power Binary to 10<sup>n</sup> Gain Low Frequency Amplifier**

**FIGURE 6. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain**

This datasheet has been download from:

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Datasheets for electronics components.