



Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

General Description

The DG411F/DG412F/DG413F are quad, single-pole/single-throw (SPST), fault-protected analog switches. They are pin compatible with the industry-standard nonprotected DG411/DG412/DG413. These new switches feature fault-protected inputs and Rail-to-Rail® signal-handling capability. All terminals are protected from overvoltage faults up to $\pm 36V$ with power on and up to $\pm 40V$ with power off. During a fault condition, the COM, NO, or NC terminal becomes an open circuit and only microamperes of leakage current flow from the source. On-resistance is 35Ω (max) and is matched between switches to 1.5Ω (max) at $+25^\circ C$.

The DG411F has four normally closed (NC) switches. The DG412F has four normally open (NO) switches. The DG413F has two NC and two NO switches. These CMOS switches operate with dual power supplies ranging from $\pm 4.5V$ to $\pm 20V$ or a single supply between $+9V$ and $+36V$. All digital inputs have $+0.8V$ and $+2.4V$ logic thresholds, ensuring both TTL and CMOS logic compatibility when using $\pm 15V$ or a single $+12V$ supply.

For supply voltages of $\pm 5V$, $+5V$, and $+3V$, refer to the MAX4711/MAX4712/MAX4713 data sheet.

Applications

Communication Systems
Signal Routing
Test Equipment
Data Acquisition
Industrial and Process Control Systems
Avionics
Redundant/Backup Systems

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Functional Diagram appears at end of data sheet.

Pin Configurations continued at end of data sheet.

Features

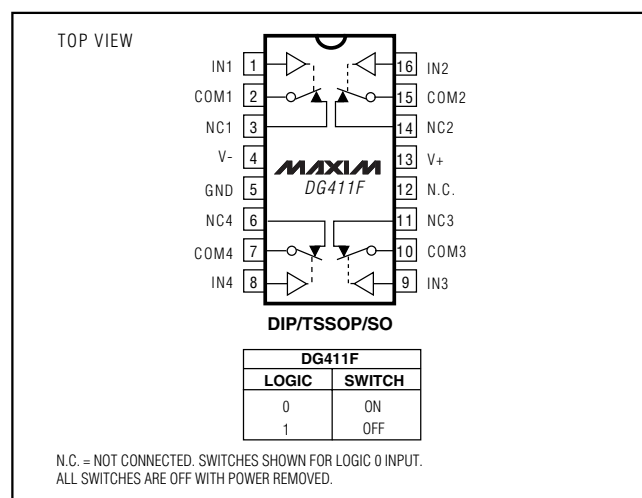
- ◆ No Power-Supply Sequencing Required
- ◆ Rail-to-Rail Signal Handling
- ◆ All Switches Off with Power Off
- ◆ All Switches Off when $V+$ is Off and $V-$ is On
- ◆ $\pm 40V$ Fault Protection with Power Off
- ◆ $\pm 36V$ Fault Protection with $\pm 15V$ Supplies
- ◆ Control Line Fault Protection from $V- - 0.3V$ to $V- + 40V$
- ◆ Pin Compatible with Industry-Standard DG411/DG412/DG413
- ◆ 20ns (typ) Fault Response Time
- ◆ 35Ω (max) R_{ON} with $\pm 15V$ Supplies
- ◆ $\pm 4.5V$ to $\pm 20V$ Dual Supplies
- ◆ $+9V$ to $+36V$ Single Supply
- ◆ TTL- and CMOS-Compatible Logic Inputs with $\pm 15V$ or Single $+9V$ to $+15V$ Supplies

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|--------------------------------|----------------|
| DG411FEUE | $-40^\circ C$ to $+85^\circ C$ | 16 TSSOP |
| DG411FDY | $-40^\circ C$ to $+85^\circ C$ | 16 SO |
| DG411FDJ | $-40^\circ C$ to $+85^\circ C$ | 16 Plastic DIP |

Ordering Information continued at end of data sheet.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

| | |
|---|---------------------------|
| V+ | -0.3V to +44V |
| V- | -44V to +0.3V |
| V+ to V-..... | -0.3V to +44V |
| IN_ | (V- - 0.3V) to (V- + 40V) |
| NO_, NC_ to COM_ (Note 1) | -40V to +40V |
| COM_, NO_, NC_ Voltage with Power On (Note 1)..... | -36V to +36V |
| COM_, NO_, NC_ Voltage with Power Off (Note 1)..... | -40V to +40V |
| Continuous Current (any terminal) | ±30mA |
| Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle) | ±100mA |

Continuous Power Dissipation (T_A = +70°C)

| | |
|--|-----------------|
| 16-Pin TSSOP (derate 9.4mW/°C above +70°C) | 755mW |
| 16-Pin SO (derate 8.7mW/°C above +70°C)..... | 696mW |
| 16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) | 842mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +160°C |
| Lead Temperature (soldering, 10s) | +300°C |

Note 1: COM_, NO_, and NC_ pins are fault protected. Signals on COM_, NO_, and NC_ exceeding -36V to +36V may damage the device during power-on conditions. When the power is off, the maximum range is -40V to +40V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±15V Dual Supplies

(V₊ = +15V, V₋ = -15V, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | T _A | MIN | TYP | MAX | UNITS |
|---|---|--|----------------|-------|--------|-------|-------|
| ANALOG SWITCH | | | | | | | |
| Fault-Free Analog Signal Range | V _{COM_} , V _{NO_} , V _{NC_} | | E | V- | | V+ | V |
| On-Resistance | R _{ON} | I _{COM_} = 10mA, V _{NO_} , V _{NC_} = ±10V | +25°C | | 25 | 35 | Ω |
| | | | E | | | 45 | |
| On-Resistance Match Between Channels (Note 4) | ΔR _{ON} | I _{COM_} = 10mA, V _{NO_} , V _{NC_} = ±10V | +25°C | | 0.2 | 1.5 | Ω |
| | | | E | | | 2.0 | |
| On-Resistance Flatness | R _{FLAT(ON)} | I _{COM_} = 10mA, V _{NO_} , V _{NC_} = ±5V, 0 | +25°C | | 1.0 | 3 | Ω |
| | | | E | | | 4 | |
| NO_, NC_ Off-Leakage Current (Note 5) | I _{NO_(OFF)} , I _{NC_(OFF)} | V _{COM_} = ±10V, V _{NO_} , V _{NC_} = > 10V | +25°C | -0.25 | +0.025 | +0.25 | nA |
| | | | E | -20 | | +20 | |
| COM_ Off-Leakage Current (Note 5) | I _{COM_(OFF)} | V _{COM_} = ±10V, V _{NO_} , V _{NC_} = > 10V | +25°C | -0.25 | +0.025 | +0.25 | nA |
| | | | E | -20 | | +20 | |
| COM_ On-Leakage Current (Note 5) | I _{COM_(ON)} | V _{COM_} = ±10V, V _{NO_} , V _{NC_} = ±10V or floating | +25°C | -0.5 | +0.025 | +0.5 | nA |
| | | | E | -40 | | +40 | |
| FAULT | | | | | | | |
| Fault-Protected Analog Signal Range | V _{COM_} , V _{NO_} , V _{NC_} | V ₊ = +15V, V ₋ = -15V | E | -36 | | +36 | V |
| | | V ₊ = 0, V ₋ = -15V | E | -36 | | +36 | |
| | | V ₊ = V ₋ = 0 | E | -40 | | +40 | |
| NO_ or NC_ Off-Leakage Current | I _{NO_} , I _{NC_} | V _{NO_} , V _{NC_} = ±36V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |
| COM_ Off-Leakage Current | I _{COM_} | V _{COM_} = ±36V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |

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DG411F/DG412F/DG413F

ELECTRICAL CHARACTERISTICS—±15V Dual Supplies (continued)

(V+ = +15V, V- = -15V, VIH = +2.4V, VIL = +0.8V, GND = 0, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | TA | MIN | TYP | MAX | UNITS |
|---|------------|---|-------|----------|------|----------|-------|
| NO_ or NC_ Leakage Current | INO_, INC_ | VNO_, VNC_ = ±40V, V+ = V- = 0 | +25°C | -1 | | +1 | µA |
| | | | E | -10 | | +10 | |
| COM_ Leakage Current | ICOM_ | VCOM_ = ±40V, V+ = V- = 0 | +25°C | -1 | | +1 | µA |
| | | | E | -10 | | +10 | |
| NO_ or NC_ Off-Leakage Current | INO_, INC_ | V+ = 0, V- = -15V, VNO_, VNC_ = ±36V | +25°C | -1 | | +1 | µA |
| | | | E | -10 | | +10 | |
| COM_ Off-Leakage Current | ICOM_ | V+ = 0, V- = -15V, VCOM_ = ±36V | +25°C | -1 | | +1 | µA |
| | | | E | -10 | | +10 | |
| Fault-Trip Threshold | | | E | V- - 0.4 | | V+ + 0.4 | V |
| ± Fault Output Turn-Off Delay | | VNO_, VNC_ = ±36V, RL = 1kΩ | E | | 20 | | ns |
| ± Fault Recovery Time | | VNO_, VNC_ = ±36V, RL = 1kΩ | E | | 1 | | µs |
| SWITCH DYNAMICS | | | | | | | |
| Turn-On Time | tON | VNO_ or VNC_ = ±10V, RL = 300Ω, CL = 35pF, Figure 2 | +25°C | | 70 | 175 | ns |
| | | | E | | | 220 | |
| Turn-Off Time | tOFF | VNO_ or VNC_ = ±10V, RL = 300Ω, CL = 35pF, Figure 2 | +25°C | | 55 | 145 | ns |
| | | | E | | | 160 | |
| Break-Before-Make Time Delay (DG413F only) (Note 6) | tBBM | VNO_ or VNC_ = ±10V, RL = 100Ω, CL = 10pF, Figure 3 | +25°C | 2 | 15 | | ns |
| | | | E | 1 | | | |
| Charge Injection | Q | VGEN = 0, RGEN = 0, CL = 1nF, Figure 4 | +25°C | | 5 | | pC |
| NO_ or NC_ Off-Capacitance | CN_(OFF) | f = 1MHz, Figure 5 | +25°C | | 15 | | pF |
| COM_ Off-Capacitance | CCOM_(OFF) | f = 1MHz, Figure 5 | +25°C | | 15 | | pF |
| COM_ On-Capacitance | CCOM_(ON) | f = 1MHz, Figure 5 | +25°C | | 47 | | pF |
| Off-Isolation (Note 7) | VISO | f = 1MHz, RL = 50Ω, CL = 15pF, PIN = 0dBm, Figure 6 | +25°C | | -65 | | dB |
| Channel-to-Channel Crosstalk (Note 8) | VCT | f = 1MHz, RL = 50Ω, CL = 15pF, PIN = 0dBm, Figure 6 | +25°C | | -105 | | dB |
| LOGIC INPUT | | | | | | | |
| Input Logic High | VIH | | E | 2.4 | | | V |
| Input Logic Low | VIL | | E | | | 0.8 | V |
| Input Leakage Current | IIN | VIN_ = 0 or V+ | E | -1 | | +1 | µA |
| POWER SUPPLY | | | | | | | |
| Power-Supply Range | V+, V- | | E | ±4.5 | | ±20 | V |
| V+ Supply Current | I+ | All VIN_ = +5V, VCOM_ = 0 | +25°C | | 355 | 600 | µA |
| | | | E | | | 800 | |
| | | All VIN_ = 0 or V+, VCOM_ = 0 | +25°C | | 155 | 300 | |
| | | | E | | | 400 | |

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ELECTRICAL CHARACTERISTICS—±15V Dual Supplies (continued)

(V+ = +15V, V- = -15V, VIH = +2.4V, VIL = +0.8V, GND = 0, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | TA | MIN | TYP | MAX | UNITS |
|--------------------|--------|-------------------------------|-------|-----|-----|-----|-------|
| V- Supply Current | I- | All VIN_ = +5V, VCOM_ = 0 | +25°C | | 155 | 250 | μA |
| | | | E | | | 325 | |
| | | All VIN_ = 0 or V+, VCOM_ = 0 | +25°C | | 155 | 250 | |
| | | | E | | | 325 | |
| GND Supply Current | IGND | All VIN_ = +5V, VCOM_ = 0 | +25°C | | 200 | 350 | μA |
| | | | E | | | 475 | |
| | | All VIN_ = 0 or V+, VCOM_ = 0 | +25°C | | 0.1 | 1 | |
| | | | E | | | 10 | |

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +12V, V- = 0, VIH = +2.4V, VIL = +0.8V, GND = 0, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | TA | MIN | TYP | MAX | UNITS |
|---|----------------------|--|-------|-------|-----|-------|-------|
| ANALOG SWITCH | | | | | | | |
| Fault-Free Analog Signal Range | VCOM_, VNO_, VNC_ | | E | 0 | | V+ | V |
| On-Resistance | RON | ICOM_ = 1mA, VNO_, VNC_ = +10V | +25°C | | 56 | 85 | Ω |
| | | | E | | | 120 | |
| On-Resistance Match Between Channels (Note 4) | ΔRON | ICOM_ = 1mA, VNO_, VNC_ = +10V | +25°C | | 1.0 | 4 | Ω |
| | | | E | | | 5 | |
| NO_, NC_ Off-Leakage Current (Note 5) | INO_(OFF), INC_(OFF) | VCOM_ = +1V, +10V, VNO_, VNC_ = +10V, +1V | +25°C | -0.25 | | +0.25 | nA |
| | | | E | -20 | | +20 | |
| COM_ Off-Leakage Current (Note 5) | ICOM_(OFF) | VCOM_ = +1V, +10V, VNO_, VNC_ = +10V, +1V | +25°C | -0.5 | | +0.25 | nA |
| | | | E | -20 | | +20 | |
| COM_ On-Leakage Current (Note 5) | ICOM_(ON) | VCOM_ = +1V, +10V, VNO_, VNC_ = +1V, +10V, or floating | +25°C | -0.5 | | +0.5 | nA |
| | | | E | -40 | | +40 | |
| FAULT | | | | | | | |
| Fault-Protected Analog Signal Range | VCOM_, VNO_, VNC_ | Power on | E | -36 | | +36 | V |
| | | Power off | E | -40 | | +40 | |
| NO_ or NC_ Off-Leakage Current (Note 5) | INO_, INC_ | VNO_, VNC_ = ±36V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |
| COM_ Off-Leakage Current (Note 5) | ICOM_ | VNO_, VNC_ = ±36V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |
| NO_ or NC_ Leakage Current (Note 5) | INO_, INC_ | Supplies off, VNO_, VNC_ = ±40V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

DG411F/DG412F/DG413F

ELECTRICAL CHARACTERISTICS—Single +12V Supply (continued)

(V+ = +12V, V- = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | T _A | MIN | TYP | MAX | UNITS |
|---|-------------------|---|----------------|-----|-----|-----|-------|
| COM_ Leakage Current (Note 5) | I _{COM_} | Supplies off, V _{NO_} , V _{NC_} = ±40V | +25°C | -1 | | +1 | μA |
| | | | E | -10 | | +10 | |
| +Fault Output Turn-Off Delay | | V _{NO_} , V _{NC_} = +36V, R _L = 1kΩ | E | | 20 | | ns |
| +Fault Recovery Time | | V _{NO_} , V _{NC_} = +36V, R _L = 1kΩ | E | | 1 | | μs |
| SWITCH DYNAMICS | | | | | | | |
| Turn-On Time | t _{ON} | V _{NO_} or V _{NC_} = +10V, R _L = 300Ω, C _L = 35pF, Figure 2 | +25°C | | 120 | 250 | ns |
| | | | E | | | 315 | |
| Turn-Off Time | t _{OFF} | V _{NO_} or V _{NC_} = +10V, R _L = 300Ω, C _L = 35pF, Figure 2 | +25°C | | 70 | 125 | ns |
| | | | E | | | 140 | |
| Break-Before-Make Time Delay (DG413F Only) (Note 6) | t _{BBM} | V _{NO_} or V _{NC_} = +10V, R _L = 100Ω, C _L = 10pF, Figure 3 | +25°C | 2 | 50 | | ns |
| | | | E | 1 | | | |
| Charge Injection | Q | V _{GEN} = 0, R _{GEN} = 0, C _L = 1nF, Figure 4 | +25°C | | 5 | | pC |
| LOGIC INPUT | | | | | | | |
| Input Logic High | V _{IH} | | E | 2.4 | | | V |
| Input Logic Low | V _{IL} | | E | | | 0.8 | V |
| Input Leakage Current (Note 5) | I _{IN} | V _{IN_} = 0 or V+ | E | -1 | | +1 | μA |
| POWER SUPPLY | | | | | | | |
| Power-Supply Range | V+ | | E | +9 | | +36 | V |
| V+ Supply Current | I+ | All V _{IN_} = +5V, V _{COM_} = +6V | +25°C | | 180 | 350 | μA |
| | | | E | | | 450 | |
| | | All V _{IN_} = 0 or V+, V _{COM_} = +6V | +25°C | | 85 | 150 | |
| | | | E | | | 250 | |

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Electrical specifications at -40°C are not production tested and guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.

Note 5: Leakage parameters are 100% tested at maximum rated temperature and with dual supplies and guaranteed by design at +25°C.

Note 6: Guaranteed by design.

Note 7: Off-Isolation = $20 \log_{10} [V_{COM}/(V_{NC} \text{ or } V_{NO})]$, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

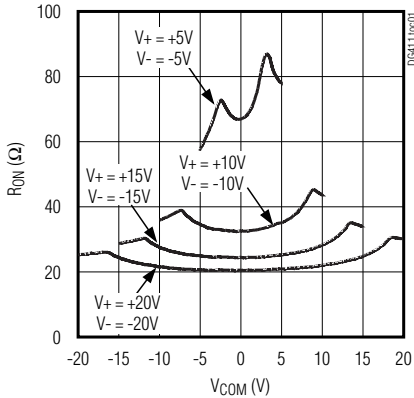
Note 8: Between any two switches.

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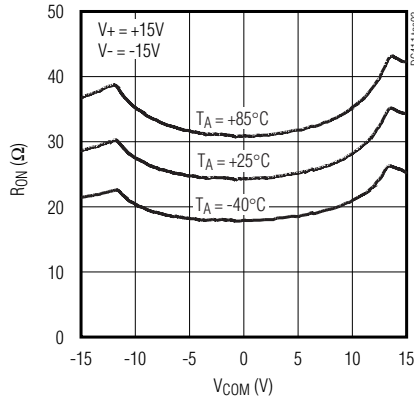
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

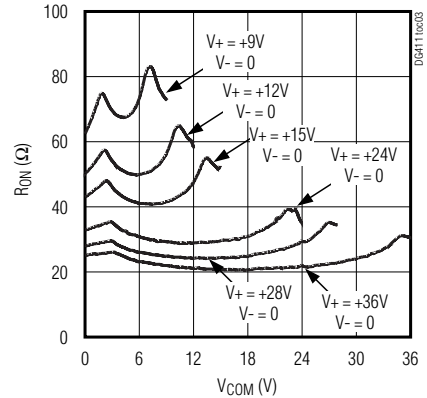
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



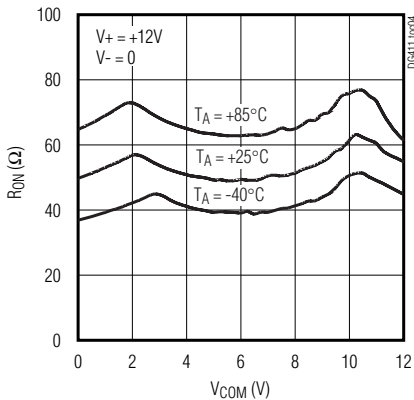
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



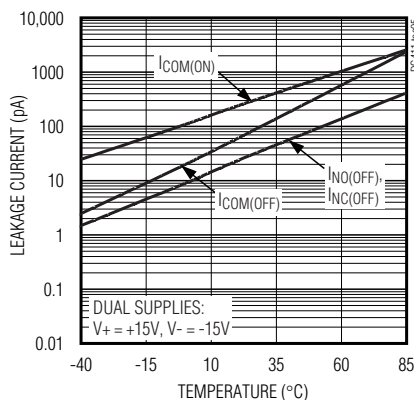
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



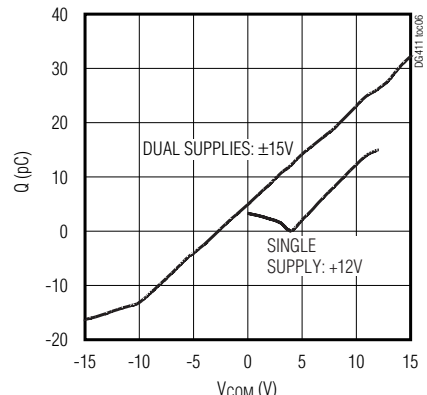
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



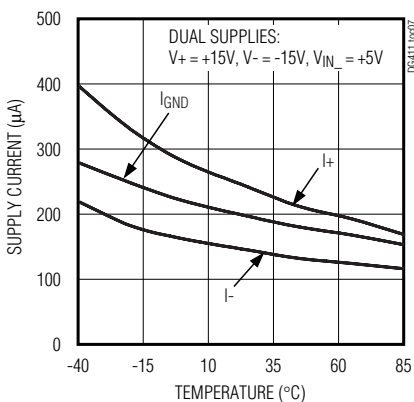
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



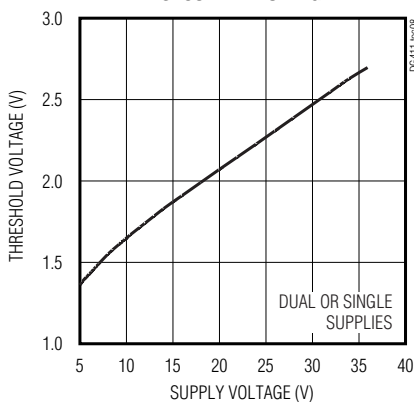
CHARGE INJECTION vs. V_{COM}



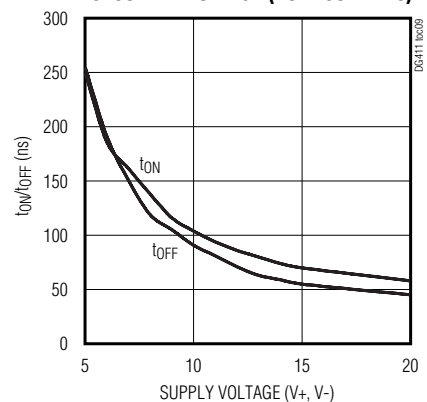
SUPPLY CURRENT vs. TEMPERATURE



LOGIC-LEVEL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



TURN-ON/TURN-OFF TIMES vs. SUPPLY VOLTAGE (DUAL SUPPLIES)

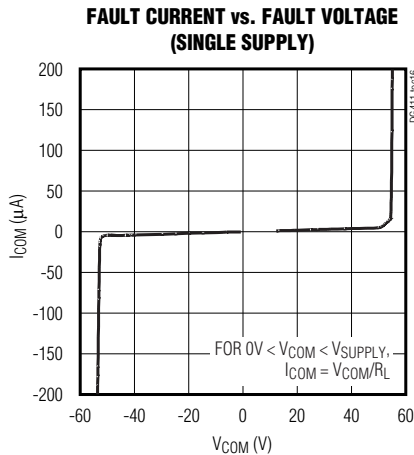
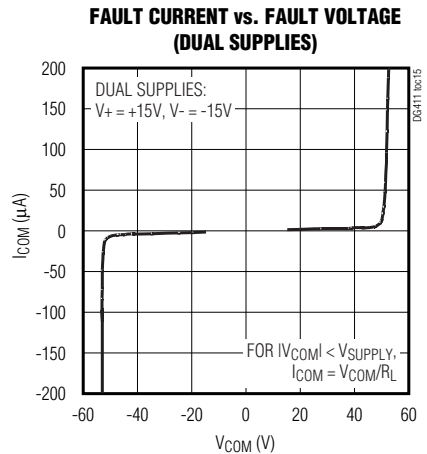
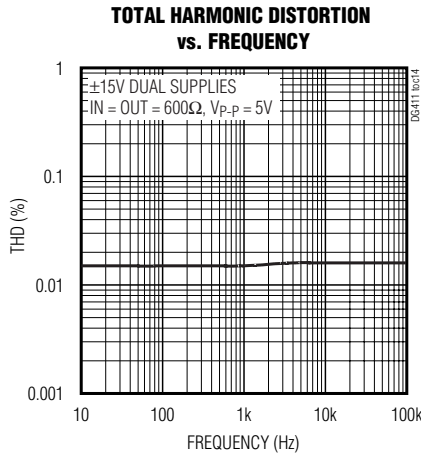
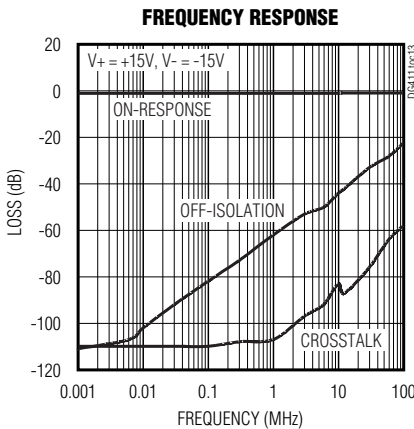
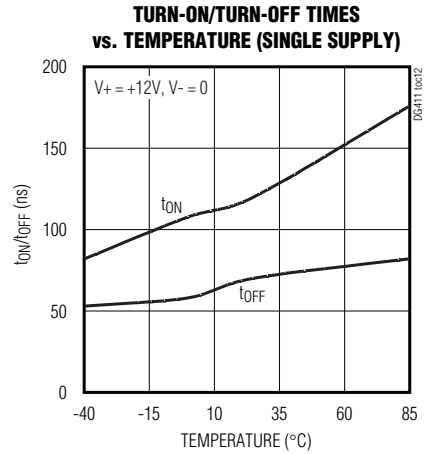
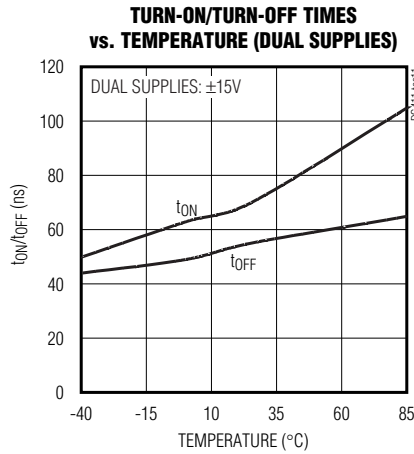
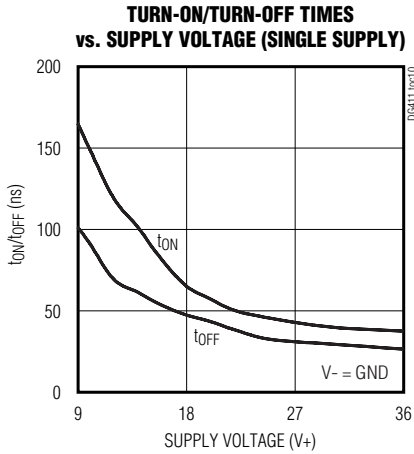


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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

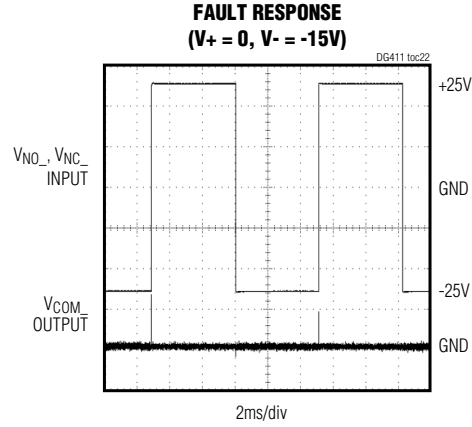
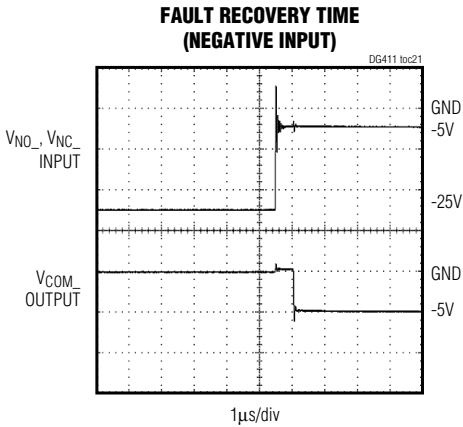
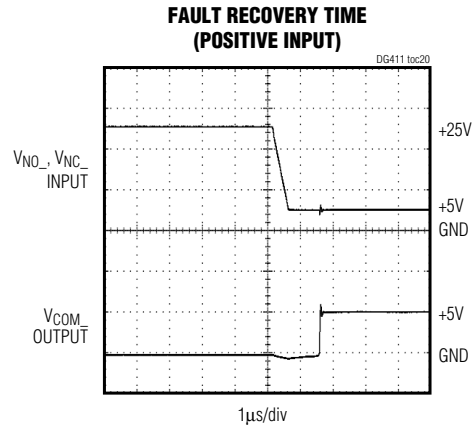
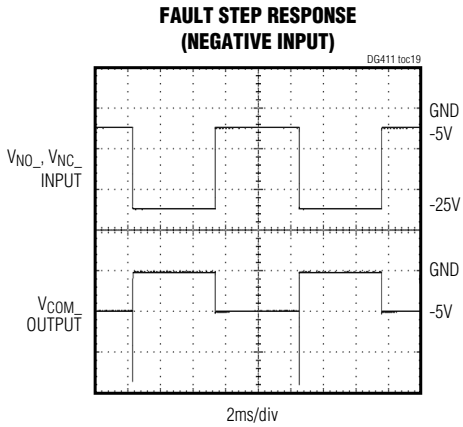
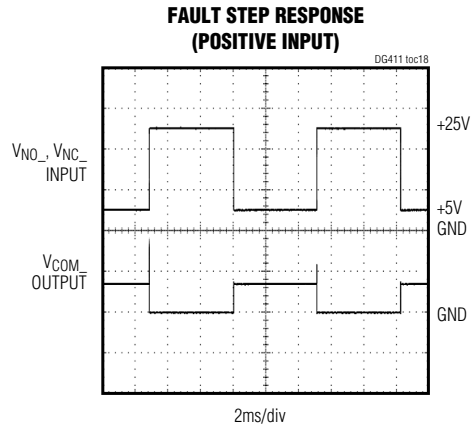
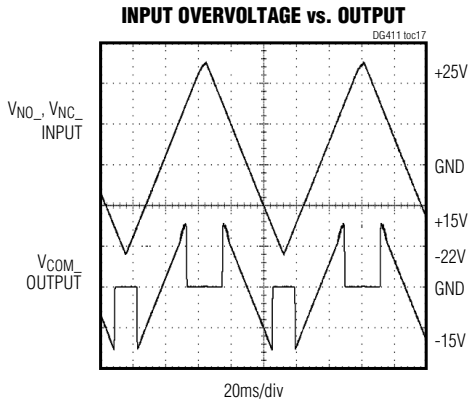
DG411F/DG412F/DG413F



Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Pin Description

DG411F/DG412F/DG413F

| PIN | | | NAME | FUNCTION |
|--------------|--------------|--------------|------------------------|--|
| DG411F | DG412F | DG413F | | |
| 1, 16, 9, 8 | 1, 16, 9, 8 | 1, 16, 9, 8 | IN1, IN2, IN3, IN4 | Logic Control Digital Inputs |
| 2, 15, 10, 7 | 2, 15, 10, 7 | 2, 15, 10, 7 | COM1, COM2, COM3, COM4 | Analog Switch Common Terminals |
| 3, 14, 11, 6 | — | — | NC1, NC2, NC3, NC4 | Analog Switch Normally Closed Terminals |
| — | 3, 14, 11, 6 | — | NO1, NO2, NO3, NO4 | Analog Switch Normally Open Terminals |
| — | — | 3, 6 | NO1, NO4 | Analog Switch Normally Open Terminals |
| — | — | 14, 11 | NC2, NC3 | Analog Switch Normally Closed Terminals |
| 4 | 4 | 4 | V- | Negative-Supply Voltage Input. Connect to GND for single-supply operation. Bypass with a 0.1μF capacitor to GND. |
| 5 | 5 | 5 | GND | Ground. Connect to digital ground. |
| 12 | 12 | 12 | N.C. | No Connection. Not internally connected. |
| 13 | 13 | 13 | V+ | Positive-Supply Voltage Input. Bypass with a 0.1μF capacitor to GND. |

Detailed Description

The DG411F/DG412F/DG413F are fault-protected CMOS analog switches with unique operation and construction. These switches differ considerably from traditional fault-protection switches, with several advantages. First, they are constructed with two parallel FETs, allowing very low on-resistance when the switch is on. Second, they allow signals on the NO_ or NC_ pins that are within, or slightly beyond, the supply rails to be passed through the switch to the COM_ terminal (or vice versa), allowing true rail-to-rail signal operation. Third, the DG411F/DG412F/DG413F have the same fault-protection performance on any of the NO_, NC_, or COM_ switch inputs. Operation is identical for both fault polarities. The fault protection extends to ±36V from GND with ±15V supplies.

During a fault condition, the particular overvoltage input (COM_, NO_, NC_) pin becomes high impedance regardless of the switch state or load resistance. When power is removed, the fault protection is still in effect. In this case, the COM_, NO_, or NC_ terminals are a virtual open circuit. The fault can be up to ±40V with power off. The switches turn off when V+ is not powered, regardless of V-.

Pin Compatibility

These switches have identical pinouts to common non-fault-protected CMOS switches. They allow for carefree

direct replacement in existing printed circuit boards since the NO_, NC_, and COM_ pins of each switch are fault protected.

Internal Construction

Internal construction is shown in Figure 1, with the analog signal paths shown in bold. A single NO switch is shown. The NC configuration is identical except the logic-level translator becomes an inverter. The analog switch is formed by the parallel combination of N-channel FET (N1) and P-channel FET (P1), which are driven on and off simultaneously according to the input fault condition and the logic-level state.

Normal Operation

Two comparators continuously compare the voltage on the COM_, NO_, and NC_ pins with V+ and V-. When the signal on COM_, NO_, or NC_ is between V+ and V-, the switch acts normally, with FETs N1 and P1 turning on and off in response to IN_ signals. The parallel combination of N1 and P1 forms a low-value resistor between NO_ (or NC_) and COM_ so that signals pass equally well in either direction.

Positive Fault Condition

When the signal on NO_ (or NC_) and COM_ exceeds V+ by about 50mV, the high-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) and COM_ pins high impedance regardless of

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

the switch state. If the switch state is off, all FETs are turned off and both NO₋ (or NC₋) and COM₋ are high impedance.

Negative Fault Condition

When the signal on NO₋ (or NC₋) and COM₋ exceeds V₋ by about 50mV, the low-fault comparator output is high, turning off FETs N1 and P1. This makes the NO₋ (or NC₋) and COM₋ pins high impedance regardless of the switch state. If the switch state is off, all FETs are turned off and both NO₋ (or NC₋) and COM₋ are high impedance.

Transient Fault Response and Recovery

When a fast rise-time and fall-time transient on NO₋, NC₋, or COM₋ exceeds V₊ or V₋, the output follows the input to the supply rail with only a few nanoseconds delay. This delay is due to the switch on-resistance and circuit capacitance to ground. When the input transient returns to within the supply rails, however, there is a longer output recovery time delay. For positive faults, the recovery time is typically 1μs. For negative faults, the recovery time is typically 0.5μs. These values depend on the output resistance and capacitance, and are not production tested or guaranteed. The delays are not dependent on the fault amplitude. Higher load resistance and capacitance increase recovery times.

Fault-Protection Voltage and Power Off

The maximum fault voltage on the NO₋ (or NC₋) and COM₋ pins is ±36V with power applied and ±40V with power off.

Failure Modes

Exceeding the fault-protection voltage limits on NO₋, NC₋, or COM₋, even for very short periods, can cause the device to fail. See the *Absolute Maximum Ratings*. The failure modes may not be obvious, and failure in one switch may or may not affect other switches in the same package.

Ground

There is no galvanic connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V₊ and V₋ by the logic-level translators. However, the potential of the analog signals must be defined or at least limited with respect to GND.

V₊ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V₊ and V₋ signals to drive the gates of the analog switches. This drive signal is the only connection between the power supplies and the analog signals.

IN₋ Logic-Level Thresholds

The logic-level thresholds are CMOS and TTL compatible when V₊ is +15V. As V₊ is raised, the threshold increases slightly, and when V₊ reaches 25V, the level threshold is about 2.3V, above the TTL output high-level minimum of 2.4V, but still compatible with CMOS outputs (see the *Typical Operating Characteristics*). V₋ has no effect on the logic-level thresholds.

Bipolar Supplies

The DG411F/DG412F/DG413F operate with bipolar supplies between ±4.5V and ±20V. The V₊ and V₋ supplies need not be symmetrical, but their difference cannot exceed the absolute maximum rating of 44V.

Single Supply

The DG411F/DG412F/DG413F operate from a single supply between +9V and +36V when V₋ is connected to GND.

Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|----------------|
| DG412FEUE | -40°C to +85°C | 16 TSSOP |
| DG412FDY | -40°C to +85°C | 16 SO |
| DG412FDJ | -40°C to +85°C | 16 Plastic DIP |
| DG413FEUE | -40°C to +85°C | 16 TSSOP |
| DG413FDY | -40°C to +85°C | 16 SO |
| DG413FDJ | -40°C to +85°C | 16 Plastic DIP |

Chip Information

TRANSISTOR COUNT: 251

PROCESS: CMOS

SUBSTRATE CONNECTED TO: V₊

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Test Circuits/Timing Diagrams

DG411F/DG412F/DG413F

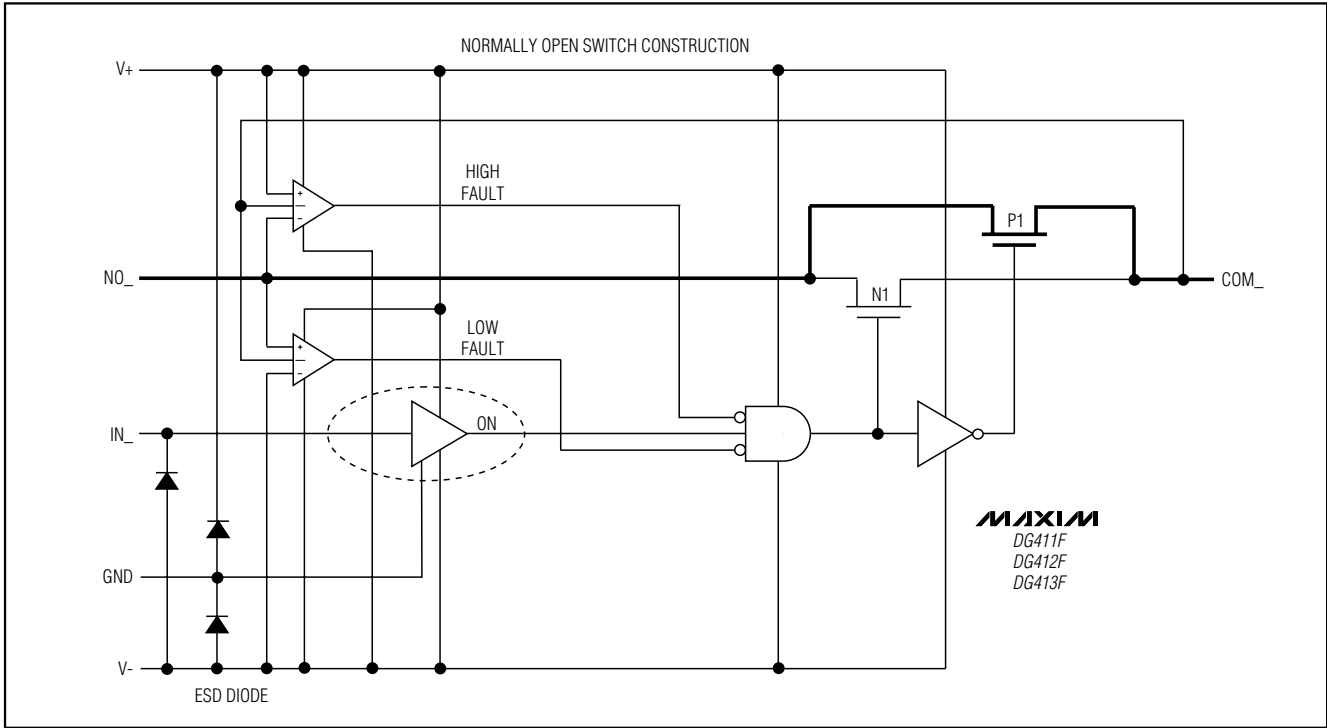


Figure 1. Functional Diagram

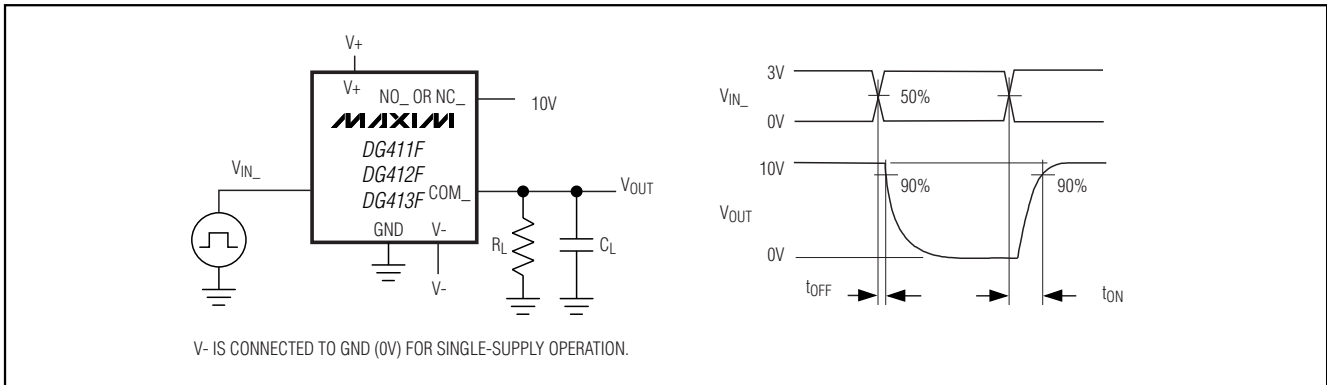


Figure 2. Switch Turn-On/Turn-Off Times

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

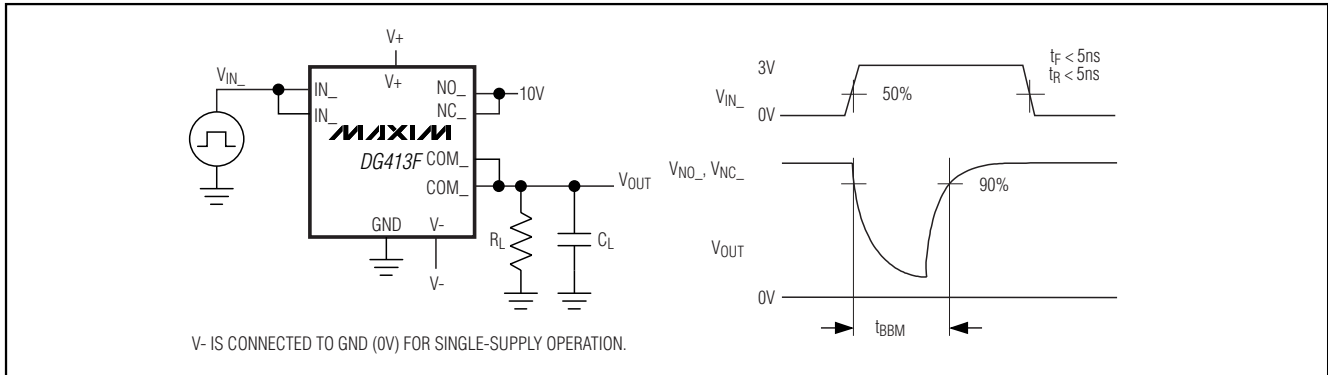


Figure 3. DG413F Break-Before-Make Interval

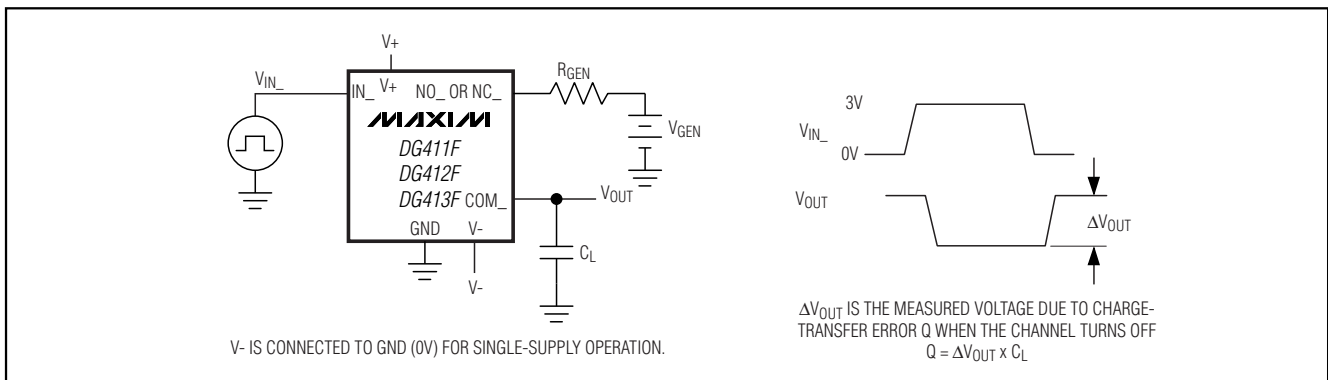


Figure 4. Charge Injection

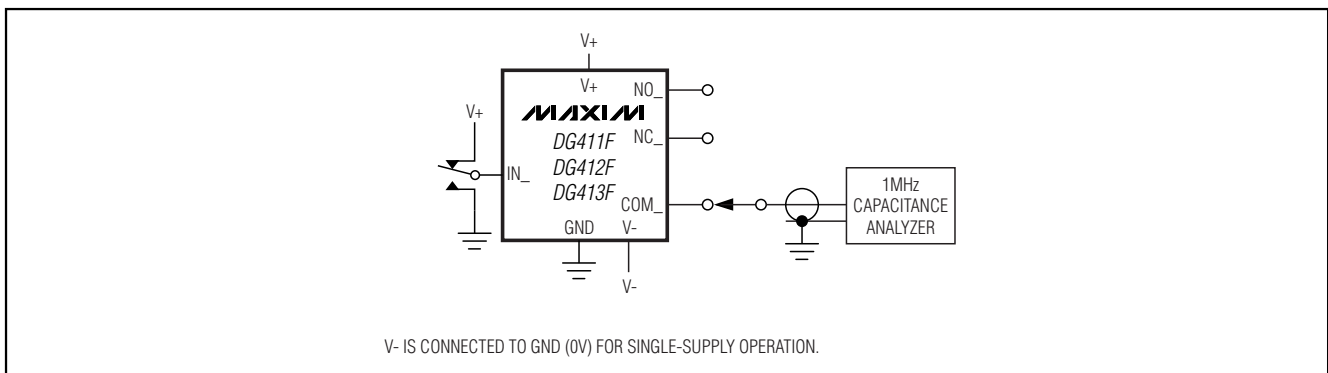


Figure 5. COM_, NO_, NC_ Capacitance

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

DG411F/DG412F/DG413F

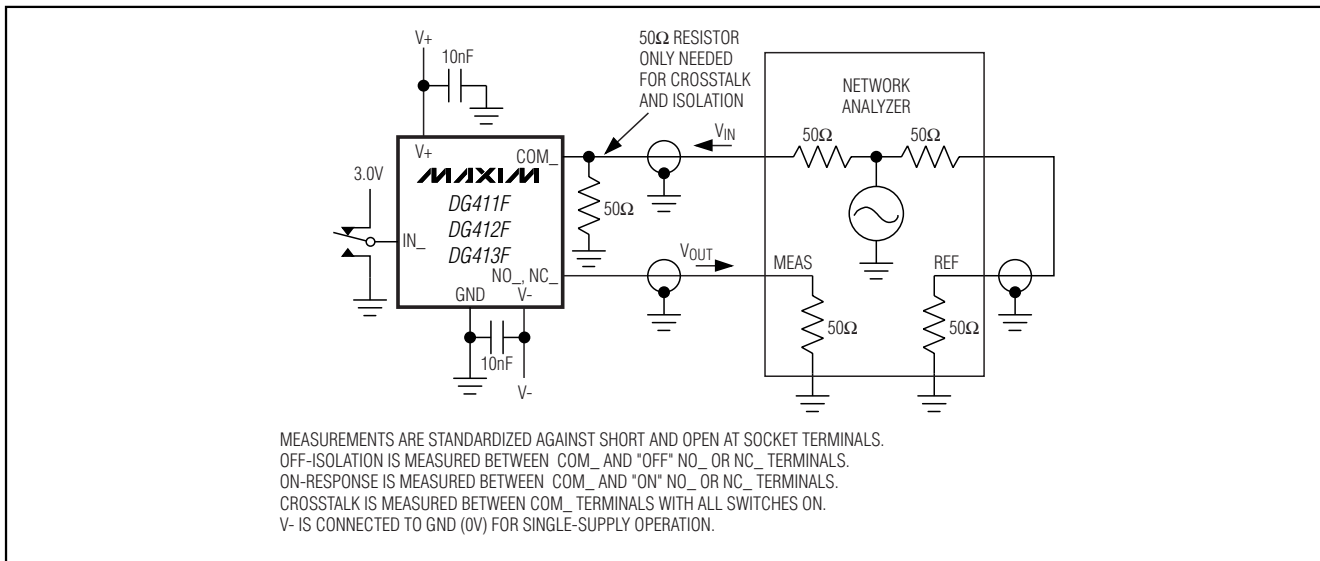
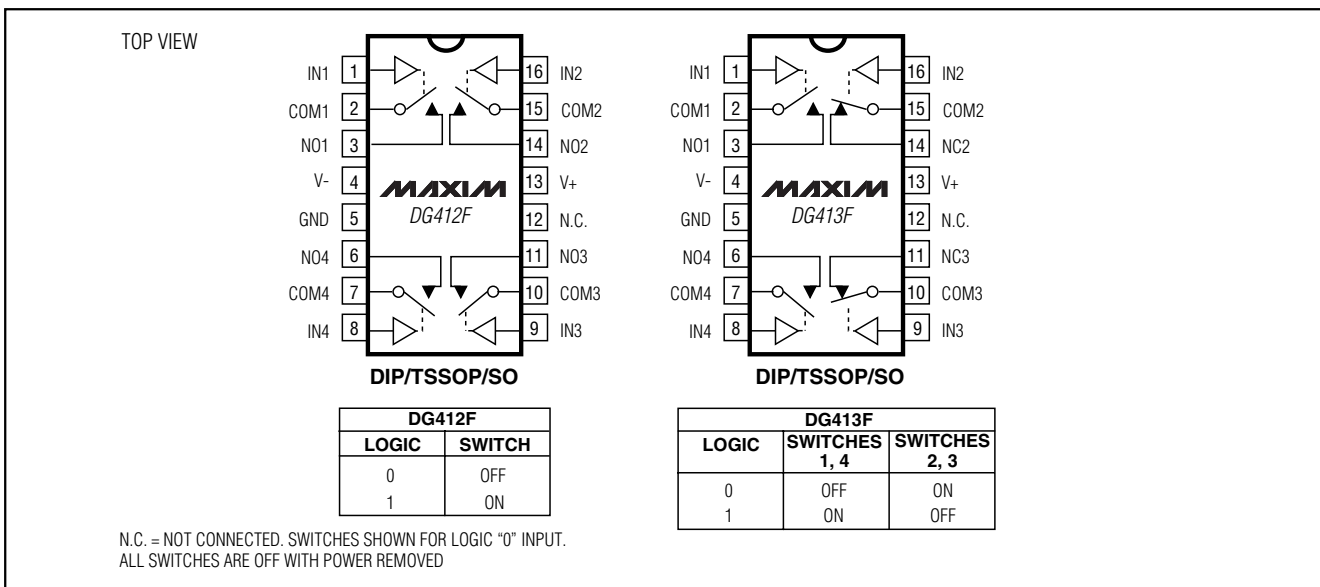


Figure 6. Frequency Response, Off-Isolation, and Crosstalk

Pin Configurations (continued)



Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.180 | --- | 4.572 |
| A1 | 0.020 | --- | 0.508 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.015 | 0.021 | 0.381 | 0.533 |
| B1 | 0.045 | 0.060 | 1.14 | 1.524 |
| C | 0.009 | 0.014 | 0.229 | 0.355 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.255 |
| E1 | 0.275 | 0.295 | 6.985 | 7.493 |
| e | 0.100 | --- | 2.54 | --- |
| eA | 0.300 | --- | 7.62 | --- |
| eB | --- | 0.400 | --- | 10.16 |
| L | 0.115 | 0.150 | 2.921 | 3.81 |

| | INCHES | | MILLIMETERS | | N | MS001 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILAR TO JEDEC MS-095-AH
 6. N = NUMBER OF PINS

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 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300" 1/1 21-0043 B
 TITLE DOCUMENT CONTROL NUMBER REV

PDIPN.EPS

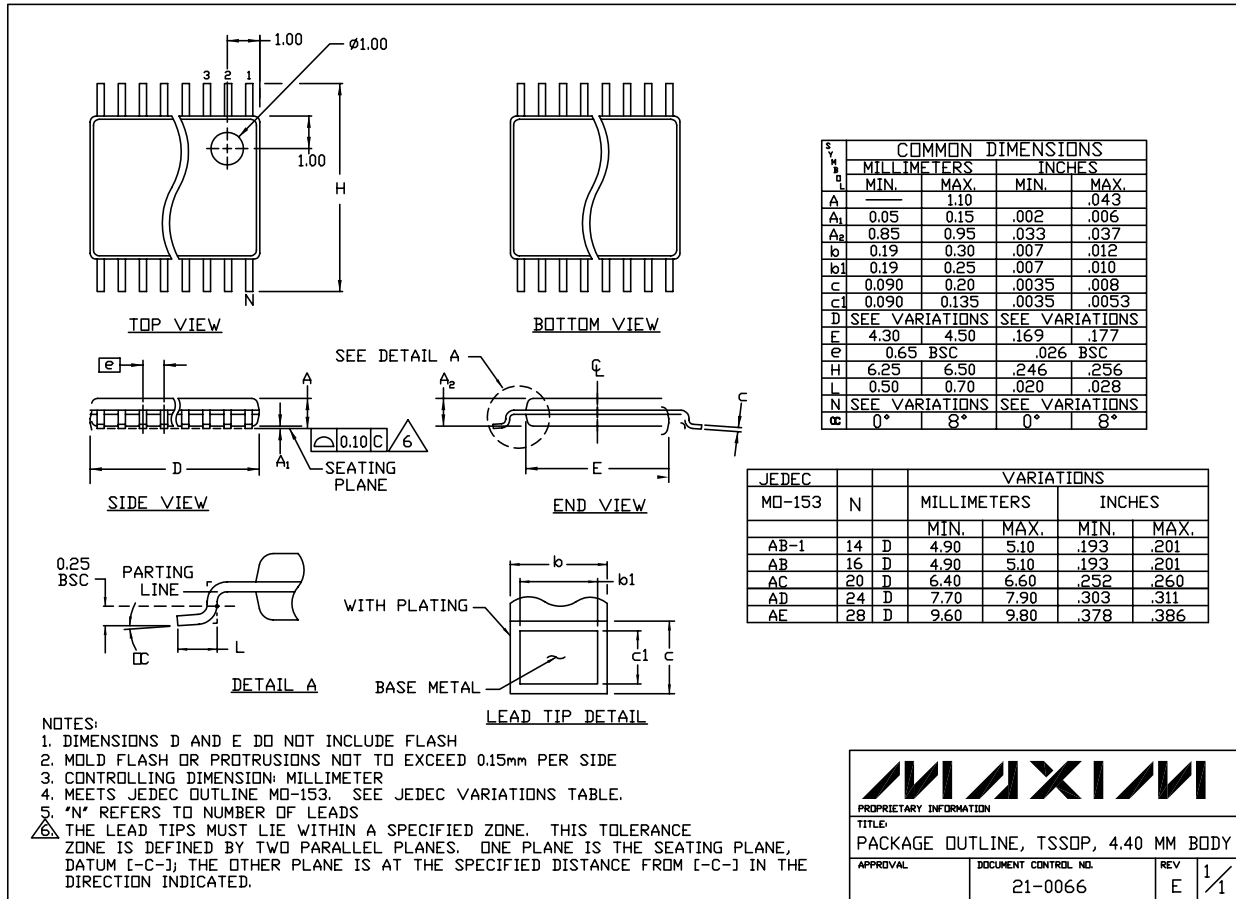
Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Package Information (continued)

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DG411F/DG412F/DG413F

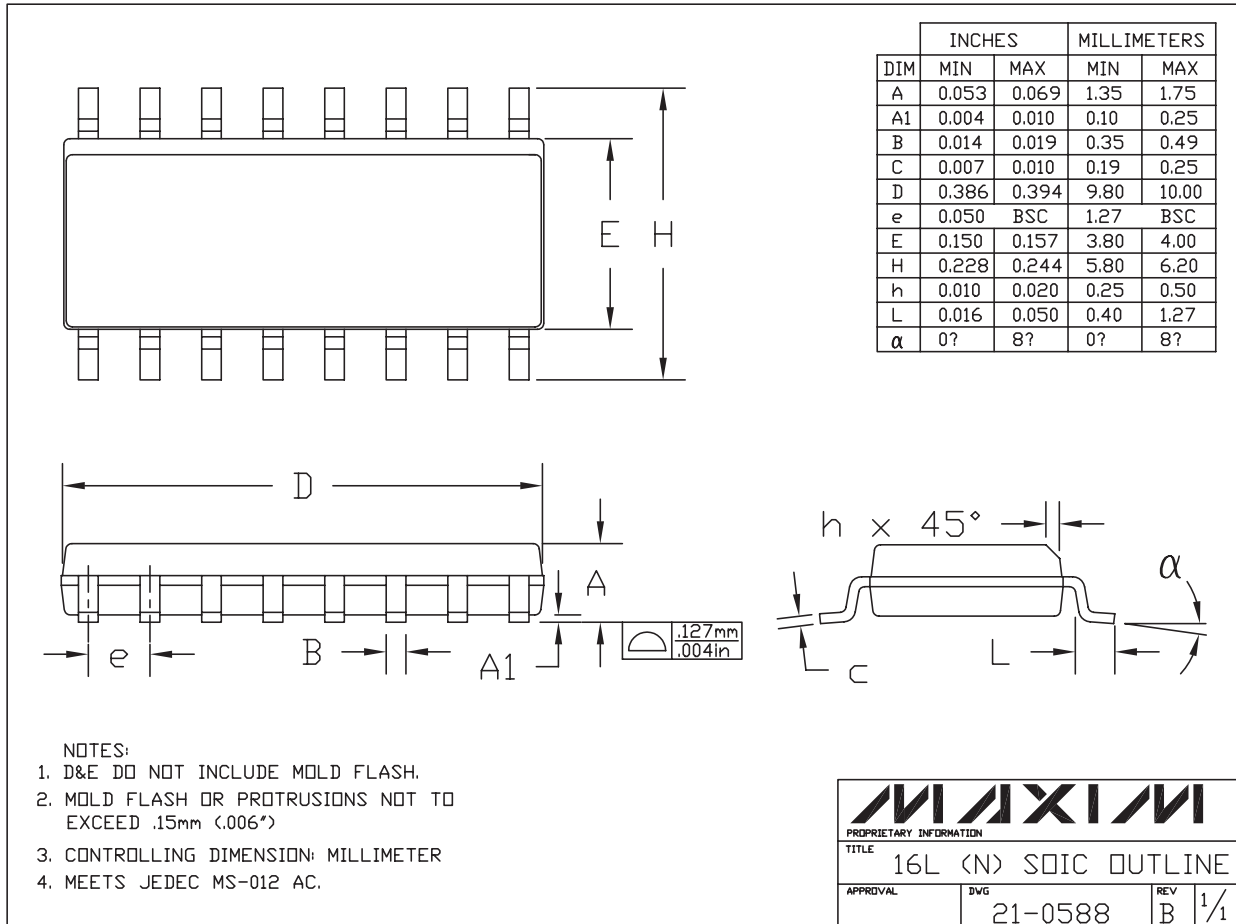
TSSOP, NO PADS, EPS



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Package Information (continued)

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