

5-Bit Shift Registers

General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

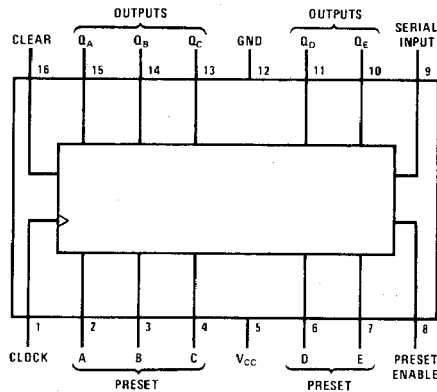
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

Connection Diagram



5496(J), (W); 7496(J), (N), (W);
54LS96/74LS96(J), (N), (W)

Truth Table

CLEAR	PRESET ENABLE	INPUTS					CLOCK	SERIAL	OUTPUTS				
		PRESET							QA	QB	QC	QD	QE
		A	B	C	D	E							
L	L	X	X	X	X	X	X	L	L	L	L	L	L
L	X	L	L	L	L	L	X	L	L	L	L	L	L
H	H	H	H	H	H	H	X	H	H	H	H	H	H
H	H	L	L	L	L	L	L	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	H	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	L	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	X	↑	H	H	QA _n	QB _n	QC _n	QD _n
H	L	X	X	X	X	X	↑	L	L	QA _n	QB _n	QC _n	QD _n

H = high level (steady state), L = low level (steady state)

X = don't care (any input, including transitions)

↑ = transition from low to high level

QA0, QB0, etc. = the level of QA, QB, etc., respectively before the indicated steady state input conditions were established.

QA_n, QB_n, etc. = the level of QA, QB, etc., respectively before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74		DM54LS/74LS			UNITS	
				96		LS96				
				MIN	TYP(1)	MAX	MIN	TYP(1)		MAX
V _{IH}	High Level Input Voltage				2			2	V	
V _{IL}	Low Level Input Voltage			DM54		0.8		0.7	V	
				DM74		0.8		0.8		
V _I	Input Clamp Voltage	V _{CC} = Min	I _I = -12 mA I _I = -18 mA			-1.5		-1.5	V	
I _{OH}	High Level Output Current					-400		-400	μA	
V _{OH}	High Level Output Voltage	V _{CC} = Min, V _{IH} = 2V V _{IL} = Max, I _{OH} = -400μA		DM54	2.4	3.4		2.5	3.5	V
				DM74	2.4	3.4		2.7	3.5	
I _{OL}	Low Level Output Current			DM54		16		4	mA	
				DM74		16		8		
V _{OL}	Low Level Output Voltage	V _{CC} = Min V _{IH} = 2V V _{IL} = Max	I _{OL} = Max	DM54	0.2	0.4		0.25	0.4	V
				DM74	0.2	0.4		0.35	0.5	
				DM74				0.25	0.4	
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max	V _I = 5.5V			1			mA	
			V _I = 7V					0.1		
I _{IH}	High Level Input Current	Any Input Except Preset Enable Preset Enable	V _{CC} = Max	V _I = 2.4V		40			μA	
				V _I = 2.7V				20		
				V _I = 2.4V		200				
				V _I = 2.7V				20		
I _{IL}	Low Level Input Current	Any Input Except Preset Enable Preset Enable	V _{CC} = Max, V _I = 0.4V			-1.6		-0.4	mA	
						-8		-2		
I _{OS}	Short Circuit Output Current	V _{CC} = Max(2)		DM54	-20	-57	-30	-130	mA	
				DM74	-18	-57	-30	-130		
I _{CC}	Supply Current	V _{CC} = Max(3)		DM54	48	68	12	20	mA	
				DM74	48	79	12	20		

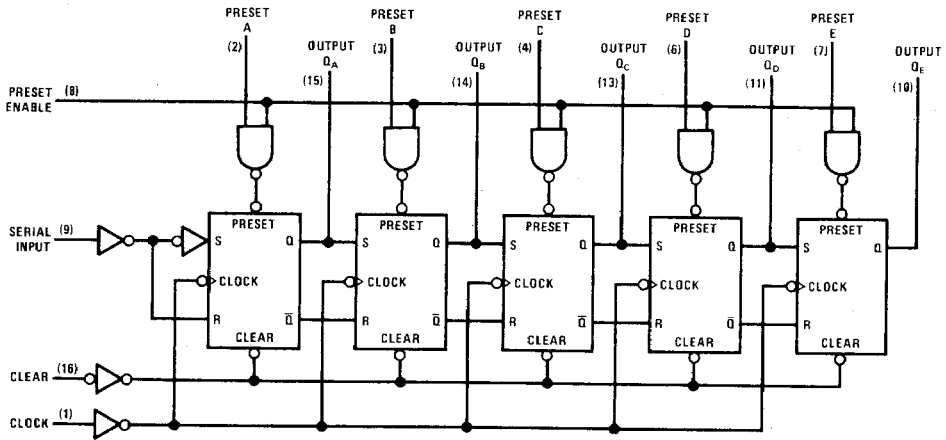
Notes

- (1) All typical values are at V_{CC} = 5V, T_A = 25°C.
- (2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.
- (3) I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS		DM54/74			DM54LS/74LS			UNITS
				96			LS96			
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Maximum Shift Frequency			10				10	MHz	
t _{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock			25	40			25	40	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock			25	40			25	40	ns
t _{PLH}	Propagation Delay Time, Low-to-High Level Output From Preset or Preset Enable		C _L = 15 pF, R _L = 400Ω	25	35		C _L = 15 pF, R _L = 2 kΩ	28	35	ns
t _{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				55			55	ns	
t _{W(CLOCK)}	Width of Clock Input Pulse			35				35	ns	
t _W	Width of Preset and Clear Input Pulse			30				30	ns	
t _{SETUP}	Serial Input Setup Time			30				30	ns	
t _{HOLD}	Serial Input Hold Time			0				0	ns	

Logic Diagram



Timing Diagram

TYPICAL CLEAR, SHIFT, PRESET, AND SHIFT SEQUENCES

