April 1984
Revised March 2000

DM74AS161 • DM74AS163
Synchronous 4-Bit Counter with Asynchronous Clear • Synchronous 4-Bit Counter

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The DM74AS161 and DM74AS163 are 4-bit binary counters. The DM74AS161 clear asynchronously, while the DM74AS163 clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may each be preset to either level. As presetting is synchronous, setting up a low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. LOW-to-HIGH transitions at the $\overline{\text{LOAD}}$ input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The DM74AS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs LOW regardless of the levels of clock, load or enable inputs. This counter is provided with a clear on power-up feature. The DM74AS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs LOW after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all LOW outputs. LOW-to-HIGH transitions at the clear input of the DM74AS163 is also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be HIGH to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the enable P or T inputs of the DM74AS161 and DM74AS163, may occur regardless of the logic level on the clock.

The DM74AS161 and DM74AS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

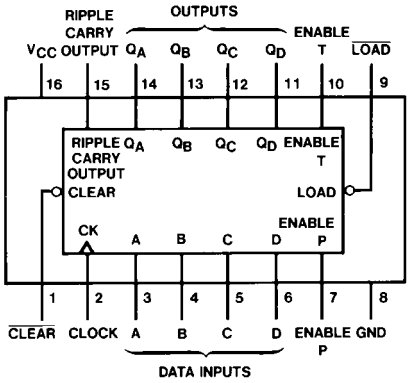
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

Ordering Code:

Order Number	Package Number	Package Description
DM74AS161M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74AS161N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74AS163M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74AS163N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

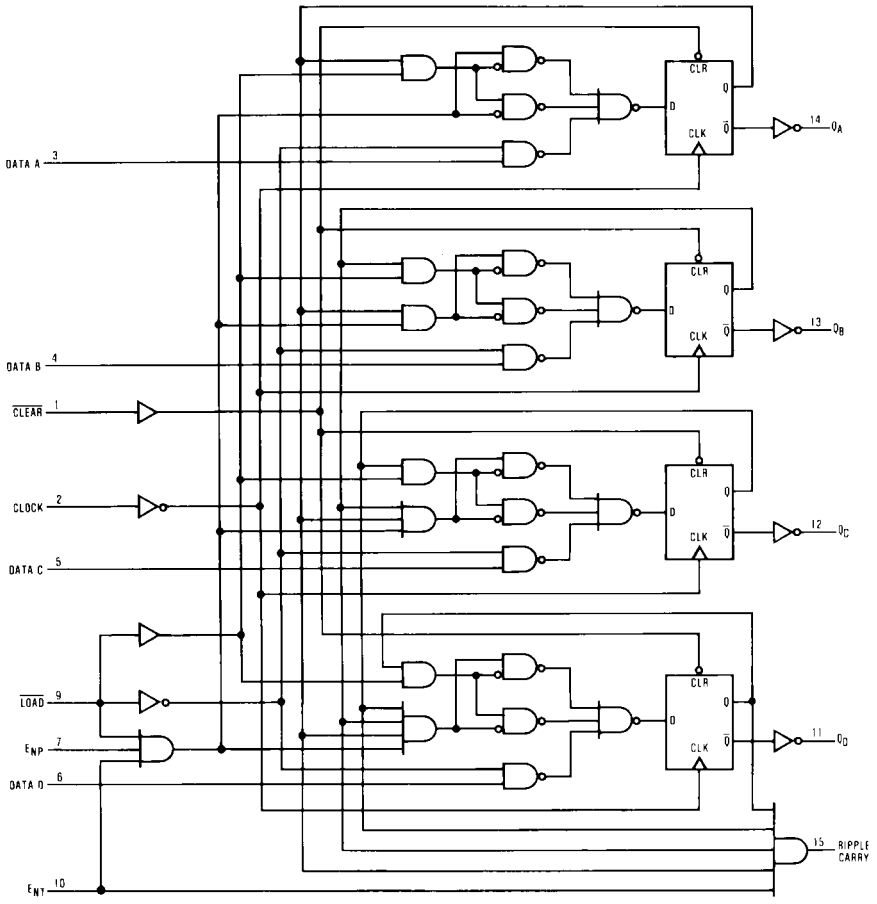
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

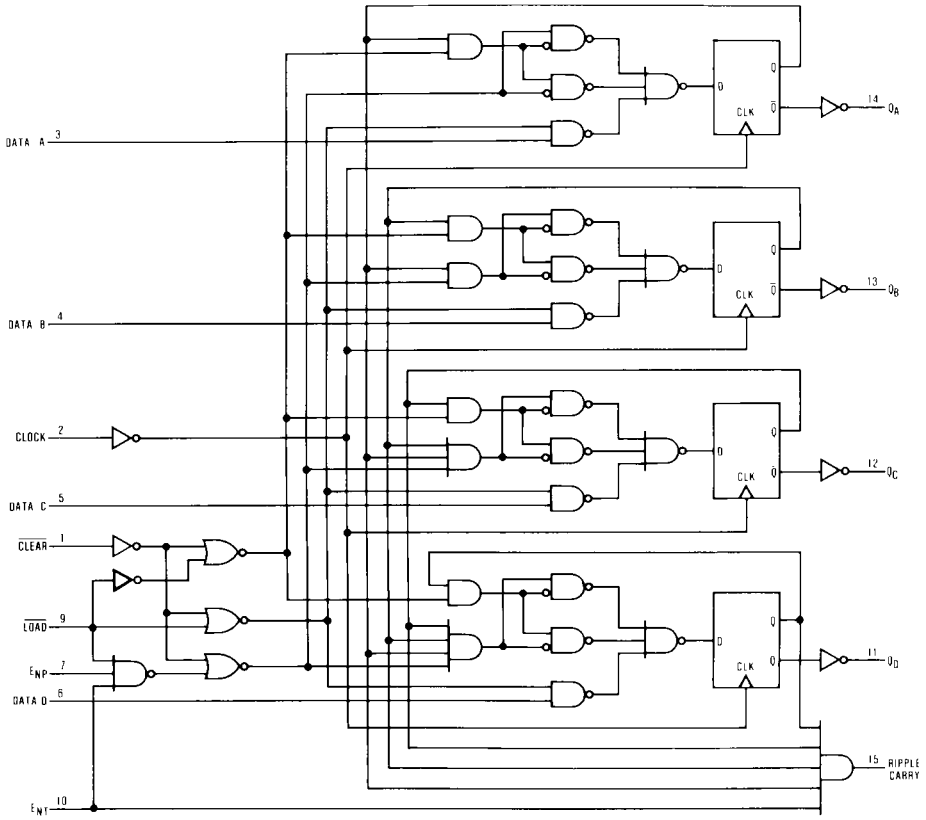


Logic Diagrams

DM74AS161



DM74AS163


DATA A
3
DATA B
4
CLOCK
2
DATA C
5
CLEAR
1
LOAD
9
ENP
7
DATA D
6
ENT
10
D
Q
CLK
14
QA
13
QB
12
QC
11
QD
15
RIPPLE CARRY

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	71.5°C/W
M Package	101.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter			Min	Nom	Max	Units
V_{CC}	Supply Voltage			4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage			2			V
V_{IL}	LOW Level Input Voltage					0.8	V
I_{OH}	HIGH Level Output Current					−2	mA
I_{OL}	LOW Level Output Current					20	mA
f_{CLK}	Clock Frequency			0		75	MHz
t_{SU}	t_{SETUP}, Set-Up Time	Data; A, B, C, D		8			ns
		En P, En T		8			ns
		$\overline{LOAD}$		8			ns
		$\overline{CLEAR}$ (Only for DM74AS163)	LOW	12			ns
			HIGH	9			
	Set-up 1 (Only for DM74AS161)	$\overline{CLEAR}$		8			ns
t_H	t_{HOLD}, Hold Time	Data; A, B, C, D		0			ns
		En P, En T		0			ns
		$\overline{LOAD}$		0			ns
		$\overline{CLEAR}$ (Only for DM74AS163)		0			ns
	Hold 0 (Only for DM74AS161)	$\overline{CLEAR}$		0			ns
t_{WCLK}	Width of Clock Pulse			6.7			ns
t_{WCLR}	Width of Clear Pulse, (DM74ASAS161 LOW)			8			ns

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -2$ mA, $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 20$ mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$	$\overline{LOAD}$			0.3	mA
			ENT			0.2	
			Others			0.1	
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$	$\overline{LOAD}$			60	µA
			ENT			40	
			Others			20	
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	$\overline{LOAD}$			−0.5	mA
			ENT			−1	
			Others			−0.5	
I_O (Note 2)	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			35	53	mA

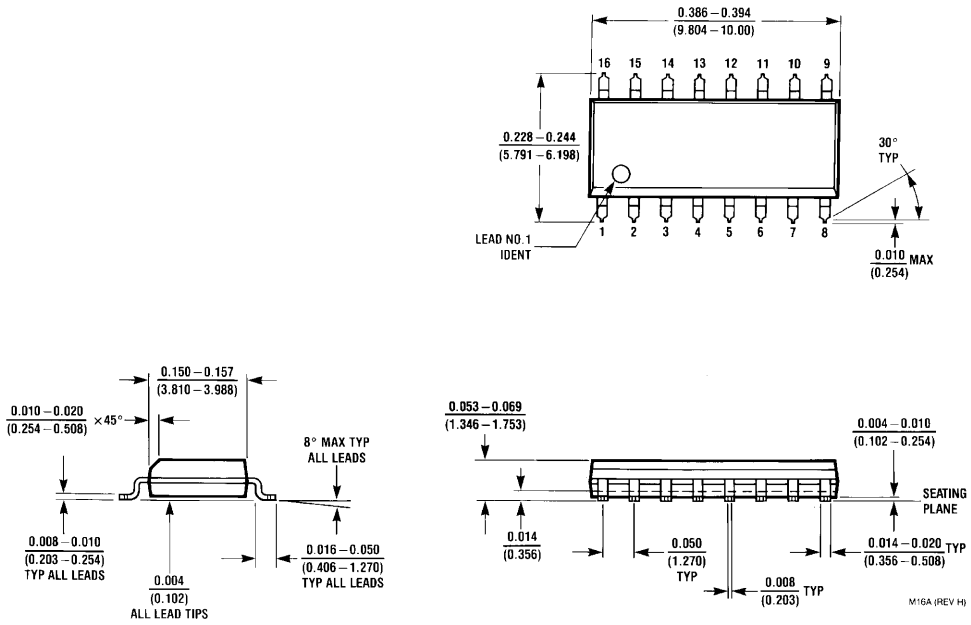
Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Switching Characteristics

over recommended operating free air temperature range

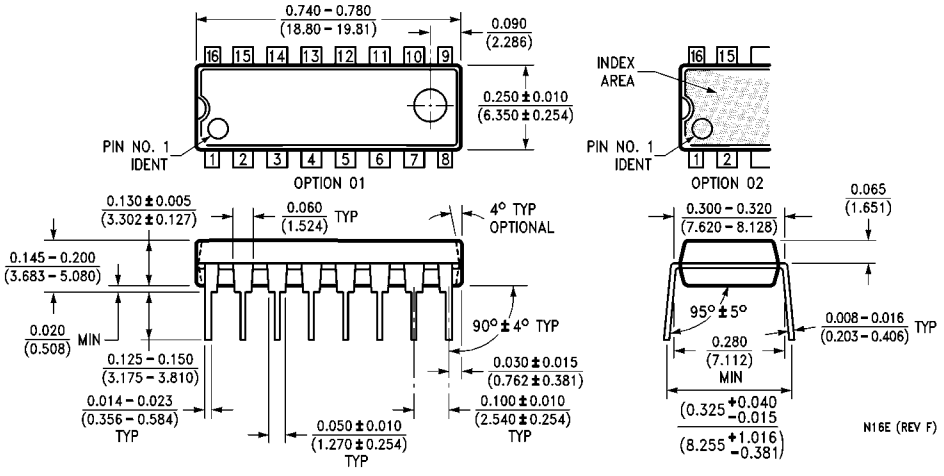
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5V$ to 5.5V			75		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$R_L = 500\Omega$ $C_L = 50$ pF	Clock	Ripple Carry	2	12.5	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output with Load HIGH		Clock	Ripple Carry	1	8	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output with Load LOW		Clock	Ripple Carry	3	16.5	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		Clock	Any Q	1	7	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		Clock	Any Q	2	13	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		En T	Ripple Carry	1.5	9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		En T	Ripple Carry	1	8.5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		$\overline{CLEAR}$ (DM74AS161)	Any Q	2	13	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		$\overline{CLEAR}$ (DM74AS161)	Ripple Carry	2	12.5	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E