

## DM54S195/DM74S195 4-Bit Parallel Access Shift Registers

### General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction  $Q_A$  toward  $Q_D$ )

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

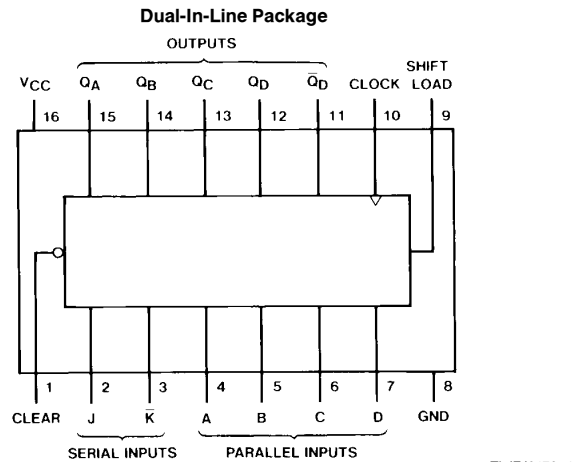
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D, or T-type flip-flop as shown in the truth table.

The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

### Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and  $\bar{K}$  inputs to first stage
- Complementary outputs from last stage
- For use in high-performance: accumulators/processors serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 105 MHz
- Typical power dissipation 350 mW

### Connection Diagram



**Order Number DM54S195J or DM74S195N**  
**See NS Package Number J16A or N16E**

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	–55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54S195			DM74S195			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			–1			–1	mA
I <sub>OL</sub>	Low Level Output Current			20			20	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)	0	105	70	0	105	70	MHz
f <sub>CLK</sub>	Clock Frequency (Note 2)	0	90	60	0	90	60	MHz
t <sub>w</sub>	Pulse Width (Note 3)	Clock			7			ns
		Clear			12			
t <sub>SU</sub>	Setup Time (Note 3)	Shift/Load			11			ns
		Data			5			
t <sub>H</sub>	Data Hold Time (Note 3)	3			3			ns
t <sub>REL</sub>	Shift/Load Release Time (Note 3)	6			6			ns
	Clear Release Time (Note 3)	9			9			
T <sub>A</sub>	Free Air Operating Temperature	–55		125	0		70	°C

Note 1: C<sub>L</sub> = 15 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 2: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 3: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.2	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	DM54	2.5	3.4	V
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	2.7	3.4	
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.5	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			50	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.5V			–2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 5)	DM54	–40	–100	mA
			DM74	–40	–100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 6)		70	109	mA

Note 4: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, K, and data inputs, I<sub>CC</sub> is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

## Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		70		60		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Any Q		12		15	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Any Q		16.5		20	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clear to Any Q		18.5		23	ns

## Function Table

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial		Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	$\uparrow$	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{D0}$
H	H	$\uparrow$	L	H	X	X	X	X	$Q_{A0}$	$Q_{A0}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	L	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	H	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	H	L	X	X	X	X	$\bar{Q}_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

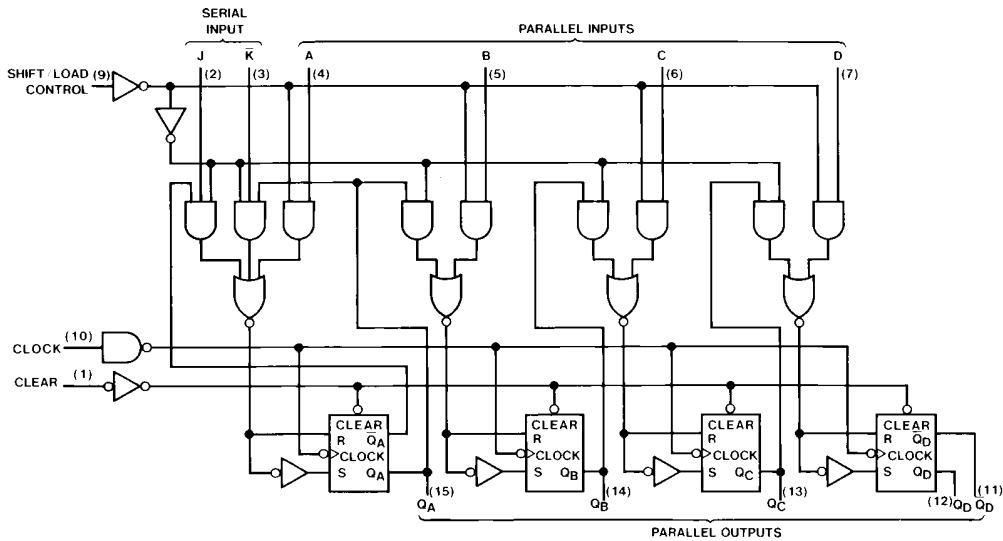
$\uparrow$  = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

$Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$  = The level of  $Q_A, Q_B, Q_C,$  or  $Q_D,$  respectively, before the indicated steady state input conditions were established.

$Q_{An}, Q_{Bn}, Q_{Cn}$  = The level of  $Q_A, Q_B, Q_C,$  respectively, before the most recent transition of the clock.

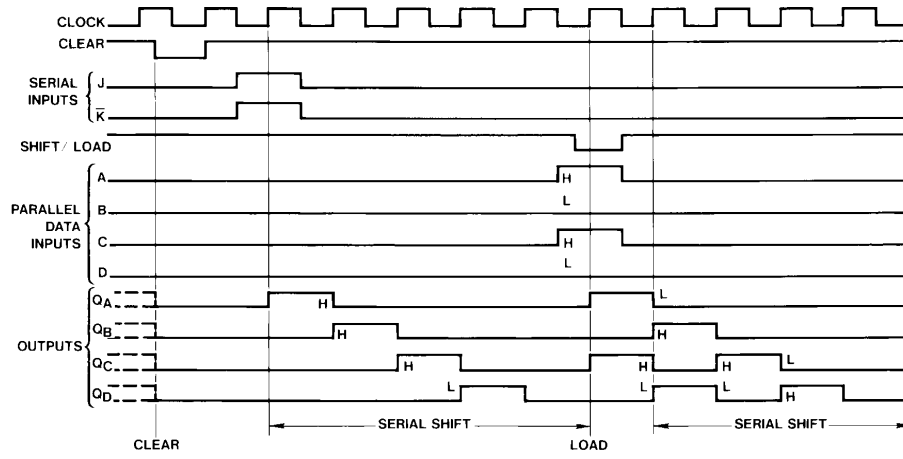
## Logic Diagram



TL/F/6476-2

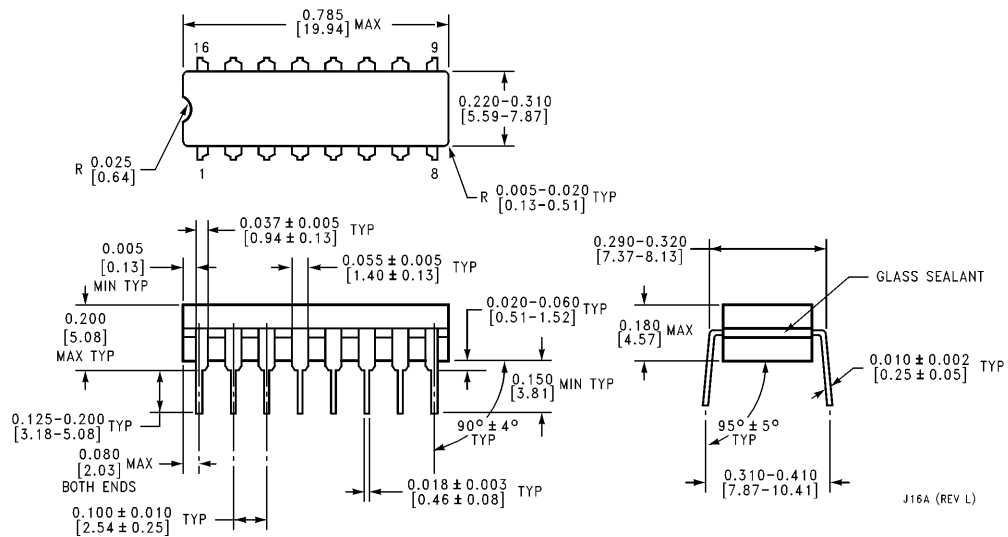
# Timing Diagram

## Typical Clear, Shift, and Load Sequences



TL/F/6476-3

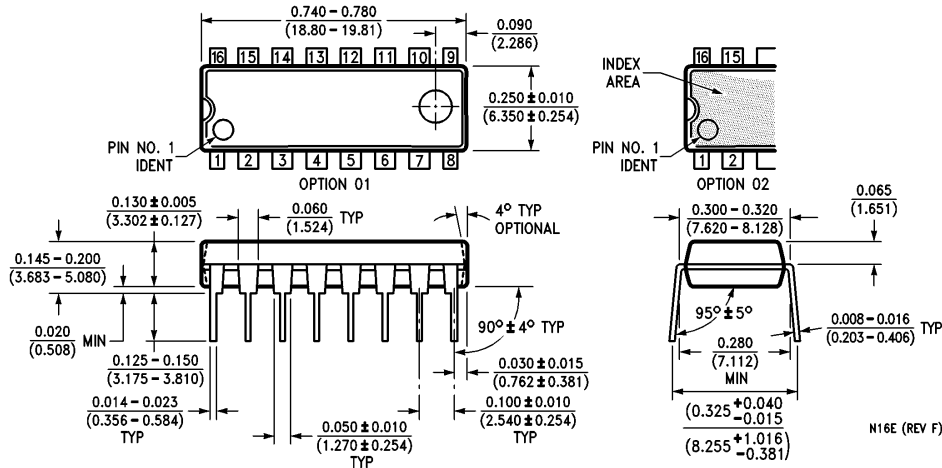
**Physical Dimensions** inches (millimeters)



**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54S195J**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74S195N**  
**NS Package Number N16E**

N16E (REV F)

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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: cnjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 19th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
 Tel: 81-043-299-2309  
 Fax: 81-043-299-2408

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