DS1963L
4k-BIT MONETARY iButton™

www.dalsemi.com

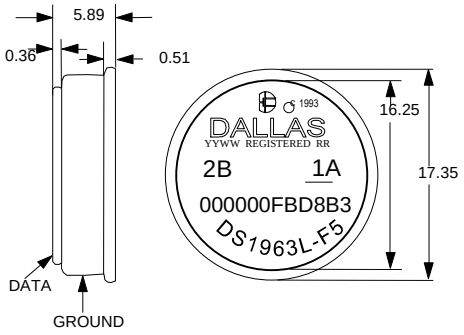
SPECIAL FEATURES

- 4096 bits of read/write nonvolatile memory
- Overdrive mode boosts communication speed to 142 kbits per second
- 256-bit scratchpad ensures integrity of data transfer
- Memory partitioned into 256-bit pages for packetizing data
- Data integrity assured with strict read/write protocols
- Four 32-bit read-only non rolling-over page write cycle counters
- 32 factory-preset tamper-detect bits to indicate physical intrusion
- On-chip 16-bit CRC generator for safeguarding data transfers
- Operating temperature range from -40°C to +70°C
- Over 10 years of data retention

COMMON iButton FEATURES

- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN
- Digital identification and information by momentary contact
- Chip-based data carrier compactly stores information
- Can be accessed while affixed to object
- Economically communicates to host with a single digital signal at 16.3 kbits per second
- Standard 16-mm diameter and 1-Wire™ protocol ensure compatibility with iButton device family
- Button shape is self-aligning with cup-shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

F5 MICROCAN ™



All dimensions in millimeters.

ORDERING INFORMATION

DS1963L-F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self-Stick Adhesive Pad
DS9101	Multi-Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap-In Fob
DS9092	iButton Probe

iButton DESCRIPTION

The DS1963L Monetary iButton is a rugged read/write data carrier that acts as a localized database that can be easily accessed with minimal hardware. The nonvolatile memory offers a simple solution to storing and retrieving information pertaining to the object to which the iButton is associated. Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory lasered into each DS1963L to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1963L to be easily used by human operators. Accessories permit the DS1963L to be mounted on almost any surface including plastic key fobs, photo-ID badges and printed circuit boards.

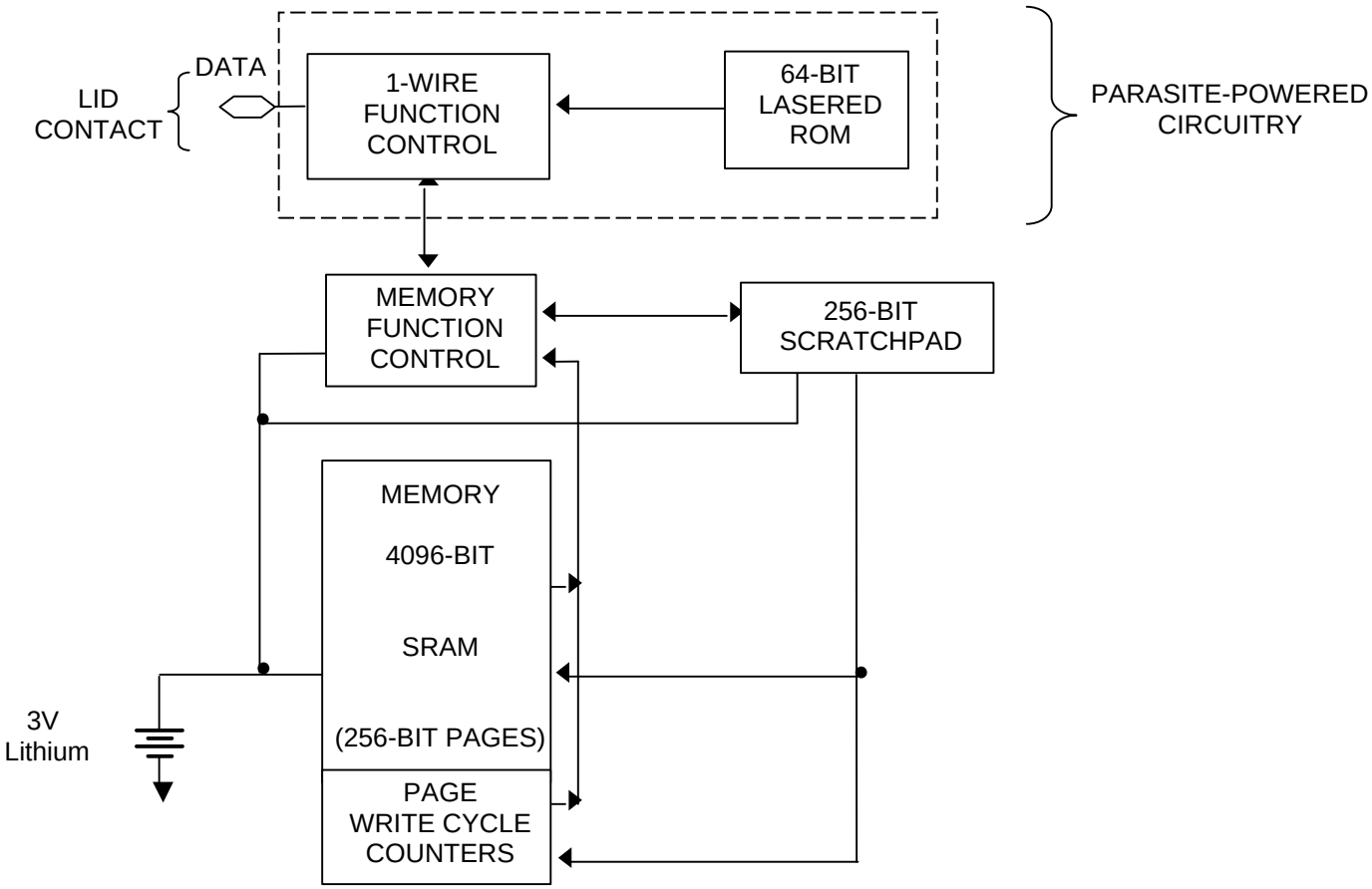
APPLICATION

The DS1963L Monetary iButton can store encrypted data which represents money. The unique registration number, the page write cycle counters, CRC generator and tamper-detect bits prevent unauthorized refilling of the purses. Four independent change purses can be randomly accessed from the on-chip directory. Tamper-detect bits report if the purses have experienced physical tampering. Each write cycle (“Monetary Transaction”) generates a unique number to audit the dispensing and refilling of the purses. A change purse can be decremented with less than 100 ms touch dwell time for rapid processing in crowded public facilities.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1963L. The DS1963L has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) four 32-bit read-only page write cycle counters. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. Each of these counters is associated with one of the 256-bit memory pages. The four counters of the DS1963L are associated with pages 12 to 15. The contents of the counter are read together with the memory data using a special command. The bus master must first provide one of the six ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

DS1963L BLOCK DIAGRAM Figure 1



PARASITE POWER

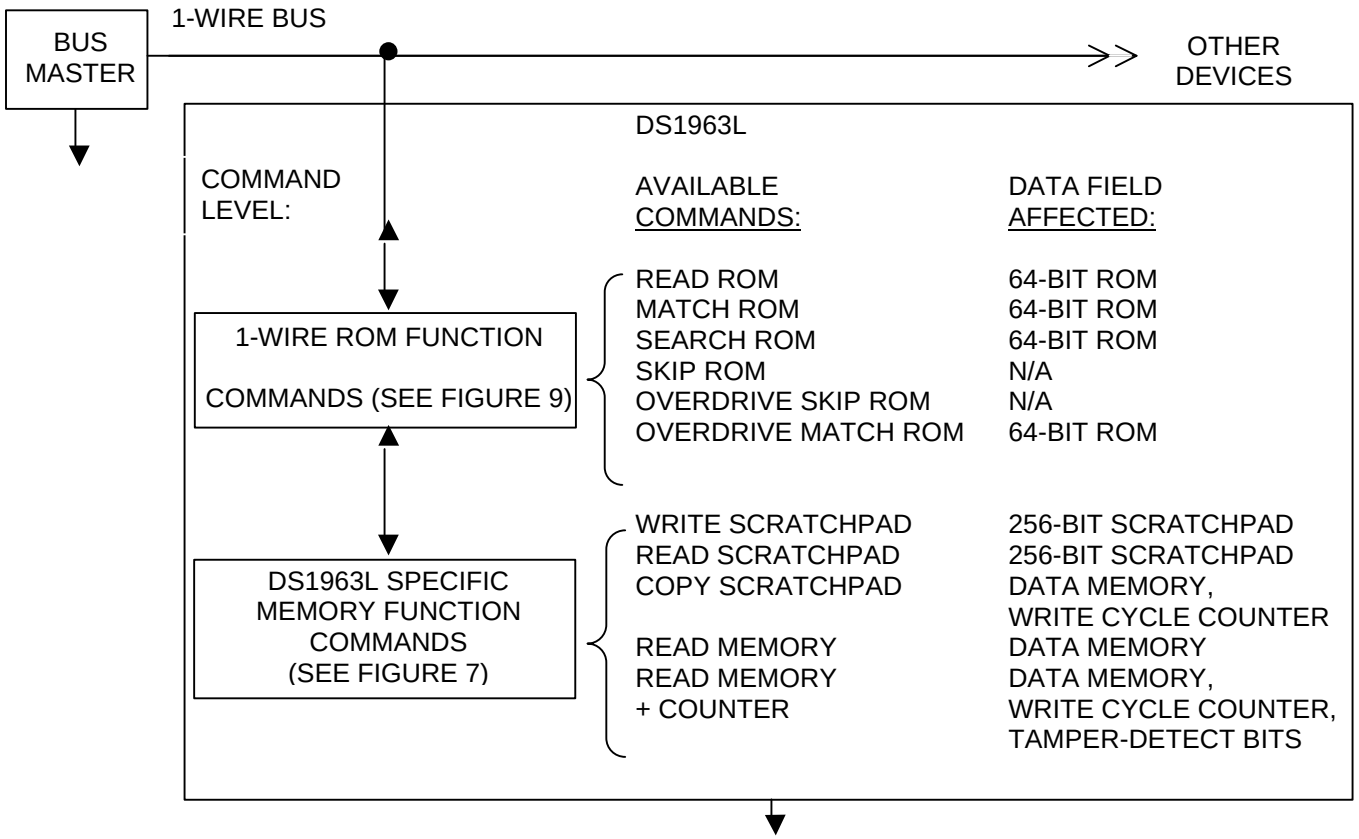
The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved and 2) if the lithium is exhausted for any reason, the ROM may still be read normally.

64-BIT LASERED ROM

Each DS1963L contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards.

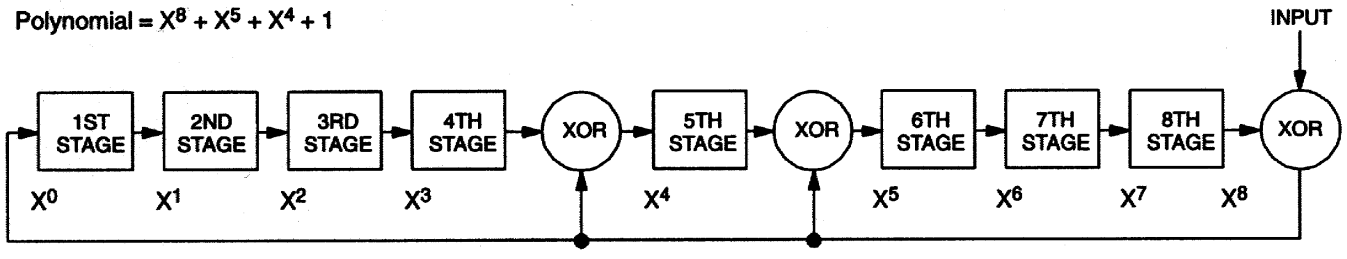
The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

HIERARCHCAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3

1-WIRE CRC GENERATOR Figure 4



MEMORY

The memory map in Figure 5 shows a 32-byte page called the scratchpad and additional 32-byte pages called memory. The DS1963L contains pages 0 through 15 which make up the 4096-bit SRAM. The scratchpad is an additional page that acts as a buffer when writing to memory.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS1963L employs three address registers, called TA1, TA2 and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or "partial byte flag," is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 has no function; it always reads 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address (TA1) for a Write command is 03CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only four bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page; i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial Flag support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

WRITING WITH VERIFICATION

To write data to the DS1963L, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see Write Scratchpad command) the master will receive an inverted CRC16 of the command, address and data at the end of the write scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC16, it has to send the Read Scratchpad command to read back the scratchpad to verify data integrity. As preamble to the scratchpad data, the DS1963L repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the iButton. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue reading and verifying every data byte. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S. The master may obtain the contents of these registers by reading the scratchpad or derive it from the target address and the amount of data to be written. As soon as the DS1963L has received these bytes correctly, it will copy the data to the requested location beginning at the target address.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart. The communication between master and DS1963L takes place either at regular speed (default, OD = 0) or at Overdrive speed (OD = 1). If not explicitly set into the Overdrive mode the DS1963L assumes regular speed.

Write Scratchpad Command [0FH]

After issuing the write scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4: E0) will be the byte offset at which the master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete its content will be ignored and the partial byte flag PF will be set.

When executing the Write Scratchpad command the CRC generator inside the DS1963L (see Figure 12) calculates a CRC over the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0FH) of the Write Scratchpad command, the Target Addresses TA1 and TA2 as supplied by the master and all the data bytes. The master may end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master may send 16 read time slots and will receive the CRC generated by the DS1963L.

The memory address range of the DS1963L is 0000H to 01FFH. If the bus master sends a target address higher than this, the internal circuitry of the chip will set the seven most significant address bits to 0 as they are shifted into the internal address register. The Read Scratchpad command will reveal the target address as it will be used by the DS1963L. The master will identify such address modifications by comparing the target address read back to the target address transmitted. If the master does not read the scratchpad, a subsequent copy scratchpad command will not work since the most significant bits of the target address the master sends will not match the value the DS1963L expects.

Read Scratchpad Command [AAH]

This command is used to verify scratchpad data and target address. After issuing the read scratchpad command, the master begins reading. The first 2 bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The master may read data until the end of the scratchpad after which the data read will be all logic 1's.

Copy Scratchpad [5AH]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the master must provide a 3-byte authorization pattern which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A pattern of alternating 1s and 0s will be transmitted after the data has been copied until a reset pulse is issued by the master. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 30 µs.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. The AA flag will be cleared only by executing a write scratchpad command.

Read Memory [F0H]

The read memory command may be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the 2 bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1s will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1963L provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the Book of DS19xx iButton Standards, Chapter 7 for the recommended file structure.)

DS1963L MEMORY MAP Figure 5

ADDRESS		
	32-BYTE INTERMEDIATE STORAGE SCRATCHPAD	
0000H TO 001FH	32-BYTE FINAL STORAGE NV RAM	page 0
0020H TO 003FH	32-BYTE FINAL STORAGE NV RAM	page 1
0040H TO 005FH	32-BYTE FINAL STORAGE NV RAM	page 2
0060H TO 007FH	32-BYTE FINAL STORAGE NV RAM	page 3
0080H TO 017FH	FINAL STORAGE NV RAM	page 4 to page 11
0180H TO 019FH	32-BYTE FINAL STORAGE NV RAM	page 12
01A0H TO 01BFH	32-BYTE FINAL STORAGE NV RAM	page 13
01C0H TO 01DFH	32-BYTE FINAL STORAGE NV RAM	page 14
01E0H TO 01FFH	32-BYTE FINAL STORAGE NV RAM	page 15

NON-MEMORY MAPPED WRITE-CYCLE COUNTERS (ACCESSIBLE THROUGH A SPECIAL READ COMMAND)

COUNTER 1	WITH PAGE 12
COUNTER 2	WITH PAGE 13
COUNTER 3	WITH PAGE 14
COUNTER 4	WITH PAGE 15

ADDRESS REGISTERS Figure 6

TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	1)	PF	E4	E3	E2	E1	E0

1) THIS BIT WILL ALWAYS BE 0.

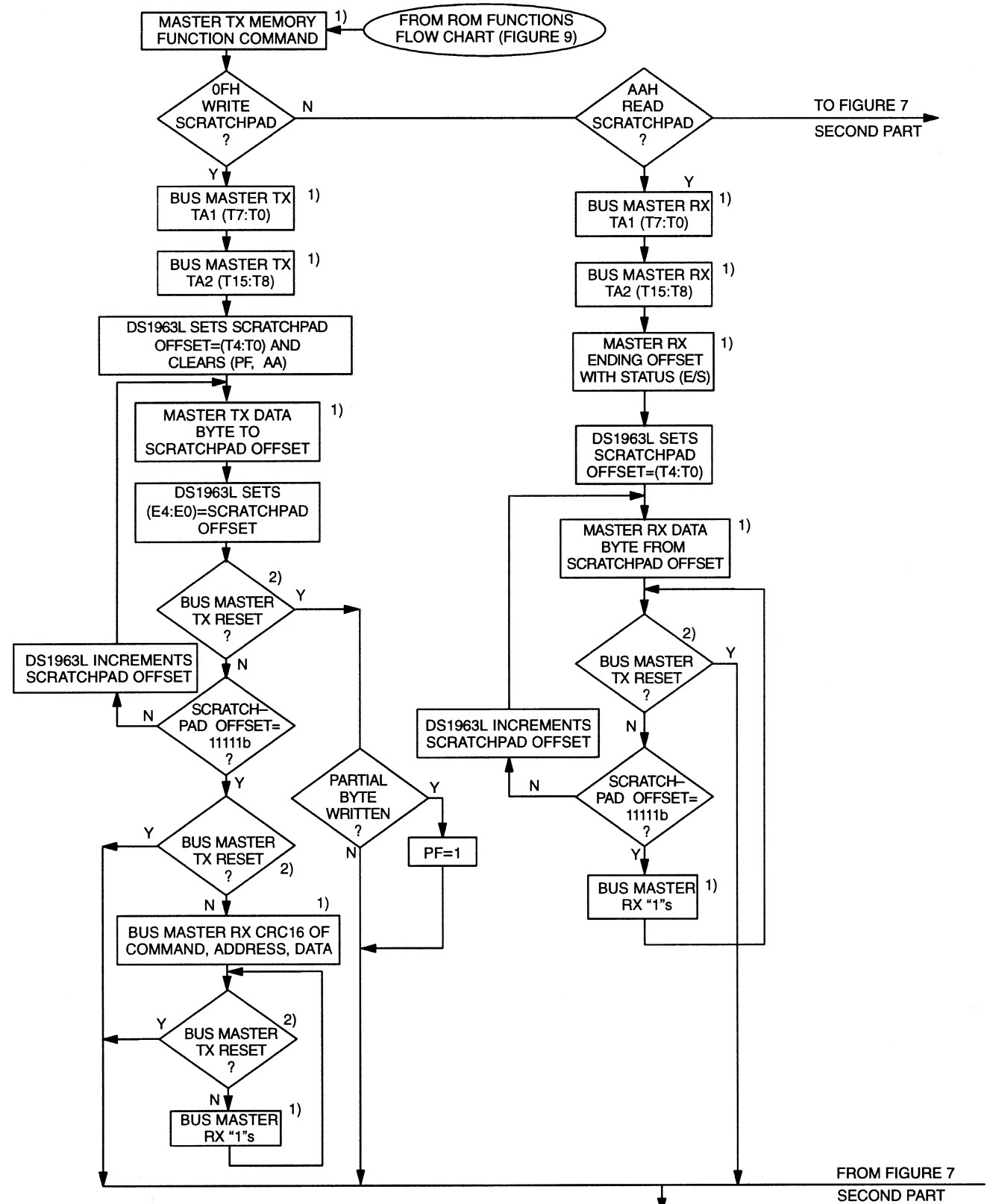
Read Memory + Counter [A5H]

The Read Memory + Counter command is used to read memory data together with the write cycle counter associated with the addressed page of data memory. The additional information is transmitted by the DS1963L as the end of a memory page is encountered. Following the current value of the page write cycle counter the DS1963L transmits 32 tamper-detect bits and a 16-bit CRC generated by the DS1963L. The tamper-detect bits are factory-preset to 55555555H and locked. Tampering with the device will change this data pattern.

After having sent the command code of the Read Memory + Counter command, the bus master sends a 2-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With the subsequent read data time slots the master receives data from the DS1963L starting at the initial address and continuing until the end of a 32-byte page is reached. At that point the bus master will send 80 additional read data time slots and receive the contents of the 32-bit write cycle counter associated with the addressed page, the status of the 32 tamper-detect bits and a 16-bit CRC. With subsequent read data time slots the master will receive data starting at the beginning of the next page followed again by the contents of the page write cycle counter, tamper-detect bits and CRC for that page. This sequence will continue until the final page and its accompanying data are read by the bus master. When applying the Read Memory + Counter command to a page that does not have a page write cycle counter associated, the master will read FFFFFFFFH instead of a valid cycle count.

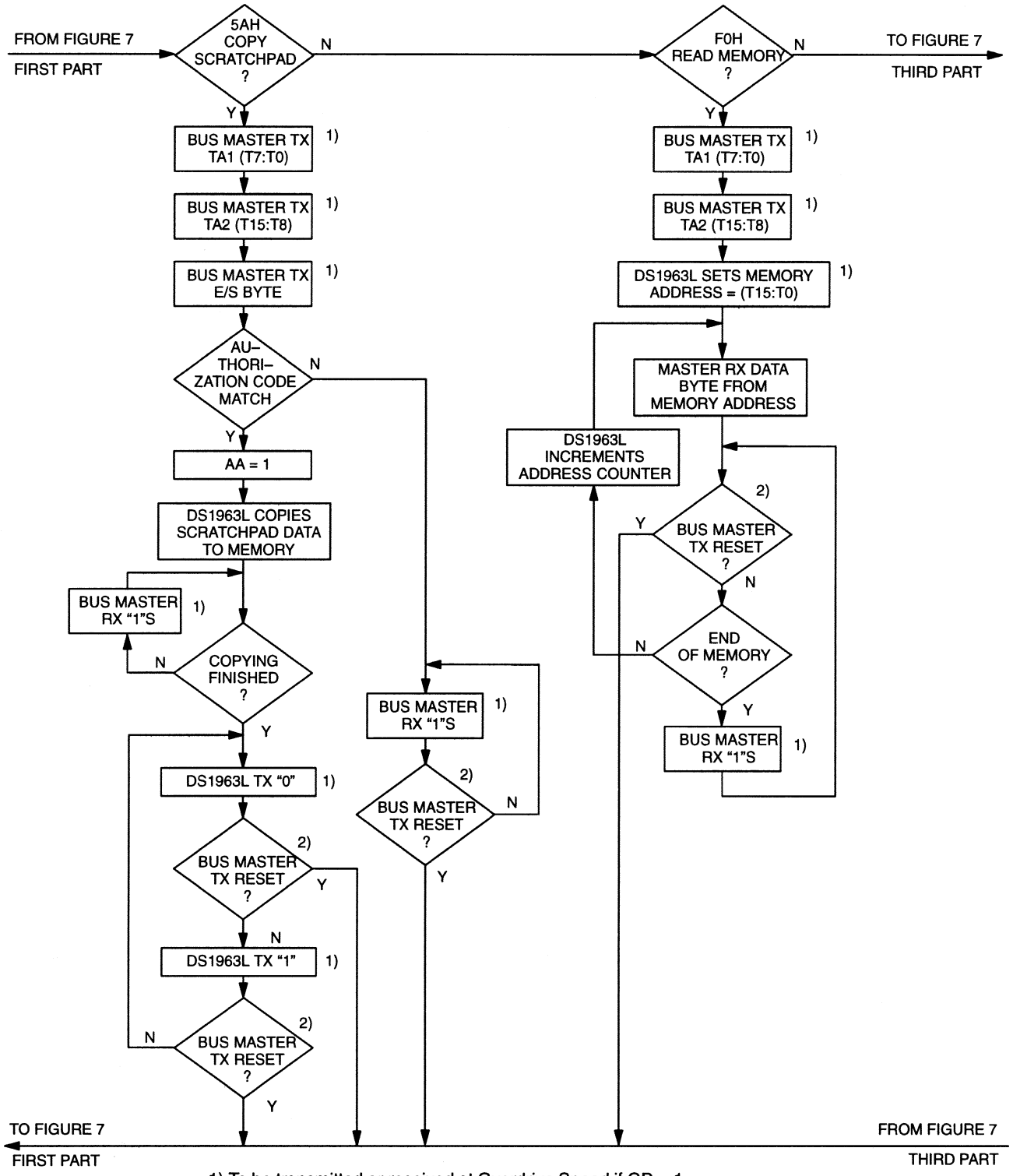
With the initial pass through the Read Memory + Counter flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the 2 address bytes, the contents of the data memory, the write page cycle counter and the tamper-detect bits. Subsequent passes through the Read Memory + Counter flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page, its associated page write cycle counter and tamper-detect bits. After the 16-bit CRC of the last page is read, the bus master will receive logical 1’s from the DS1963L until a Reset Pulse is issued. The Read Memory + Counter command sequence can be ended at any point by issuing a Reset Pulse.

MEMORY FUNCTION FLOW CHART Figure 7



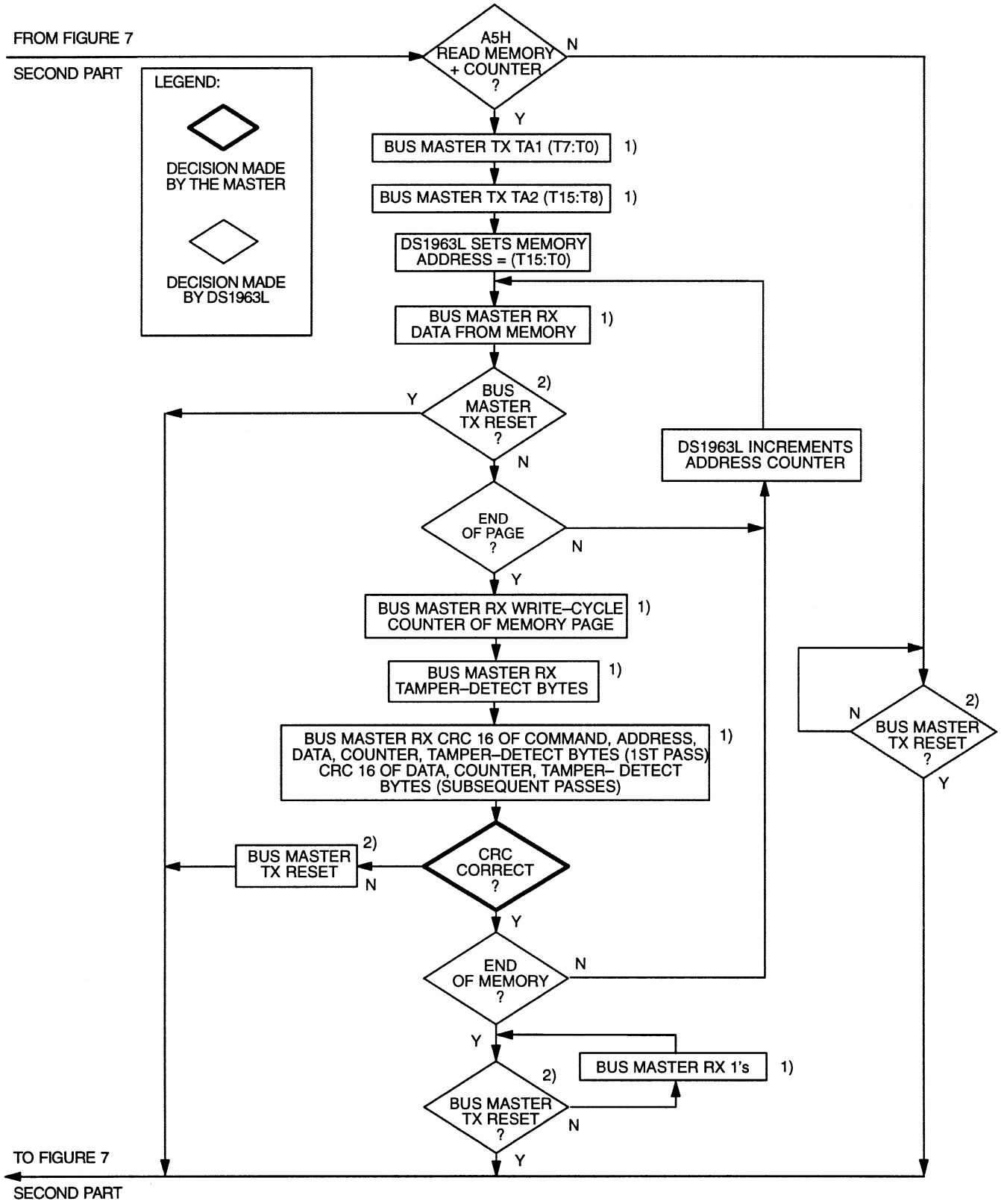
1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1963L is to be reset from Overdrive Speed to regular speed

MEMORY FUNCTION FLOW CHART Figure 7 cont'd



1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1963L is to be reset from Overdrive Speed to regular speed

MEMORY FUNCTION FLOW CHART Figure 7 cont'd



1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1963L is to be reset from Overdrive Speed to regular speed

MEMORY FUNCTION EXAMPLE

Example: Write 2 data bytes to memory location 0026 and 0027. Read entire memory.

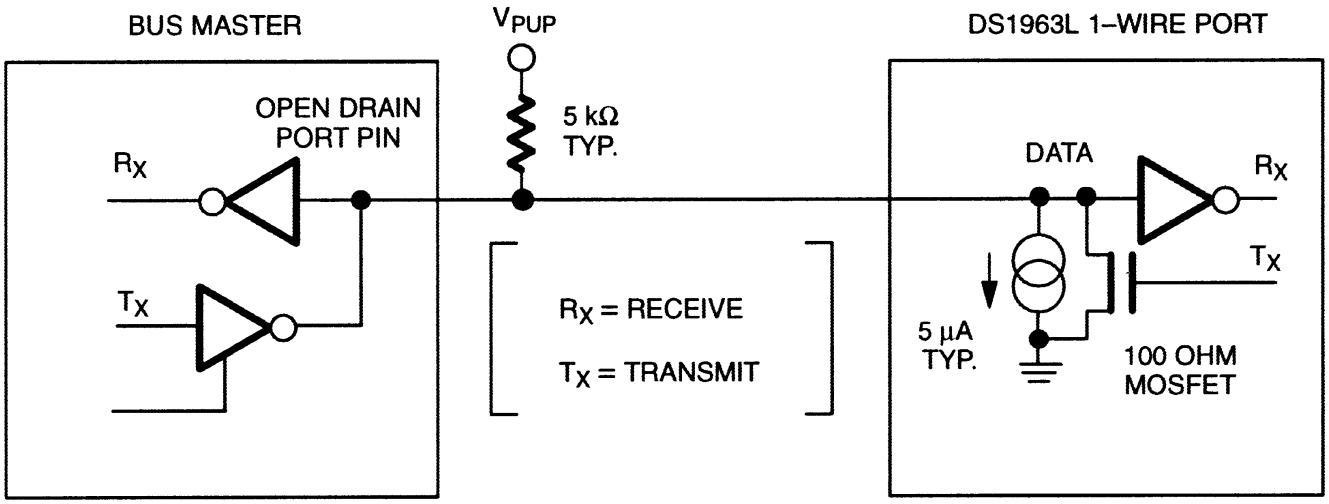
MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	26h	TA1, beginning offset=26h
TX	00h	TA2, address=0026h
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	26h	Read TA1, beginning offset=26h
RX	00h	Read TA2, address=0026h
RX	07h	Read E/S, ending offset=7h, flags=0h
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	5Ah	Issue “copy scratchpad” command
TX	26h	TA1 } AUTHORIZATION CODE
TX	00h	TA2 } AUTHORIZATION CODE
TX	07h	E/S } AUTHORIZATION CODE
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	F0h	Issue “read memory” command
TX	00h	TA1, beginning offset=0
TX	00h	TA2, address=0000h
RX	<512 Bytes>	Read entire memory
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE

Update purse file in page 12: Read Memory + Counter, Write Scratchpad, Copy Scratchpad.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence Pulse
TX	CCh	Issue “skip ROM” command
TX	A5h	Issue “read memory + counter” command
TX	80h	TA1, beginning offset=80h
TX	01h	TA2, address=0180h
RX	<32 data bytes>	Read 32 bytes of data
RX	<4 data bytes>	Read Write Cycle Counter of page 12
RX	<4 data bytes>	Read Tamper Detect Bytes of device
RX	<2 data bytes>	Read(inverted) CRC16
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	80h	Read TA1, beginning offset=80h
TX	01h	Read TA2, address=0180h
TX	<32 data bytes>	Write 32 bytes of data to scratchpad
RX	<2 data bytes>	Read (inverted) CRC16
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	5Ah	Issue “copy scratchpad” command
TX	80h	TA1
TX	01h	TA2 } AUTHORIZATION CODE
TX	1Fh	E/S
RX	<1 data byte>	Read Copy scratchpad response
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

HARDWARE CONFIGURATION Figure 8



1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS1963L is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS1963L is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive mode. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (Overdrive speed) or more than 120 µs (regular speed), one or more devices on the bus may be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1963L via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1963L is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the six ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 9):

Read ROM [33H]

This command allows the bus master to read the DS1963L's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1963L on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

Match ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1963L on a multidrop bus. Only the DS1963L that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wired-AND result).

Search ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Overdrive Skip ROM [3CH]

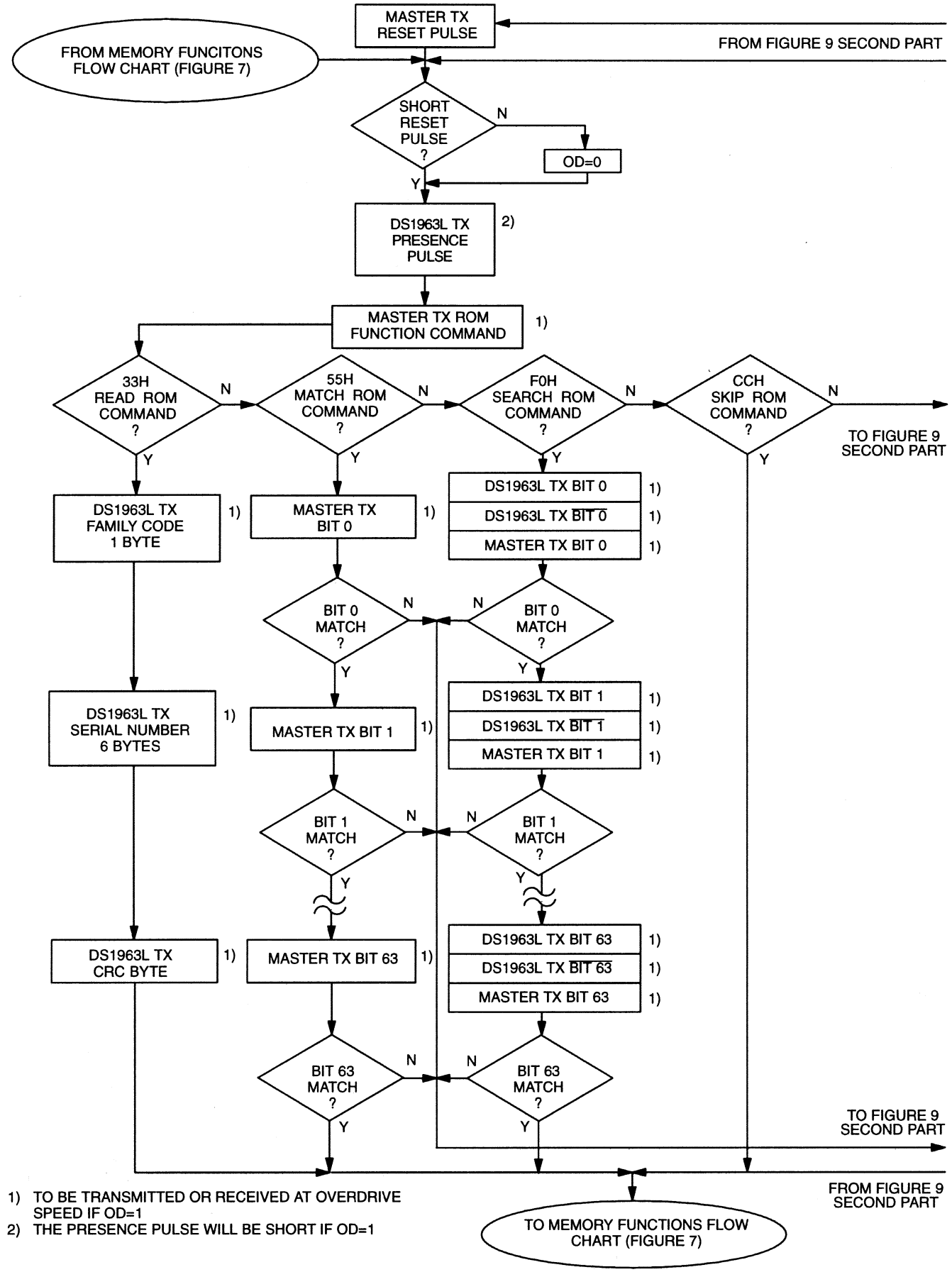
On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS1963L in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD = 0).

When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Overdrive Match ROM [69H]

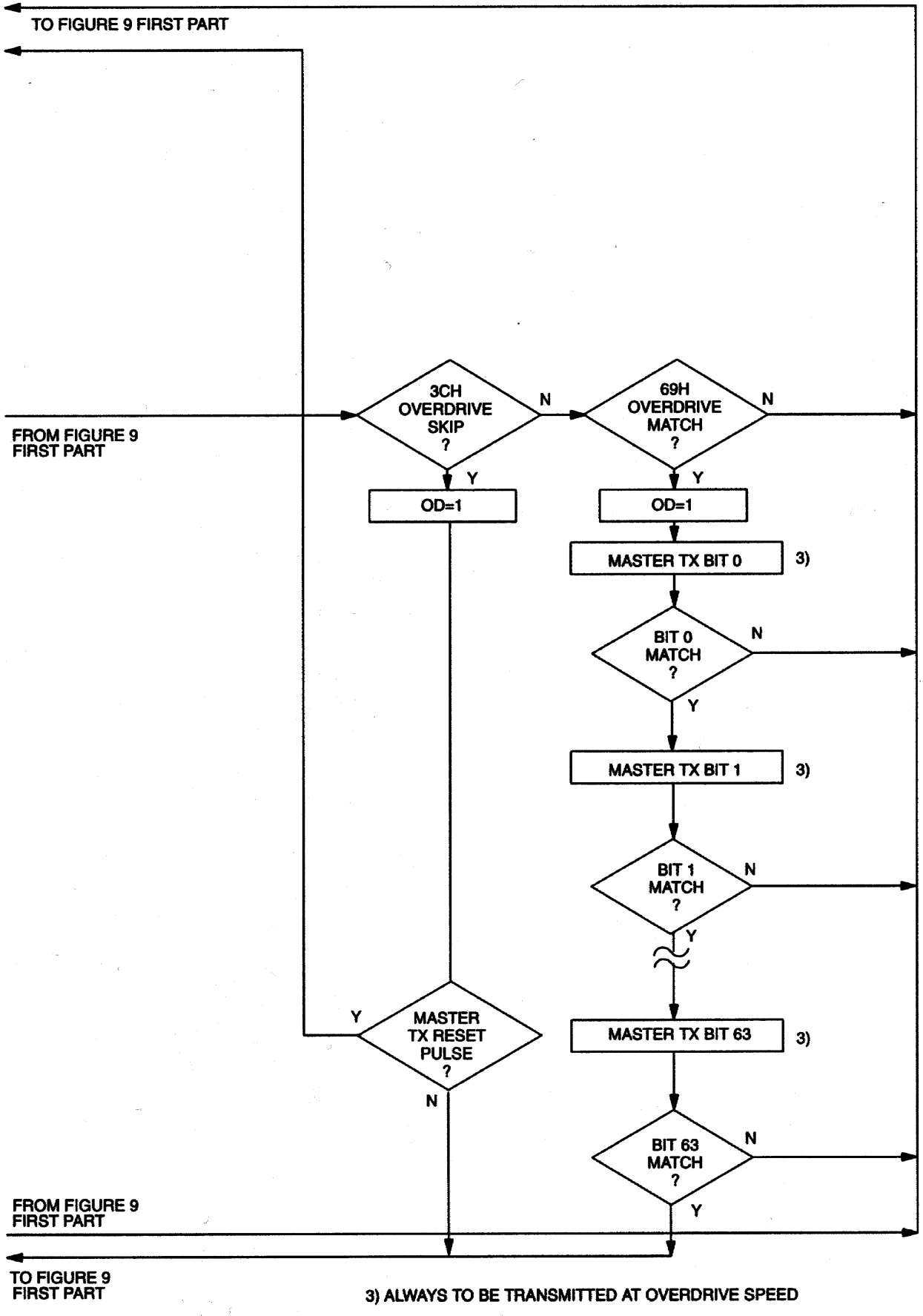
The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive speed, allows the bus master to address a specific DS1963L on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS1963L that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All other slaves that do not match the 64-bit ROM sequence or do not support Overdrive will return to or remain at regular speed and wait for a reset pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

ROM FUNCTIONS FLOW CHART Figure 9



1) TO BE TRANSMITTED OR RECEIVED AT OVERDRIVE SPEED IF OD=1
2) THE PRESENCE PULSE WILL BE SHORT IF OD=1

ROM FUNCTIONS FLOW CHART Figure 9 cont'd



1-WIRE SIGNALING

The DS1963L requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The DS1963L can communicate at two different speeds, regular speed and Overdrive speed. If not explicitly set into the Overdrive mode, the DS1963L will communicate at regular speed. While in Overdrive mode the fast timing applies to all waveforms.

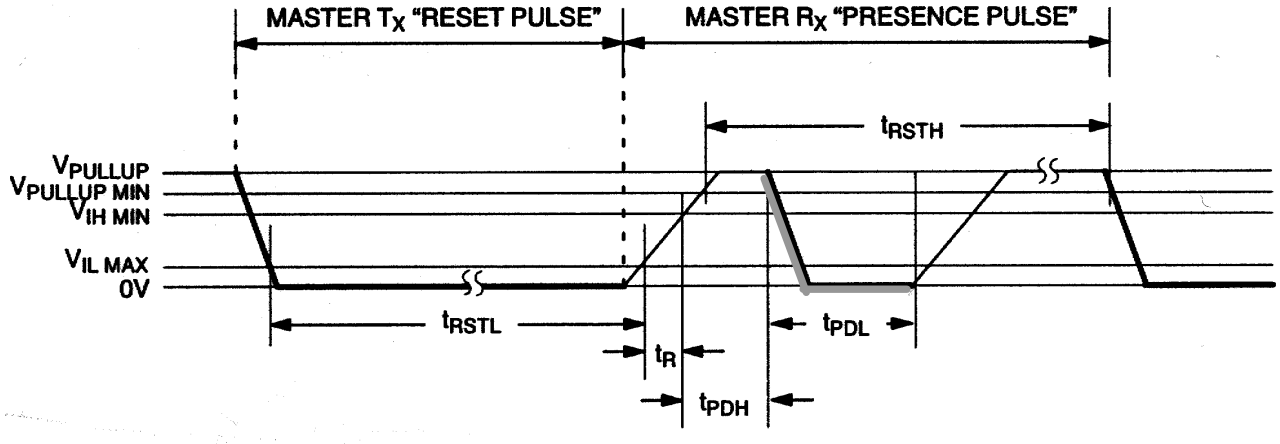
The initialization sequence required to begin any communication with the DS1963L is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1963L is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS1963L waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the presence pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive speed).

A reset pulse of 480 µs or longer will exit the Overdrive mode returning the device to regular speed. If the DS1963L is in Overdrive mode and the reset pulse is no longer than 80 µs the device will remain in Overdrive mode.

Read/Write Time Slots

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1963L to the master by triggering a delay circuit in the DS1963L. During write time slots, the delay circuit determines when the DS1963L will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1963L will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the device will leave the read data time slot unchanged.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PLUSES" Figure 10



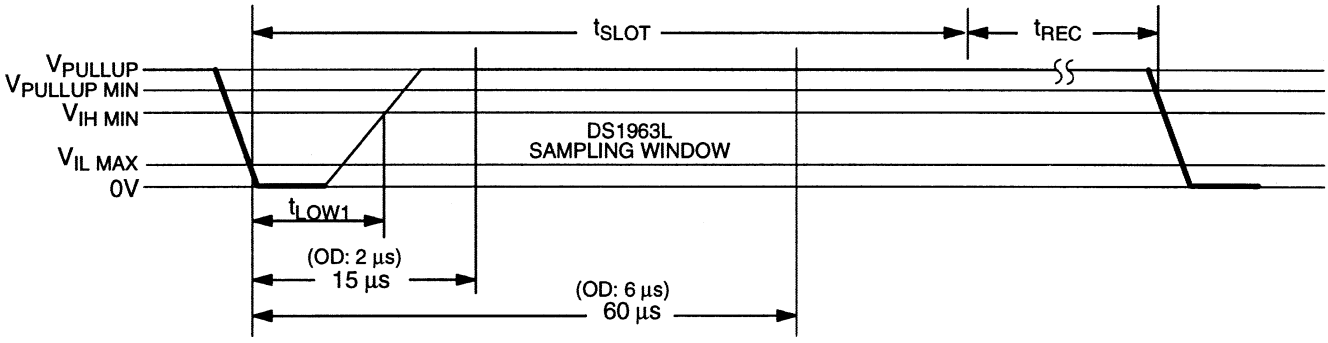
RESISTOR
MASTER
DS1963L

Regular Speed	Overdrive Speed
480 µs ≤ t_{RSTL} < ∞ *	48 µs ≤ t_{RSTL} < 80 µs
480 µs ≤ t_{RSTH} < ∞ **	48 µs ≤ t_{RSTH} < ∞ **
15 µs ≤ t_{PDH} < 60 µs	2 µs ≤ t_{PDH} < 6 µs
60µs ≤ t_{PDL} < 240 µs	8 µs ≤ t_{PDL} < 24 µs

*IN ORDER NOT TO MASK INTERRUPT SIGNALS BY OTHER DEVICES ON THE 1-WIRE BUS, $t_{RSTL + tR}$ SHOULD ALWAYS BE LESS THAN 960 µs
**INCLUDES RECOVERY TIME

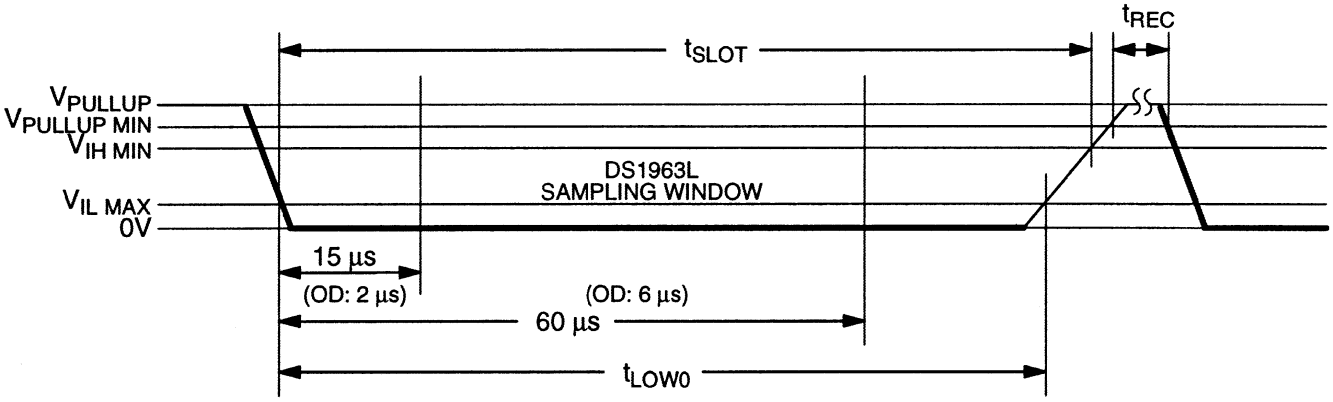
READ/WRITE TIME DIAGRAM Figure 11

Write-1 Time Slot



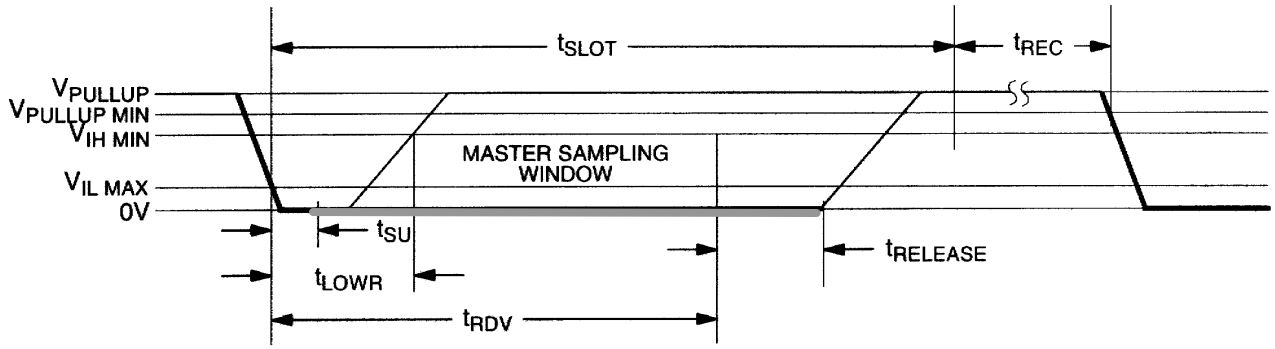
Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1µs ≤ t_{LOW1} < 15 µs	1µs ≤ t_{LOW1} < 2 µs
1µs ≤ t_{REC} < ∞	1µs ≤ t_{REC} < ∞

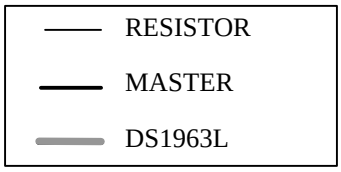
Write-0 Time Slot



Regular Speed	Overdrive Speed
60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs	6 µs ≤ t_{LOW0} < t_{SLOT} < 16 µs
1µs ≤ t_{REC} < ∞	1µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM Figure 11 cont'd
Read-data Time Slot





Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1µs ≤ t_{LOWR} < 15 µs	1µs ≤ t_{LOWR} < 2 µs
0 ≤ $t_{RELEASE}$ < 45 µs	0 ≤ $t_{RELEASE}$ < 4 µs
1µs ≤ t_{REC} < ∞	1µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs	t_{RDV} = 2 µs
t_{SU} < 1µs	t_{SU} < 1µs

CRC GENERATION

With the DS1963L there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1963L to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form when reading the ROM of the DS1963L. It is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for error detection when reading Data Memory using the Read Memory + Counter command and for fast verification of a data transfer when writing to the scratchpad. It is the same type of CRC as is used with NV RAM-based iButtons for error detection within the iButton Extended File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned or sent in the complemented (inverted) form. A CRC-generator inside the DS1963L chip (Figure 12) will calculate a new 16-bit CRC as shown in the command flow chart of Figure 7. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to re-read the portion of the data with the CRC error.

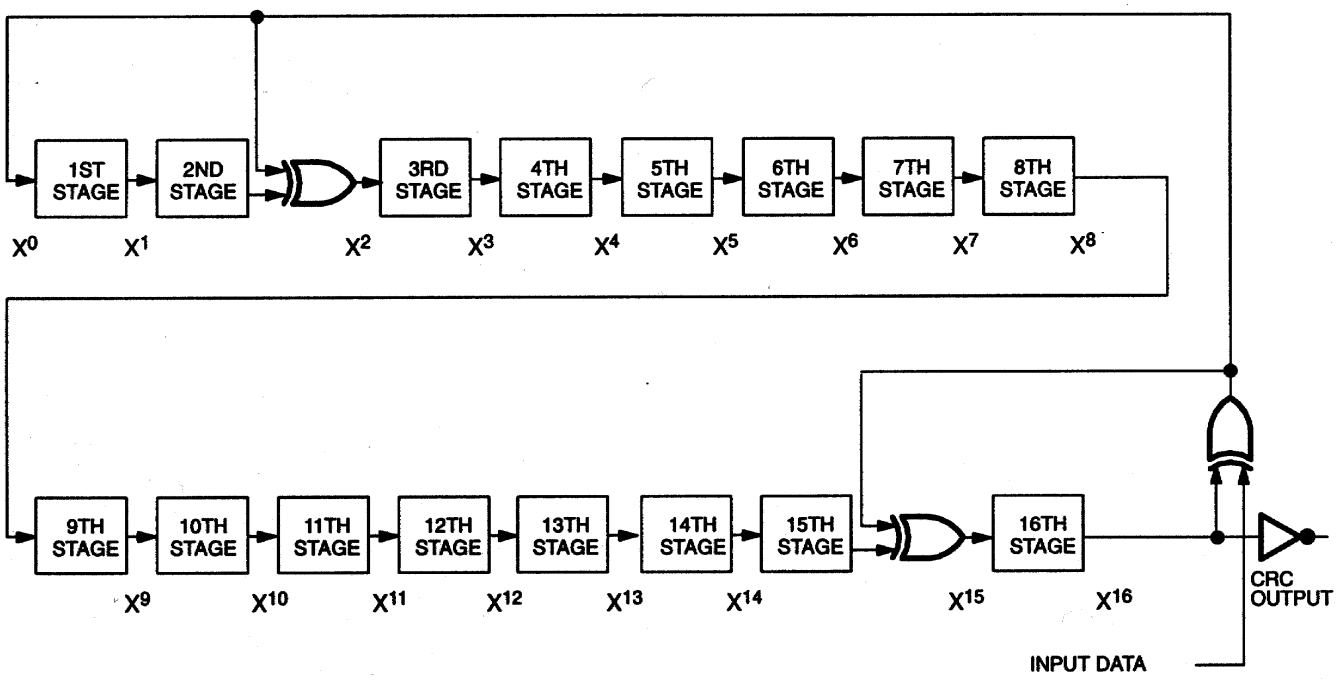
With the initial pass through the Read Memory + Counter flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the 2 address bytes, the data bytes, value of the page write cycle counter and tamper-detect bits. Subsequent passes through the Read Memory + Counter flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes, the value of the page write cycle counter and the tamper-detect bits.

With the Write Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2 and all the data bytes. The DS1963L will transmit this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data may start at any location within the scratchpad.

For more details on generating CRC values including example implementations in both hardware and software, see the "Book of DS19xx iButton Standards."

CRC–16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 12

POLYNOMIAL = $X^{16} + X^{15} + X^2 + 1$



PHYSICAL SPECIFICATION

Size	See mechanical drawing
Weight	3.3 grams
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approval under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICIAL CHARACTERISTIC (V_{PUP}=2.8V to 6.0V; -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1,8
Logic 0	V_{IL}	-0.3		+0.8	V	1,9
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current	I_L		5		µA	3

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

AC ELECTRICAL CHARACTERISTICS REGULAR SPEED

(V_{PUP}=2.8V to 6.0V; -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}		exactly 15		µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	7
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

AC ELECTRICAL CHARACTERISTICS OVERDRIVE SPEED

(V_{PUP}=2.8V to 6.0V; -40°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	
Read Data Valid	t_{RDV}		exactly 2		µs	
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	4
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDH}	2		6	µs	
Presence Detect Low	t_{PDL}	8		24	µs	

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pullup voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

6. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{PUP}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

8. V_{IH} is a function of the external pullup resistor and V_{PUP}.

9. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.