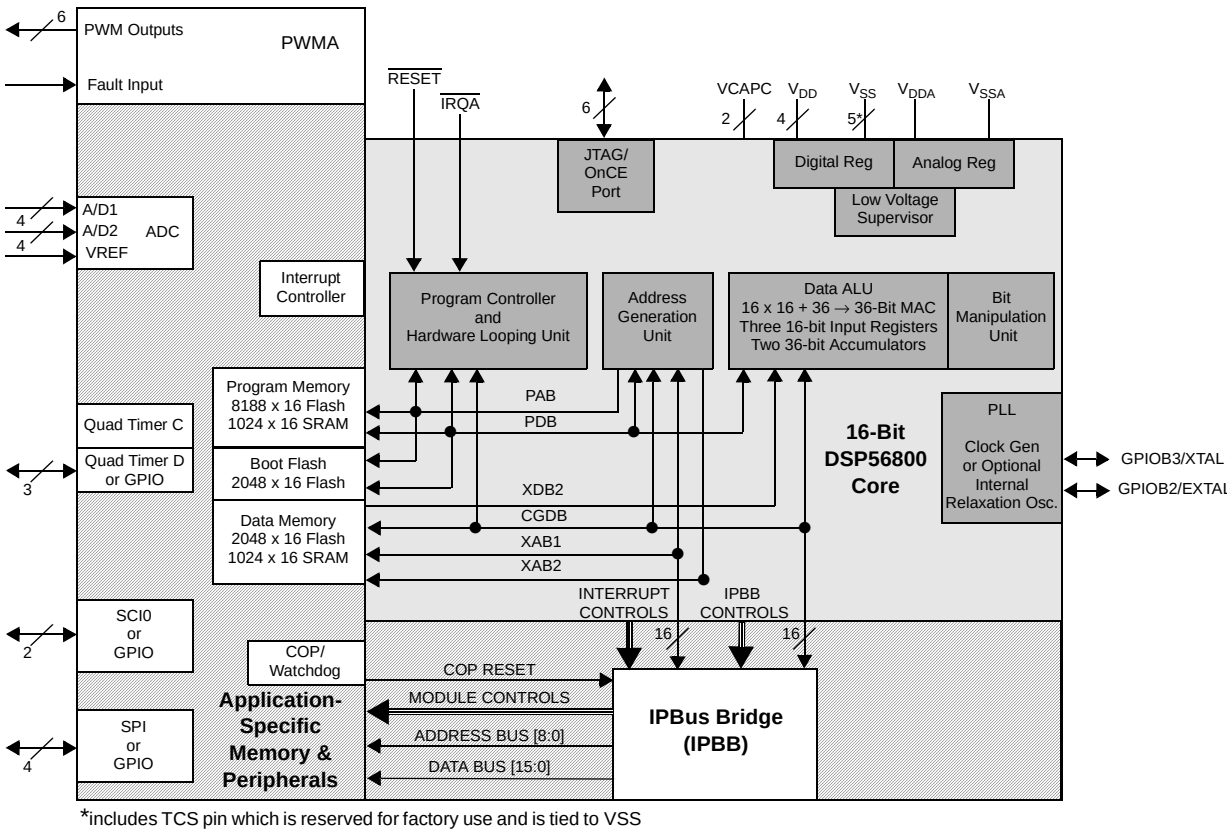
DSP56F801

Preliminary Technical Data

DSP56F801 16-bit Digital Signal Processor

- Up to 40 MIPS operation at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 8K × 16-bit words Program Flash
- 1K × 16-bit words Program RAM
- 2K × 16-bit words Data Flash
- 1K × 16-bit words Data RAM
- 2K × 16-bit words Boot Flash
- Hardware DO and REP loops
- 6-channel PWM Module
- Two 4-channel, 12-bit ADCs
- Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- General Purpose Quad Timer
- JTAG/OnCE™ port for debugging
- On-chip relaxation oscillator
- 11 shared GPIO
- 48-pin LQFP Package



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 1. DSP56F801 Block Diagram

Part 1 Overview

1.1 DSP56F801 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit DSP56800 family DSP engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80 MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume flash solution
  - — 8K × 16 bit words of Program Flash
  - — 1K × 16-bit words of Program RAM
  - — 2K × 16-bit words of Data Flash
  - — 1K × 16-bit words of Data RAM
  - — 2K × 16-bit words of Boot Flash
- Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, SPI)

1.1.3 Peripheral Circuits for DSP56F801

- Pulse Width Modulator (PWM) with six PWM outputs, two Fault inputs, fault-tolerant design with deadtime insertion; supports both center- and edge-aligned modes
- Two 12-bit, Analog-to-Digital Converters (ADCs), which support two simultaneous conversions with two 4-multiplexed inputs; ADC and PWM modules can be synchronized
- General Purpose Quad Timer: Timer D with three pins (or three additional GPIO lines)
- Serial Communication Interface (SCI) with two pins (or two additional GPIO lines)

- Serial Peripheral Interface (SPI) with configurable four-pin port (or four additional GPIO lines)
- Eleven multiplexed General Purpose I/O (GPIO) pins
- Computer-Operating Properly (COP) watchdog timer
- One dedicated external interrupt pin
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the DSP core clock
- Oscillator flexibility between either an external crystal oscillator or an on-chip relaxation oscillator for lower system cost and two additional GPIO lines

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

1.2 DSP56F801 Description

The DSP56F801 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the DSP56F801 is well-suited for many applications. The DSP56F801 includes many peripherals that are especially useful for applications such as motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, noise suppression, remote utility metering, and industrial control for power, lighting, and automation.

The DSP56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The DSP56F801 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The DSP56F801 also provides one external dedicated interrupt lines and up to 11 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The DSP56F801 DSP controller includes 8K words (16-bit) of program Flash and 2K words of Data Flash (each programmable through the JTAG port) with 1K words of both program and data RAM. A total of 2K words of Boot Flash is incorporated for easy customer-inclusion of field-programmable software routines that can be used to program the main program and data flash memory areas. Both program and data flash memories can be independently bulk erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the DSP56F801 is the inclusion of a Pulse Width Modulator (PWM) module. This modules incorporates six complementary, individually programmable PWM signal outputs to

enhance motor control functionality. Complementary operation permits programmable dead-time insertion, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Both edge and center aligned synchronous pulse width control (0% to 100% modulation) are supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard opto-isolators. A "smoke-inhibit", write-once protection feature for key parameters is also included. The PWM is double-buffered and includes interrupt control to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the Analog-to-Digital Converters.

The DSP56F801 incorporates an 8 input, 12-bit Analog-to-Digital Converter (ADC). A full set of standard programmable peripherals is provided that include a Serial Communications Interface (SCI), a Serial Peripheral Interface (SPI), and two Quad Timers. Any of these interfaces can be used as General-Purpose Input/Outputs (GPIO) if that function is not required. An on-chip relaxation oscillator provides flexibility in the choice of either on-chip or externally supplied frequency reference for chip timing operations. Application code is used to select which source is to be used.

1.3 "Best in Class" Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow programmers to create their unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1** are required for a complete description and proper design with the DSP56F801. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/dsp.

Table 1. DSP56F801 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set	DSP56800FM/D
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56F801, DSP56F803, DSP56F805, and DSP56F807	DSP56F801-7UM/D
DSP56F801 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F801/D
DSP56F801 Product Brief	Summary description and block diagram of the DSP56F801 core, memory, peripherals and interfaces	DSP56F801PB/D

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

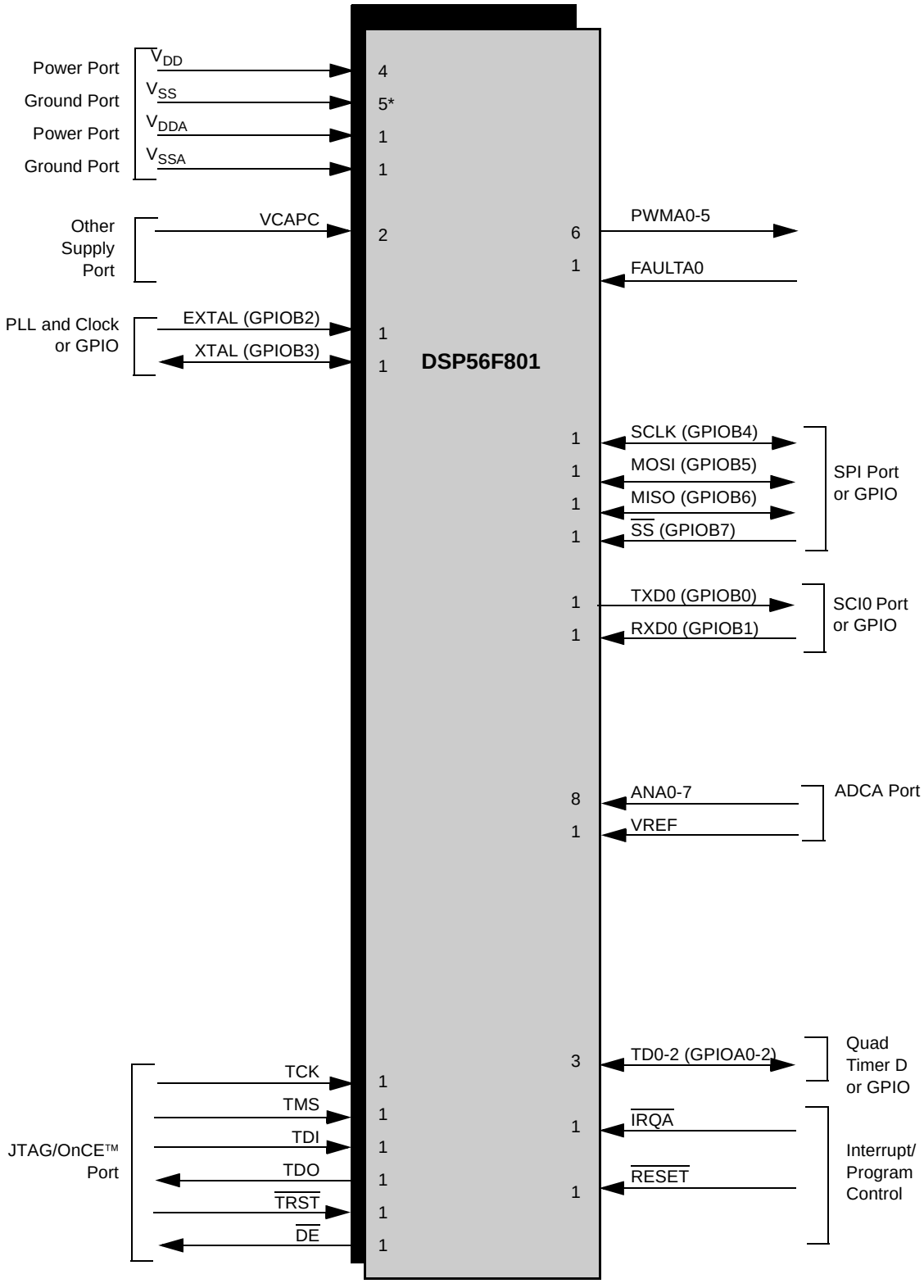
2.1 Introduction

The input and output signals of the DSP56F801 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2**. In **Table 3** through **Table 13**, each table row describes the signal or signals present on a pin.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	5	**Table 3**
Ground (V_{SS} or V_{SSA})	6	**Table 4**
Supply Capacitors	2	**Table 5**
PLL and Clock	2	**Table 6**
Interrupt and Program Control	2	**Table 7**
Pulse Width Modulator (PWM) Port	7	**Table 8**
Serial Peripheral Interface (SPI) Port[1]	4	**Table 9**
Serial Communications Interface (SCI) Port[1]	2	**Table 10**
Analog-to-Digital Converter (ADC) Port	9	**Table 11**
Quad Timer Module Port	3	**Table 12**
JTAG/On-Chip Emulation (OnCE)	6	**Table 13**

1. Alternately, GPIO pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2. DSP56F801 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Power and Ground Signals

Table 3. Power Inputs

No. of Pins	Signal Name	Signal Description
4	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
1	V_{DDA}	**Analog Power**—These pins supply an analog power source.

Table 4. Grounds

No. of Pins	Signal Name	Signal Description
4	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip, and should all be attached to V_{SS}.
1	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 5. Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC** - Connect each pin to a 2.2 µF bypass capacitor in order to bypass the core logic voltage regulator (required for proper chip operation). For more information, refer to **Section 5.2**.

2.3 Clock and Phase Lock Loop Signals

Table 6. PLL and Clock

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**EXTAL**	Input	Input	**External Crystal Oscillator Input**—This input should be connected to an 8 MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**.
	GPIOB2	Input/ Output	Input	**Port B GPIO**—This multiplexed pin is a General Purpose I/O (GPIO) pin that can be programmed as an input or output pin. This I/O can be utilized when using the on-chip relaxation oscillator so the EXTAL pin is not needed.

*includes TCS pin which is reserved for factory use and is tied to VSS

Table 6. PLL and Clock (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**XTAL**	Output	Chip-driven	**Crystal Oscillator Output**—This output should be connected to an 8 MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.5**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.5.3**.
	GPIOB3	Input/ Output	Input	**Port B GPIO**—This multiplexed pin is a General Purpose I/O (GPIO) pin that can be programmed as an input or output pin. This I/O can be utilized when using the on-chip relaxation oscillator so the XTAL pin is not needed.

2.4 Interrupt and Program Control Signals

Table 7. Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{IRQA}}$**	Input	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge- triggered.
1	**$\overline{\text{RESET}}$**	Input	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.

2.5 Pulse Width Modulator (PWM) Signals

Table 8. Pulse Width Modulator (PWMA) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0-5**	Output	Tri- stated	**PWMA0-5**— These are six PWMA output pins.
1	**FAULTA0**	Input	Input	**FAULTA0**— This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off chip.

2.6 Serial Peripheral Interface (SPI) Signals

Table 9. Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOB6	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOB5	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/ Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOB4	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{\text{SS}}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOB7	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{\text{SS}}$.

2.7 Serial Communications Interface (SCI) Signals

Table 10. Serial Communications Interface (SCI0) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—transmit data output
	GPIOB0	Input/ Output	Input	**Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD0**	Input	Input	**Receive Data (RXD0)**—receive data input
	GPIOB1	Input/ Output	Input	**Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI input.

2.8 Analog-to-Digital Converter (ADC) Signals

Table 11. Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0-3**	Input	Input	**ANA0-3**—Analog inputs to ADC channel 1
4	**ANA4-7**	Input	Input	**ANA4-7**—Analog inputs to ADC channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA}-0.3V for optimal performance.

2.9 Quad Timer Module Signals

Table 12. Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
3	**TD0-2**	Input/ Output	Input	**TD0-2**—Timer D Channel 0-2
	GPIOA0-2	Input/ Output	Input	**Port A GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is the quad timer input.

2.10 JTAG/OnCE

Table 13. JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDI**	Input	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The DSP56F801 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 14** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56F801 DC and AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 14. Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Analog inputs ANA0-7 and VREF	V_{IN}	V_{SSA}– 0.3	V_{DDA}+ 0.3	V
Analog inputs EXTAL, XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, & PWM ouputs	I	—	10	mA
Current drain per pin for PWM outputs	I	—	20	mA
Junction temperature	T_J	—	150	°C
Storage temperature range	T_{STG}	-55	150	°C

Table 15. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD},V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C

Table 16. Thermal Characteristics [1]

Characteristic	48-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	46.8	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / \theta_{JA}$	°C

1. See **Section 5.1** for more detail.

3.2 DC Electrical Characteristics

Table 17. DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$–3.6 V, $T_A = -40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	2.5	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups/pulldowns disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups/pulldowns disabled)	I_{IH}	-1	—	1	µA
Typical Pullup or pulldown resistance	R_{PU}, R_{PD}	—	30	—	KΩ
Input/output tri-state current low	I_{OZL}	-10	—	10	µA
Input/output tri-state current low	I_{OZH}	-10	—	10	µA
Output High Voltage (at IOH)	V_{OH}	$V_{DD} - 0.7$	—	—	V
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	—	—	-4	mA
Output Low Current	I_{OL}	—	—	4	mA

Table 17. DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
PWM pin output source current[1]	I_{OHP}	—	—	-10	mA
PWM pin output sink current[2]	I_{OLP}	—	—	16	mA
V_{DD} supply current	I_{DDT}[3]				
Run [4]		—	103	138	mA
Wait[5]		—	72	98	mA
Stop		—	71	97	mA
Low Voltage Interrupt[6]	V_{EI}	2.4	2.7	2.9	V
Power on Reset[7]	V_{POR}	—	1.7	2.0	V

1. PWM pin output source current measured with 50% duty cycle.
2. PWM pin output sink current measured with 50% duty cycle.
3. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for VDD + VDDA)
4. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.
5. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8 MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50 pF on all outputs. C_L = 20 pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.
6. Low voltage interrupt monitors the V_{DD} supply. When V_{DD} drops below V_{EI} value, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EI}$.
7. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.5V typical no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self regulates.

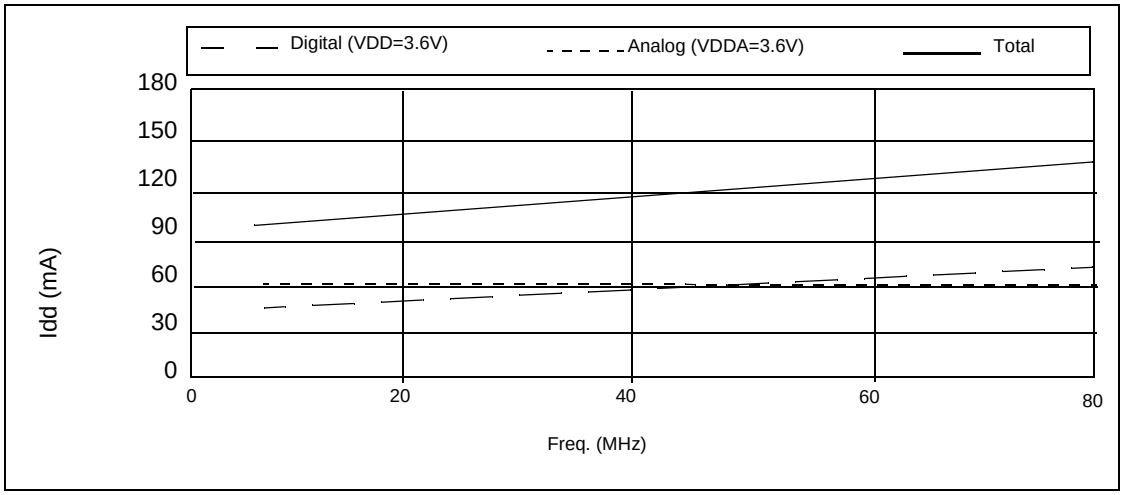
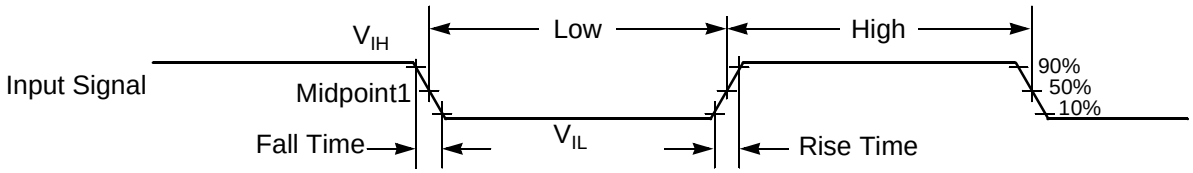


Figure 3. Maximum Run IDD vs. Frequency (see Note 4 above)

3.3 AC Electrical Characteristics

Timing waveforms in **Section 3.3** are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in **Section 3.2**. In **Figure 4** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 4. Input Signal Measurement References

Figure 5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state.
- Tri-stated, when a bus or signal is placed in a high impedance state.
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}.
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}.

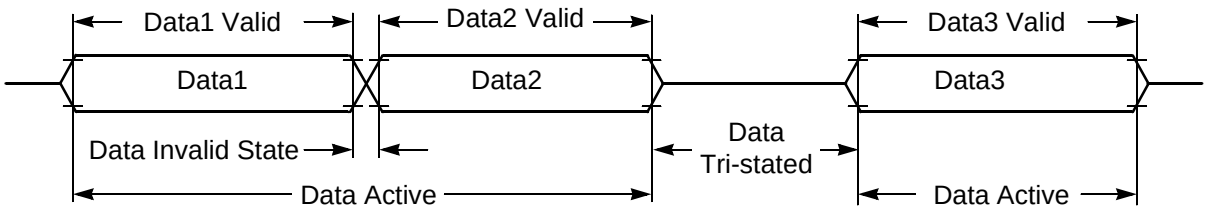


Figure 5. Signal States

3.4 Flash Memory Characteristics

Table 18. Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 19. IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 20. Timing Symbols

Characteristic	Symbol	See Figure(s)
PROG/ERASE to NVSTR set up time	T_{nvs}	Figure 6, Figure 7, Figure 8
NVSTR hold time	T_{nvh}	Figure 6, Figure 7
NVSTR hold time(mass erase)	T_{nvh1}	Figure 8
NVSTR to program set up time	T_{pgs}	Figure 6
Program hold time	T_{pgh}	Figure 6
Address/data set up time	T_{ads}	Figure 6
Address/data hold time	T_{adh}	Figure 6
Recovery time	T_{rcv}	Figure 6, Figure 7, Figure 8
Cumulative program HV period	T_{hv}	Figure 6
Program time	T_{prog}	Figure 6
Erase time	T_{erase}	Figure 7
Mass erase time	T_{me}	Figure 8

Table 21. Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF

Characteristic	Symbol	Min	Typ	Max	Unit
Program time	T_{prog}	20	–	–	us
Erase time	T_{erase}	20	–	–	ms
Mass erase time	T_{me}	100	–	–	ms
Endurance[1]	E_{CYC}	10,000	20,000	–	cycles
Data Retention[1] @ 5000 cycles	D_{RET}	10	30	–	years
PROG/ERASE to NVSTR set up time	T_{nvs}	–	5	–	us

The following parameters should only be used in the Manual Word Programming Mode

NVSTR hold time	T_{nvh}	–	5	–	us
NVSTR hold time (mass erase)	T_{nvh1}	–	100	–	us
NVSTR to program set up time	T_{pgs}	–	10	–	us

Table 21. Flash Timing Parameters (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF

Characteristic	Symbol	Min	Typ	Max	Unit
Recovery time	T_{rcv}	–	1	–	us
Cumulative program HV period[2]	T_{hv}	–	3	–	ms

1. Program specification guaranteed from $T_A = 0$ °C to 85 °C.
2. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.

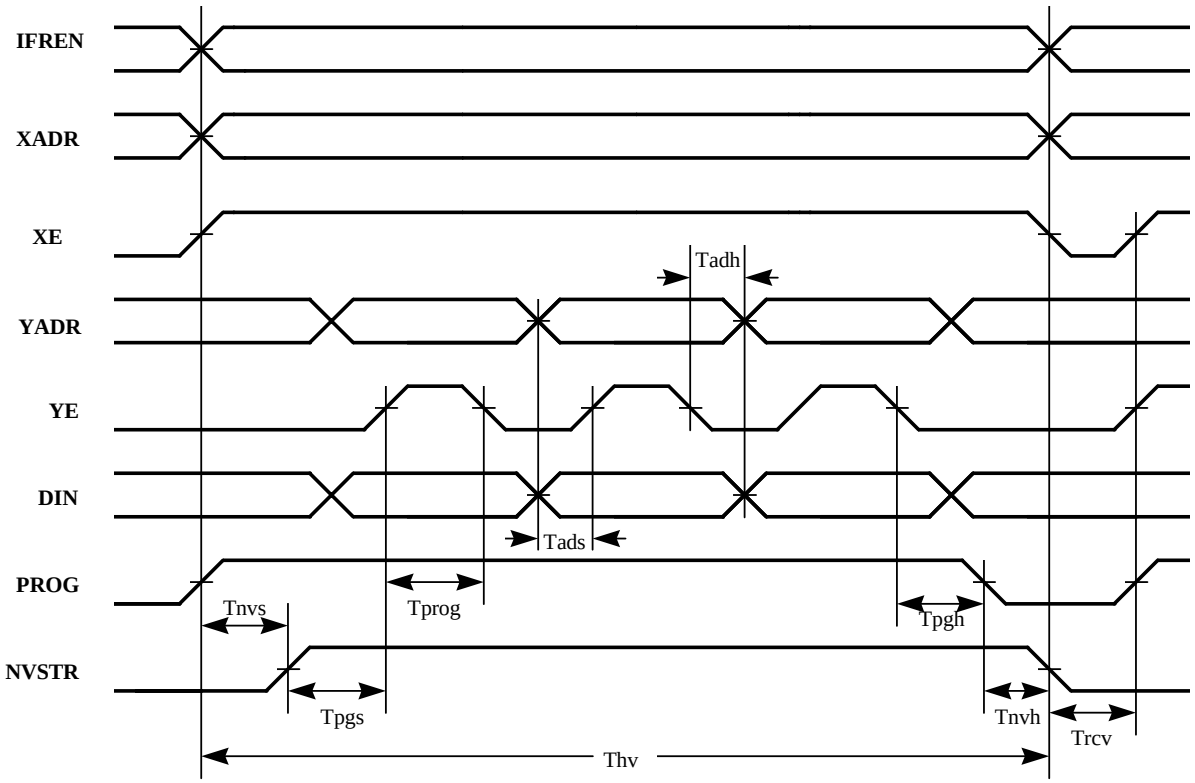


Figure 6. Flash Program Cycle

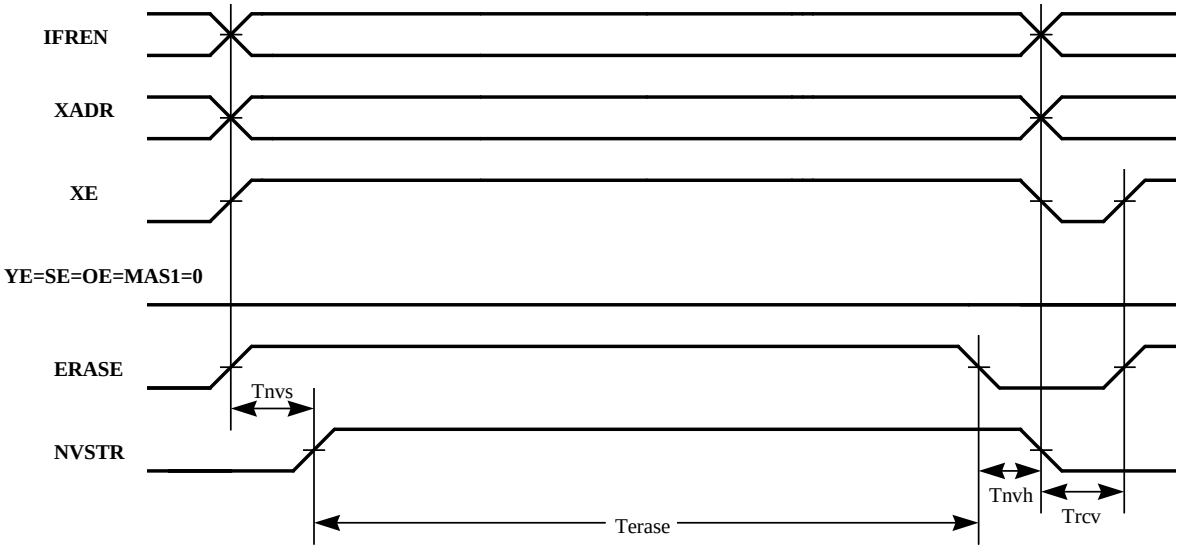


Figure 7. Flash Erase Cycle

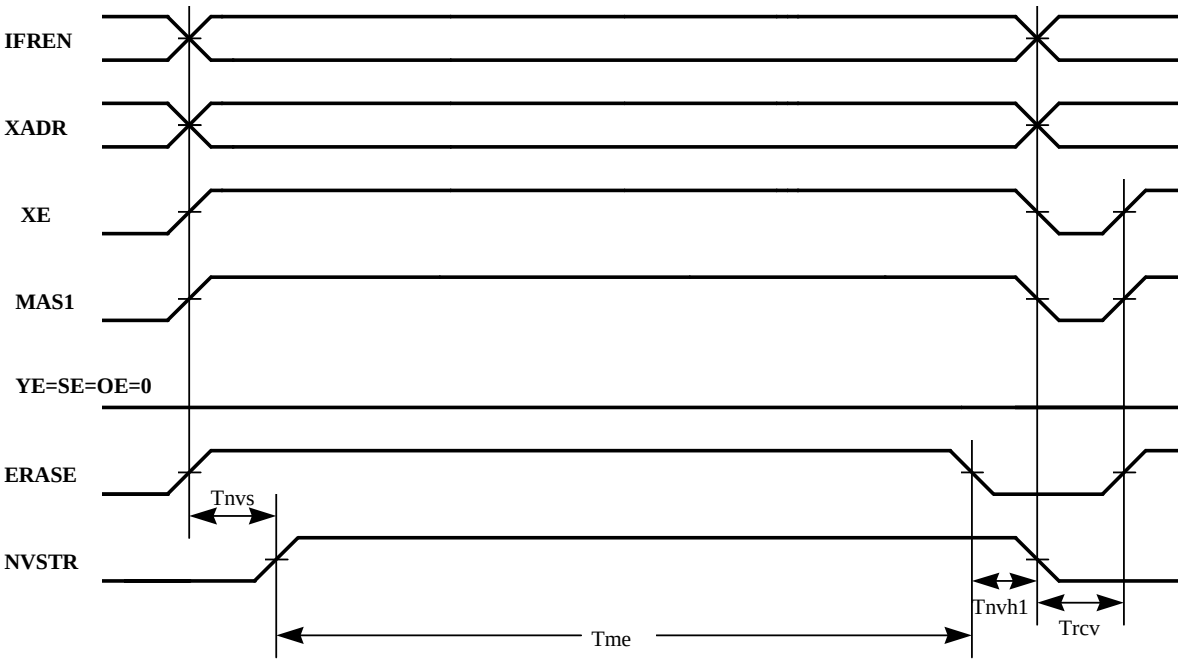


Figure 8. Flash Mass Erase Cycle

3.5 External Clock Operation

The DSP56F801 device clock is derived from either 1) an internal crystal oscillator circuit working in conjunction with an external crystal, 2) an external frequency source, or 3) an on-chip relaxation oscillator. To generate a reference frequency using the internal crystal oscillator circuit, a reference crystal external to the chip must be connected between the EXTAL and XTAL pins. Paragrahs **3.5.1** and **3.5.4** describe these methods of clocking. Whichever type of clock derivation is used provides a reference signal to a phase-locked loop (PLL) within the DSP56F801. In turn, the PLL generates a master reference frequency that determines the speed at which chip operations occur.

Application code can be set to change the frequency source between the relaxation oscillator and crystal oscillator or external source, and power down the relaxation oscillator if desired. Selection of which clock is used is determined by setting the PRECS bit in the PLLCR (phase-locked loop control register) word (bit 2). If the bit is set to 1, the external crystal oscillator circuit is selected. If the bit is set to 0, the internal relaxation oscillator is selected, and this is the default value of the bit when power is first applied.

3.5.1 Crystal Oscillator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal, which is 4-8+ MHz. **Figure 9** shows a typical crystal oscillator circuit. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

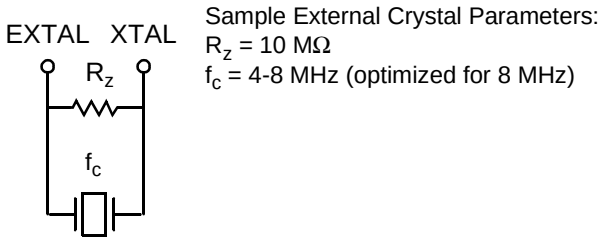


Figure 9. External Crystal Oscillator Circuit

3.5.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. In **Figure 10**, a typical ceramic resonator circuit is shown. Refer to supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins.

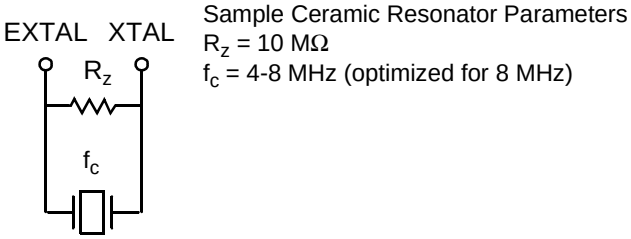


Figure 10. Connecting a Ceramic Resonator

3.5.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 11**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

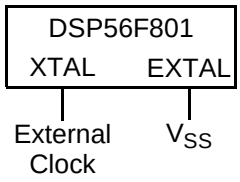


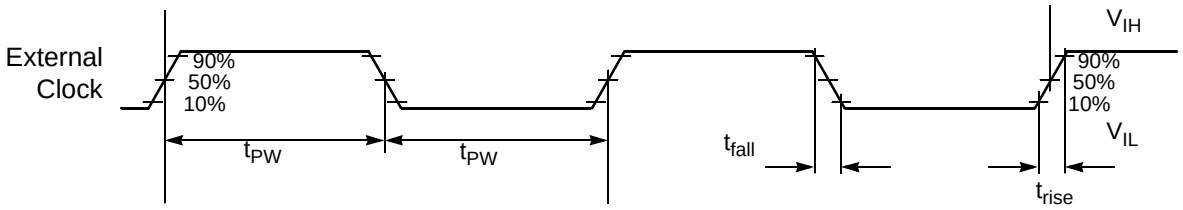
Figure 11. Connecting an External Clock Signal

Table 22. External Clock Operation Timing Requirements[5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	8	110	MHz
Clock Pulse Width[2, 5]	t_{PW}	6.25	—	—	ns
External clock input rise time[3, 5]	t_{rise}	—	—	3	ns
External clock input fall time[4, 5]	t_{fall}	—	—	3	ns

1. See **Figure 11** for details on using the recommended connection of an external clock driver.
2. The high or low pulse width must be no smaller than 6.25 ns or the chip will not function.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.
5. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 12. External Clock Timing

3.5.4 Use of On-Chip Relaxation Oscillator

Table 23. PLL Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	6	8	10	MHz
PLL output frequency[2] ($F_{out}/2$)	f_{op}	40	—	80	MHz
PLL stabilization time [3] 0^o to $+85^oC$	t_{plls}	—	10	—	ms
PLL stabilization time[3] -40^o to 0^oC	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input crystal.
2. ZCLK may not exceed 80 MHz. For additional information on ZCLK and $F_{out}/2$, please refer to the OCCS chapter in the User Manual.
3. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

An internal relaxation oscillator can supply the reference frequency when an external frequency source or crystal are not used. During a DSP56F801 boot or reset sequence, the relaxation oscillator is enabled by default, and the PRECS bit in the PLLCR word is set to 0 (**Section 3.5**). If an external oscillator is connected, the relaxation oscillator can be deselected instead by setting the PRECS bit in the PLLCR to 1. When this occurs, the PRECSS bit in the PLLSR (prescaler clock select status register) data word also sets to 1. If a changeover between internal and external oscillators is required at startup, internal device circuits compensate for any asynchronous transitions between the two clock signals so that no glitches occur in the resulting master clock to the chip. When changing clocks, the user must ensure that the clock source is not switched until the desired clock is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within ±0.25% of 8 MHz by trimming an internal capacitor. Bits 0-7 of the IOSCTL (internal oscillator control) word allow the user to set in an additional offset (trim) to this preset value to increase or decrease capacitance. The default value of this trim is 128 units, making the power-up default capacitor size 432 units. Each unit added or deleted changes the output frequency by about 0.23%, allowing incremental adjustment until the desired frequency accuracy is achieved.

Table 24. Relaxation Oscillator Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Accuracy[1]	Δf	—	± 2	± 5	%
Frequency Drift over Temp	f_T	7	8	9	MHz
Frequency Drift over Supply	$\Delta f/\Delta t$	—	± 0.1	—	$\%/^oC$
Trim Range	$\Delta f/\Delta t$	—	0.1	—	%/V
Trim Accuracy	Δf_T	—	± 0.25	—	%

1. Over full temperature range.

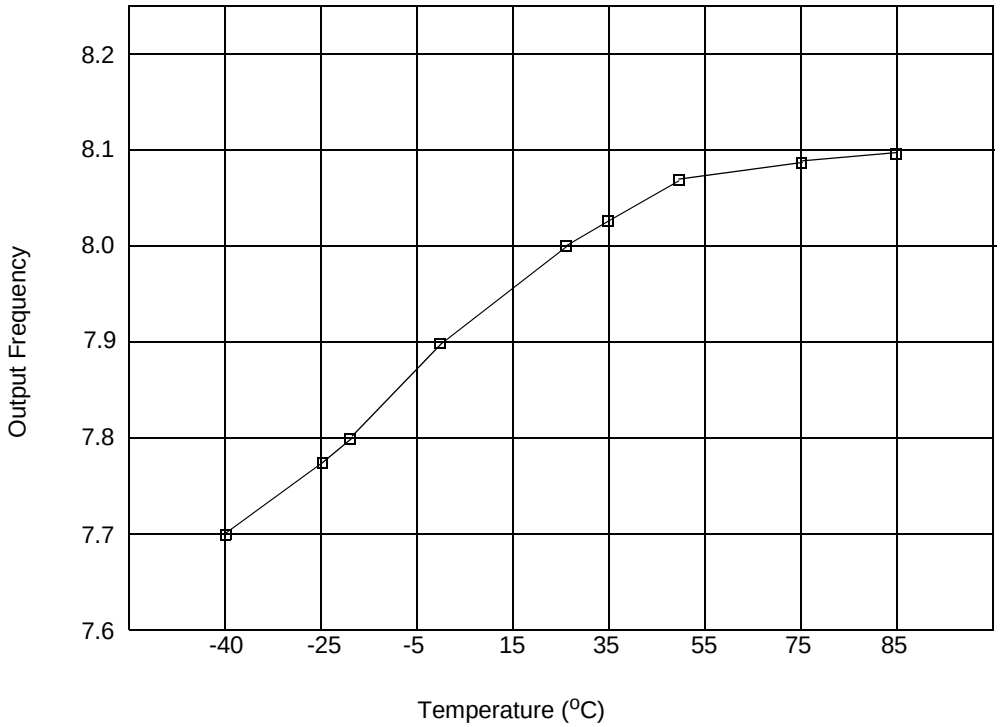


Figure 13. Typical Relaxation Oscillator Frequency vs. Temperature (Trimmed to 8MHz @ 25°C)

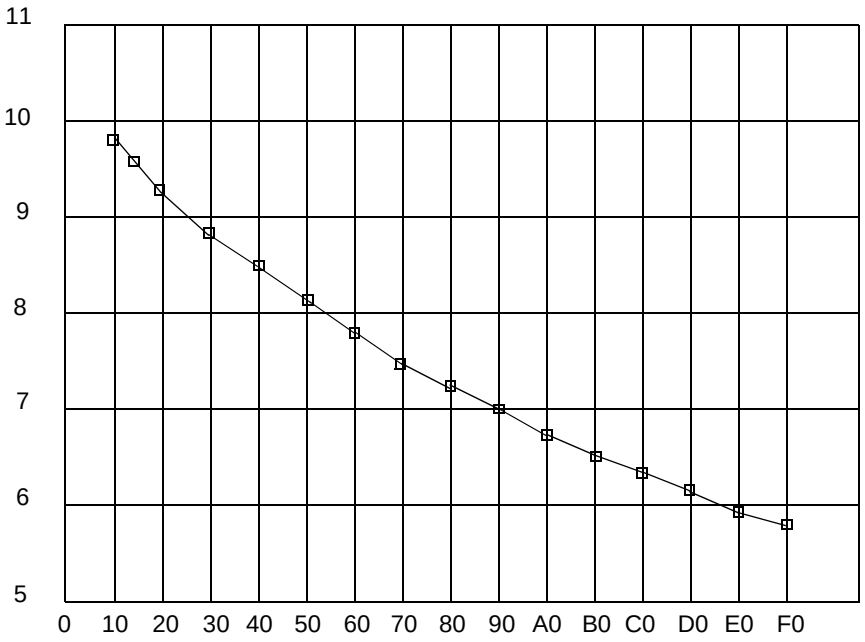


Figure 14. Typical Relaxation Oscillator Frequency vs. Trim Value @ 25°C

3.6 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 25. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF

Characteristic	Symbol	Typical Min	Typical Max	Unit	See
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 15
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 15
$\overline{\text{RESET}}$ De-assertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 15
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 16
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	—	15T	ns	Figure 17
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	—	16T	ns	Figure 17
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	—	13T	ns	Figure 18
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	—	2T	ns	Figure 19
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 19
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 20
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 20

1. In the formulas, T = clock cycle. For an operating frequency of 80 MHz, T = 12.5 ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   • After power-on reset
   • When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. Parameters listed are guaranteed by design.

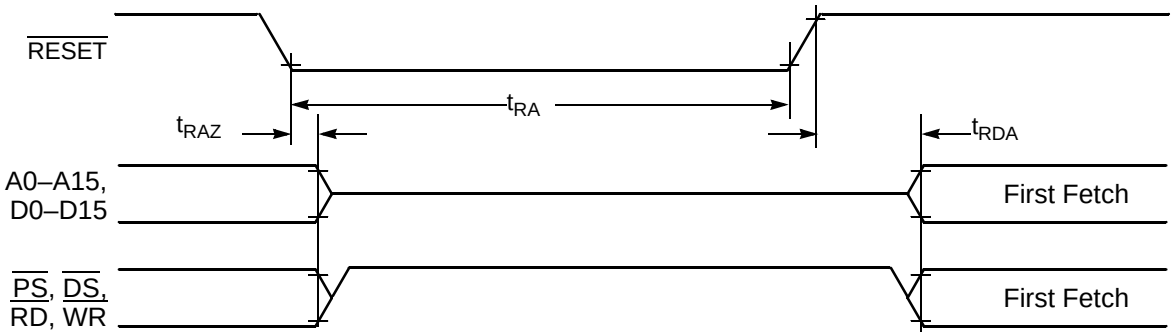


Figure 15. Asynchronous Reset Timing

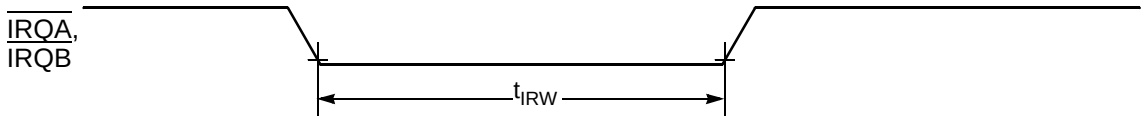


Figure 16. External Interrupt Timing (Negative-Edge-Sensitive)

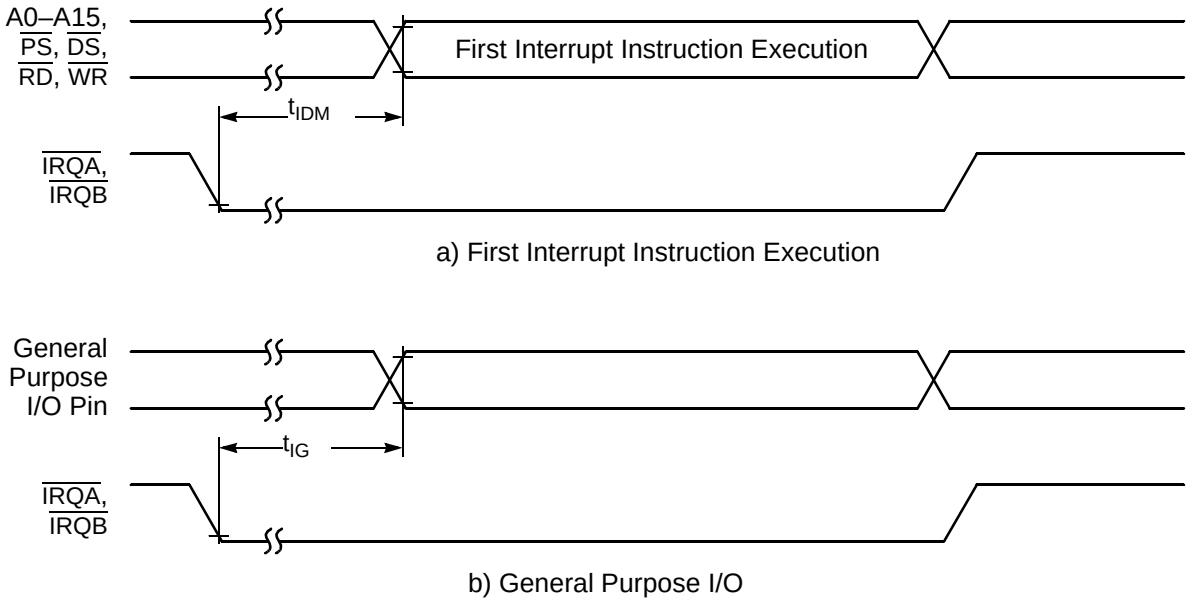


Figure 17. External Level-Sensitive Interrupt Timing

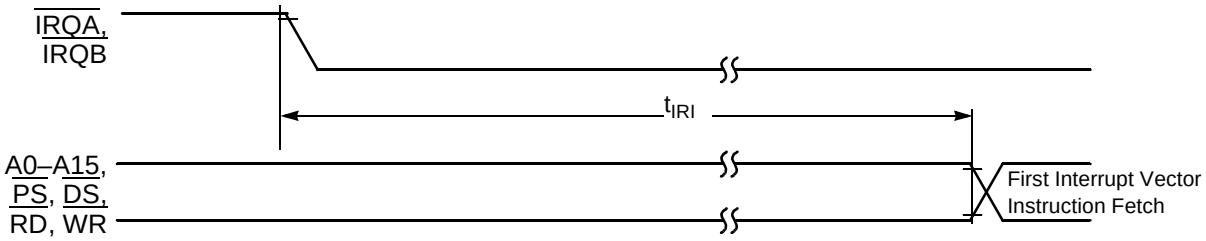


Figure 18. Interrupt from Wait State Timing

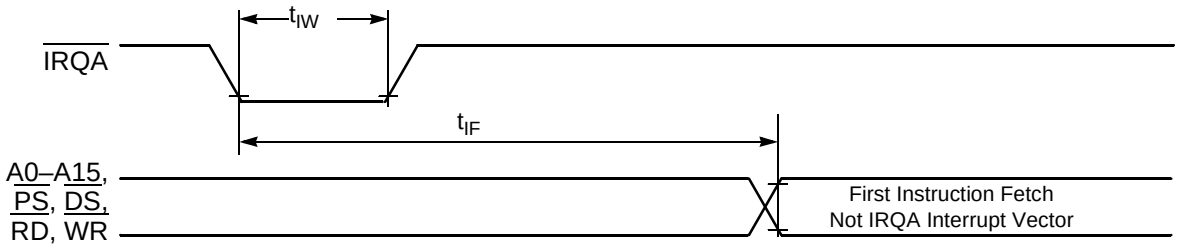


Figure 19. Recovery from Stop State Using Asynchronous Interrupt Timing

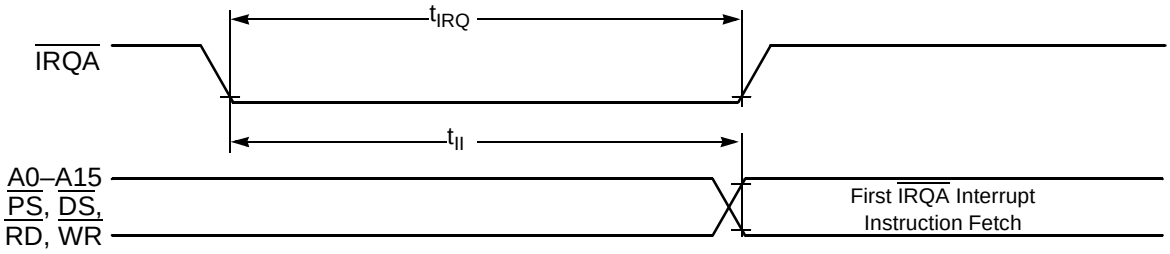


Figure 20. Recovery from Stop State Using IRQA Interrupt Service

3.7 Serial Peripheral Interface (SPI) Timing

Table 26. SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 21, 22, 23, 24
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 24
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 24
Clock (SCK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	Figures 21, 22, 23, 24
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figures 21, 22, 23, 24
Data setup time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 21, 22, 23, 24
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 21, 22, 23, 24
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 24
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 24
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 21, 22, 23, 24
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 21, 22, 23, 24
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 21, 22, 23, 24
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 21, 22, 23, 24

1. Parameters listed are guaranteed by design.

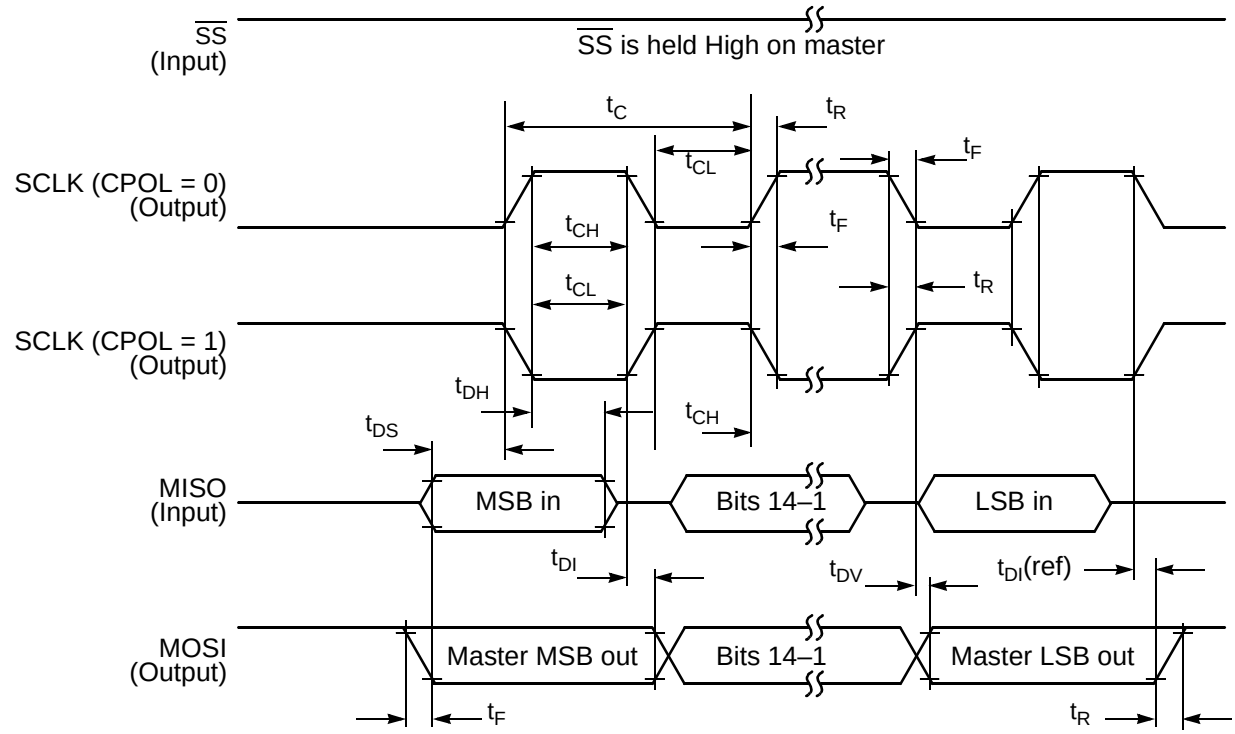


Figure 21. SPI Master Timing (CPHA = 0)

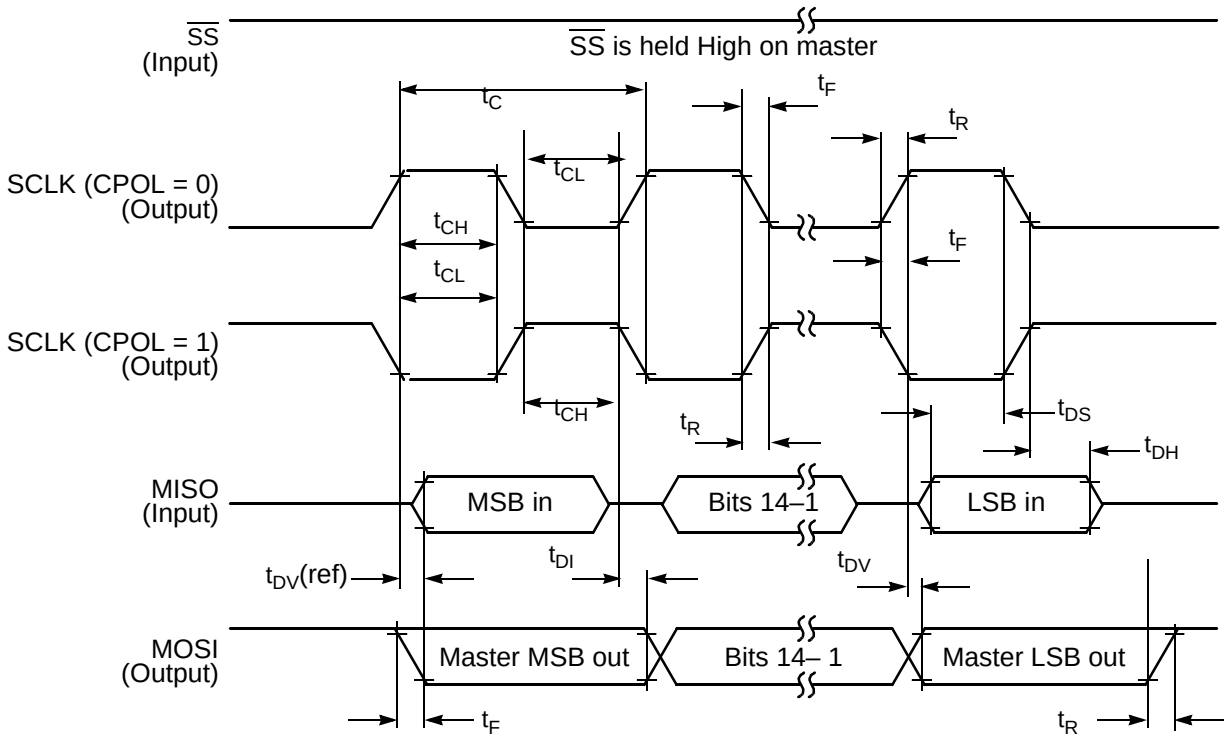


Figure 22. SPI Master Timing (CPHA = 1)

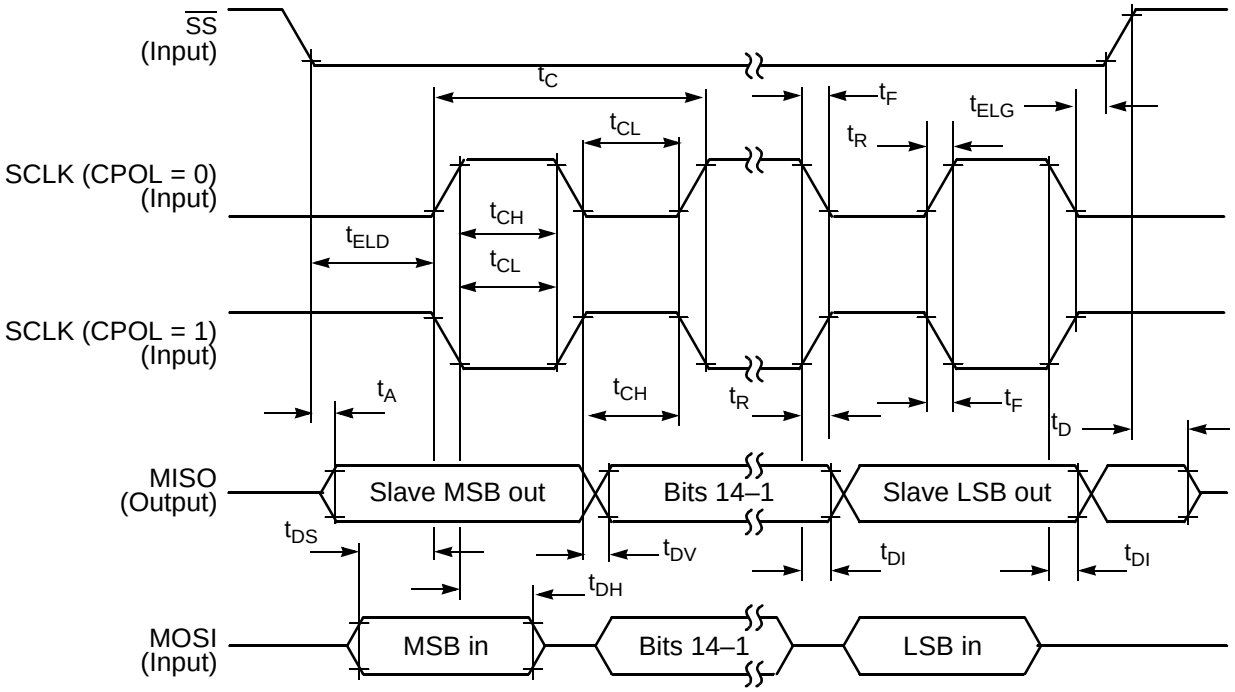


Figure 23. SPI Slave Timing (CPHA = 0)

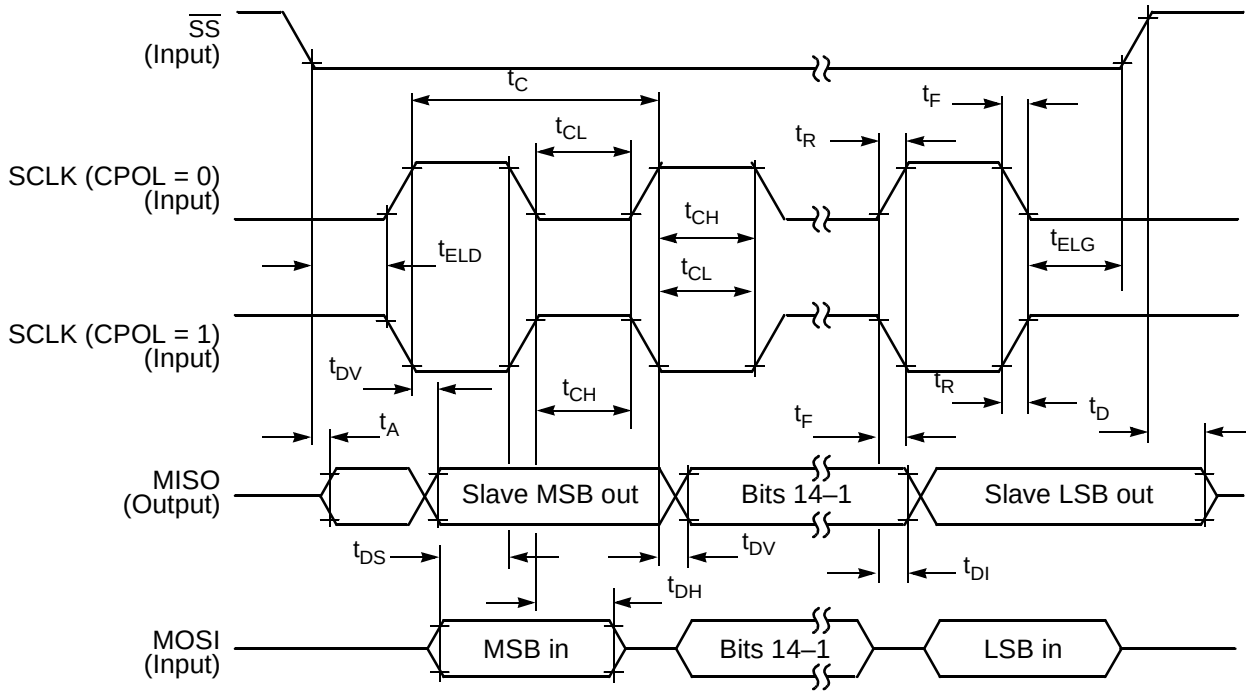


Figure 24. SPI Slave Timing (CPHA = 1)

3.8 Quad Timer Timing

Table 27. Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Typical Min	Typical Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T	—	ns
Timer output high/low period	P_{OUTHL}	1T	—	ns

1. In the formulas listed, T = clock cycle. For 80 MHz operation, T = 12.5 ns.
2. Parameters listed are guaranteed by design.

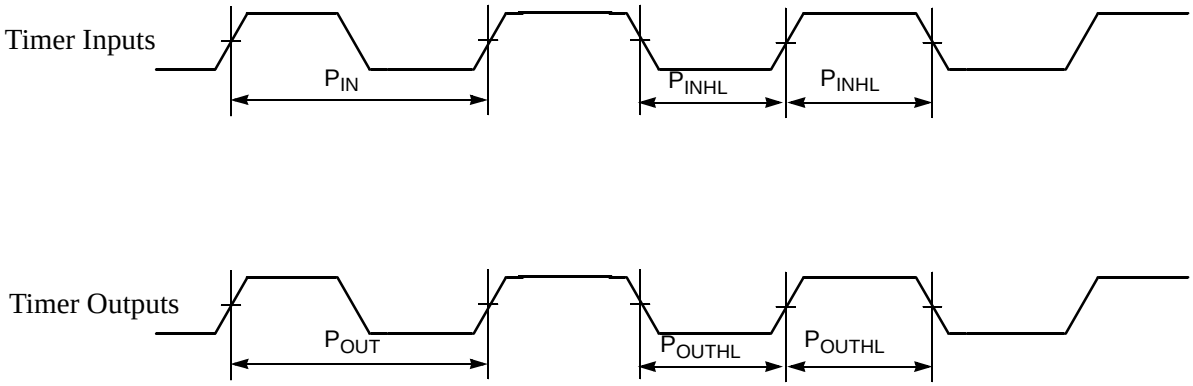


Figure 25. Timer Timing

3.9 Serial Communication Interface (SCI) Timing

Table 28. SCI Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

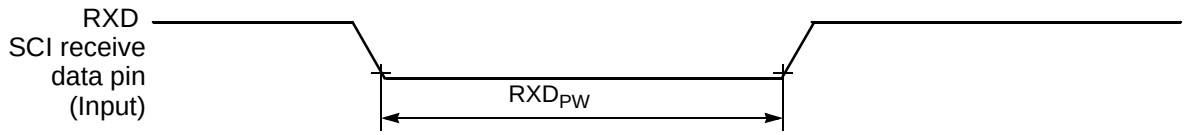


Figure 26. RXD Pulse Width

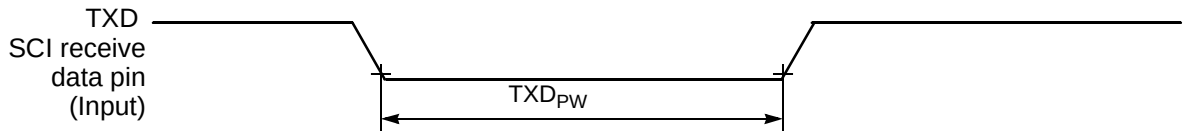


Figure 27. TXD Pulse Width

3.10 Analog-to-Digital Converter (ADC) Characteristics

Table 29. ADC Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $V_{REF} = V_{DD}$-0.3V, ADCDIV = 4, 9, or 14, ADC clock = 4MHz, 3.0–3.6 V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	0	—	V_{DDA}[1]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[2]	INL	—	+/- 4	+/- 5	LSB[3]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[3]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[4]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[4]
Input capacitance	C_{ADI}	—	5	—	pF[4]
Gain Error (transfer gain)	E_{GAIN}	1.00	1.10	1.15	—
Offset Voltage	V_{OFFSET}	+10	+230	+325	mV
Total Harmonic Distortion	THD	55	60	—	dB
Signal-to-Noise plus Distortion	SINAD	54	56	—	dB
Effective Number of Bits	ENOB	8.5	9.5	—	bit
Spurious Free Dynamic Range	SFDR	60	65	—	dB

Table 29. ADC Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $V_{REF} = V_{DD}$-0.3V, ADCDIV = 4, 9, or 14, ADC clock = 4MHz, 3.0–3.6 V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	—	100	—	KHz
ADC Quiescent Current (both ADCs)	I_{ADC}	—	39.3	—	mA
V_{REF} Quiescent Current (both ADCs)	I_{VREF}	—	11.85	14.5	mA

1. V_{DDA} should be tied to the same potential as V_{DD} via separate traces. V_{REF} must be equal to or less than V_{DD} and must be greater than or equal to 2.7V.
2. Measured in 10-90% range.
3. LSB = Least Significant Bit.

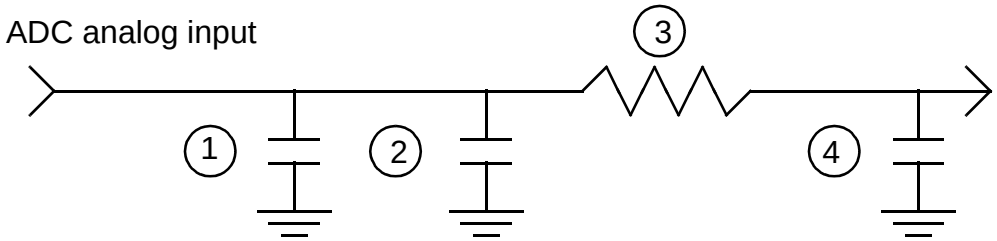


Figure 28. Equivalent Analog Input Circuit

1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. 500 ohms

Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. 1pf

3.11 JTAG Timing

Table 30. JTAG Timing [1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data setup time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	8T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80 MHz operation, T = 12.5 ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

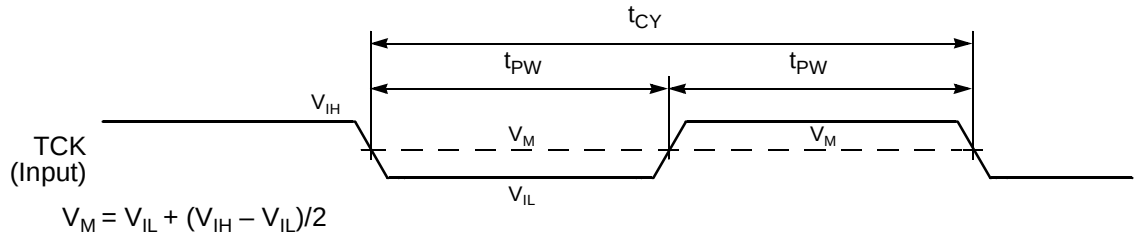


Figure 29. Test Clock Input Timing Diagram

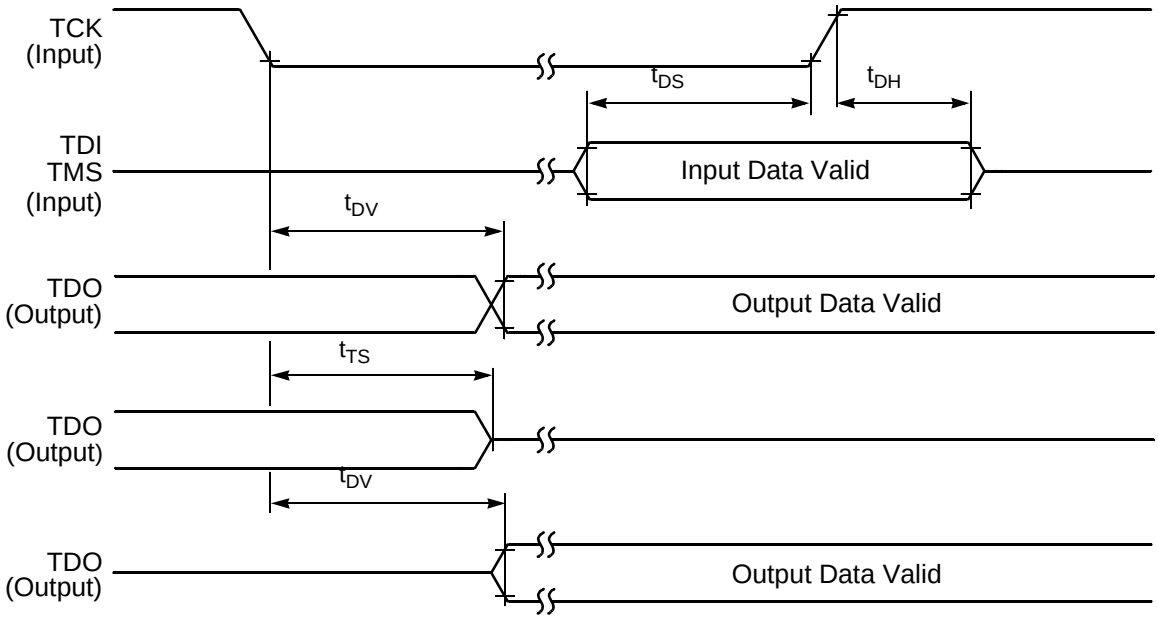


Figure 30. Test Access Port Timing Diagram

Figure 31. $\overline{\text{TRST}}$ Timing Diagram

Figure 32. OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information DSP56F801

This section contains package and pin-out information for the 48-pin LQFP configuration of the DSP56F801.

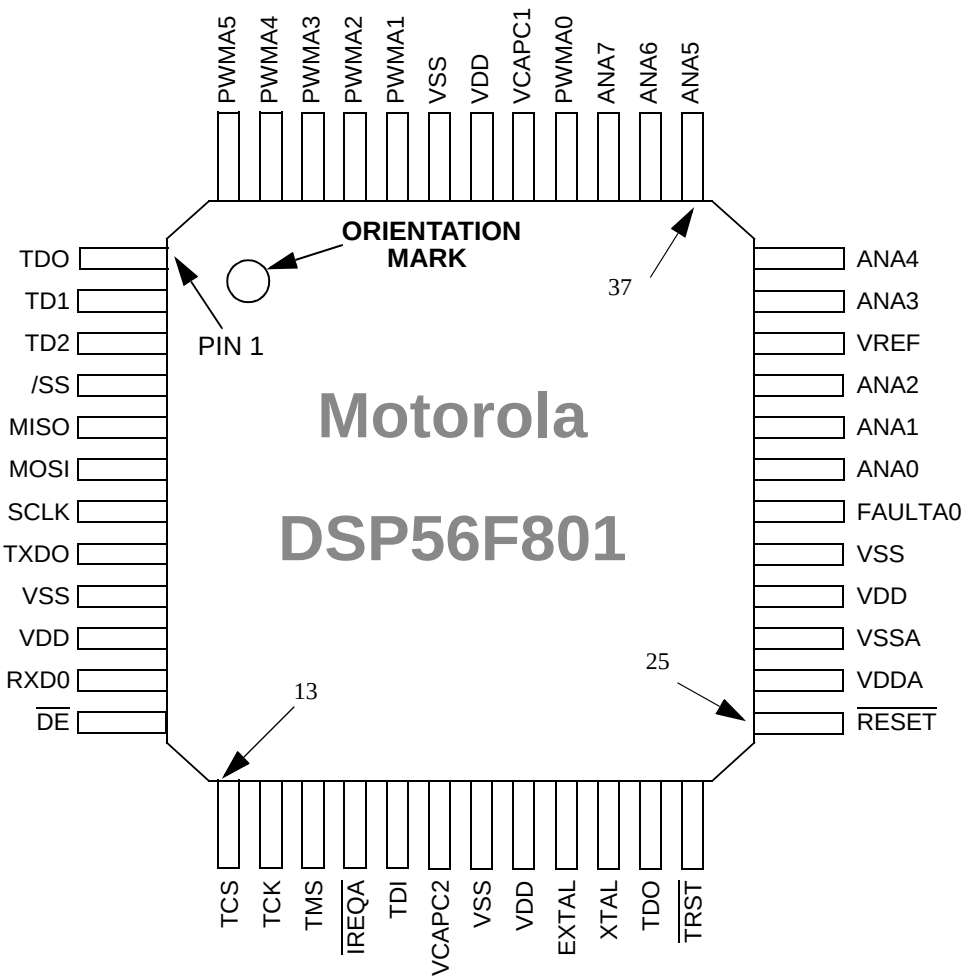
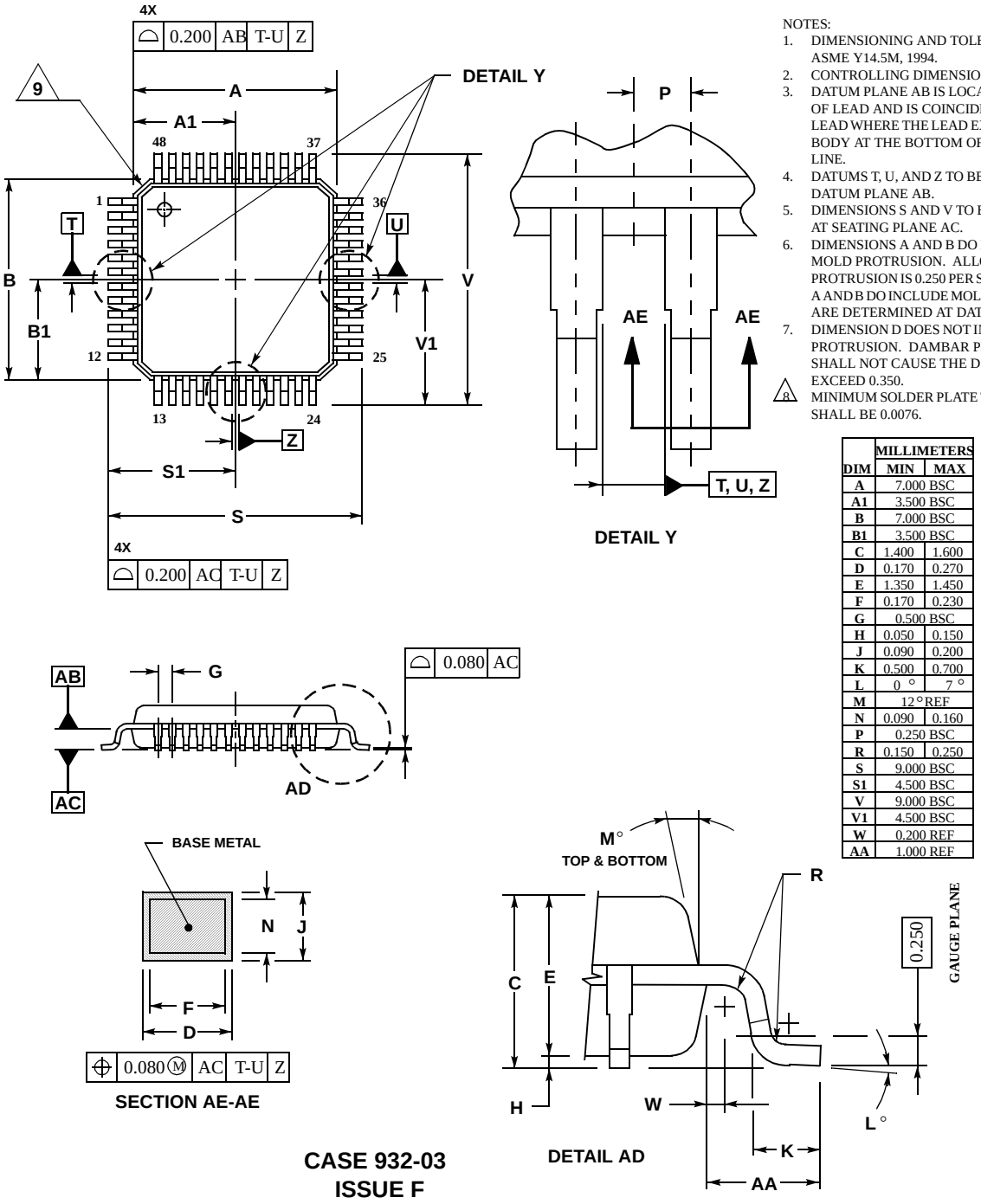


Figure 33. Top View, DSP56F801 48-pin LQFP Package

Table 31. DSP56F801 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TD0	13	TCS	25	$\overline{\text{RESET}}$	37	ANA5
2	TD1	14	TCK	26	V_{DDA}	38	ANA6
3	TD2	15	TMS	27	V_{SSA}	39	ANA7
4	$\overline{\text{SS}}$	16	$\overline{\text{IREQA}}$	28	V_{DD}	40	PWMA0
5	MISO	17	TDI	29	V_{SS}	41	VCAPC1
6	MOSI	18	VCAPC2	30	FAULTA0	42	V_{DD}
7	SCLK	19	V_{SS}	31	ANA0	43	V_{SS}
8	TXD0	20	V_{DD}	32	ANA1	44	PWMA1
9	V_{SS}	21	EXTAL	33	ANA2	45	PWMA2
10	V_{DD}	22	XTAL	34	VREF	46	PWMA3
11	RXD0	23	TDO	35	ANA3	47	PWMA4
12	$\overline{\text{DE}}$	24	$\overline{\text{TRST}}$	36	ANA4	48	PWMA5



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12 °REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

Figure 34. 48-pin LQFP Mechanical Information

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.

- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The junction-to-case thermal resistances quoted in this data sheet are determined using the first definition on page 45. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ The VCAP capacitors must be 150 milliohm or less ESR capacitors.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.

- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 32 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 32. DSP56F801 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56F801	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	48	80	DSP56F801FA80

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

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