DTC114EET1 Series

Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC−75/SOT−416 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC−75/SOT−416 Package Can be Soldered Using Wave or Reflow
- The Modified Gull−Winged Leads Absorb Thermal Stress During Soldering Eliminating the Possibility of Damage to the Die
- Available in 8 mm, 7 inch/3000 Unit Tape & Reel
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Total Device Dissipation, FR−4 Board (Note 1) @ T_A = 25°C Derate above 25°C	P_D	200 1.6	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR−4 Board (Note 2) @ T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 × 1.0 Inch Pad

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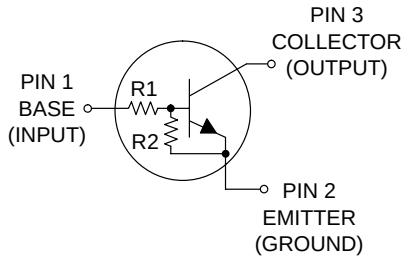
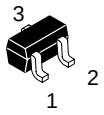
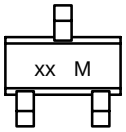
NPN SILICON BIAS RESISTOR TRANSISTORS



MARKING DIAGRAM



SC−75/SOT−416
CASE 463
STYLE 1



xx = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.

ORDERING INFORMATION, DEVICE MARKING and RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
DTC114EET1	8A	10	10	SC−75/SOT−416	3000 Tape & Reel
DTC114EET1G	8A	10	10	SC−75/SOT−416 (Pb−Free)	
DTC124EET1	8B	22	22	SC−75/SOT−416	
DTC124EET1G	8B	22	22	SC−75/SOT−416 (Pb−Free)	
DTC144EET1	8C	47	47	SC−75/SOT−416	
DTC144EET1G	8C	47	47	SC−75/SOT−416 (Pb−Free)	
DTC114YET1	8D	10	47	SC−75/SOT−416	
DTC114YET1G	8D	10	47	SC−75/SOT−416 (Pb−Free)	
DTC114TET1	94	10	∞	SC−75/SOT−416	
DTC114TET1G	94	10	∞	SC−75/SOT−416 (Pb−Free)	
DTC143TET1	8F	4.7	∞	SC−75/SOT−416	
DTC143TET1G	8F	4.7	∞	SC−75/SOT−416 (Pb−Free)	
DTC123EET1	8H	2.2	2.2	SC−75/SOT−416	
DTC123EET1G	8H	2.2	2.2	SC−75/SOT−416 (Pb−Free)	
DTC143EET1	8J	4.7	4.7	SC−75/SOT−416	
DTC143EET1G	8J	4.7	4.7	SC−75/SOT−416 (Pb−Free)	
DTC143ZET1	8K	4.7	47	SC−75/SOT−416	
DTC143ZET1G	8K	4.7	47	SC−75/SOT−416 (Pb−Free)	
DTC124XET1	8L	22	47	SC−75/SOT−416	
DTC124XET1G	8L	22	47	SC−75/SOT−416 (Pb−Free)	
DTC123JET1	8M	2.2	47	SC−75/SOT−416	
DTC123JET1G	8M	2.2	47	SC−75/SOT−416 (Pb−Free)	
DTC115EET1	8N	100	100	SC−75/SOT−416	
DTC115EET1G	8N	100	100	SC−75/SOT−416 (Pb−Free)	
DTC144WET1	8P	47	22	SC−75/SOT−416	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current	DTC114EET1	I_{EBO}	−	−	0.5	mAdc
(V_{EB} = 6.0 V, I_C = 0)	DTC124EET1		−	−	0.2	
	DTC144EET1		−	−	0.1	
	DTC114YET1		−	−	0.2	
	DTC114TET1		−	−	0.9	
	DTC143TET1		−	−	1.9	
	DTC123EET1		−	−	2.3	
	DTC143EET1		−	−	1.5	
	DTC143ZET1		−	−	0.18	
	DTC124XET1		−	−	0.13	
	DTC123JET1		−	−	0.2	
	DTC115EET1		−	−	0.05	
	DTC144WET1		−	−	0.13	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain	DTC114EET1	h_{FE}	35	60	−	
(V_{CE} = 10 V, I_C = 5.0 mA)	DTC124EET1		60	100	−	
	DTC144EET1		80	140	−	
	DTC114YET1		80	140	−	
	DTC114TET1		160	350	−	
	DTC143TET1		160	350	−	
	DTC123EET1		8.0	15	−	
	DTC143EET1		15	30	−	
	DTC143ZET1		80	200	−	
	DTC124XET1		80	150	−	
	DTC123JET1		80	140	−	
	DTC115EET1		80	150	−	
	DTC144WET1		80	140	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 5 mA) DTC123EET1 (I_C = 10 mA, I_B = 1 mA) DTC143TET1/DTC114TET1/ DTC143EET1/DTC143ZET1/DTC124XET1		$V_{CE(sat)}$	−	−	0.25	Vdc
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	DTC114EET1		−	−	0.2	
	DTC124EET1		−	−	0.2	
	DTC114YET1		−	−	0.2	
	DTC114TET1		−	−	0.2	
	DTC143TET1		−	−	0.2	
	DTC123EET1		−	−	0.2	
	DTC143EET1		−	−	0.2	
	DTC143ZET1		−	−	0.2	
	DTC124XET1		−	−	0.2	
	DTC123JET1		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	DTC144EET1		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	DTC115EET1		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	DTC144WET1		−	−	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	−	−	Vdc
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	DTC143TET1					
	DTC143ZET1					
	DTC114TET1					

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Resistor	TC114EET1	R1	7.0	10	13	kΩ
	DTC124EET1		15.4	22	28.6	
	DTC144EET1		32.9	47	61.1	
	DTC114YET1		7.0	10	13	
	DTC114TET1		7.0	10	13	
	DTC143TET1		3.3	4.7	6.1	
	DTC123EET1		1.5	2.2	2.9	
	DTC143EET1		3.3	4.7	6.1	
	DTC143ZET1		3.3	4.7	6.1	
	DTC124XET1		15.4	22	28.6	
	DTC123JET1		1.54	2.2	2.86	
	DTC115EET1		70	100	130	
	DTC144WET1		32.9	47	61.1	
Resistor Ratio	DTC114EET1/DTC124EET1/DTC144EET1/	R_1/R_2				
	DTC115EET1		0.8	1.0	1.2	
	DTC114YET1		0.17	0.21	0.25	
	DTC143TET1/DTC114TET1		–	–	–	
	DTC123EET1/DTC143EET1		0.8	1.0	1.2	
	DTC143ZET1		0.055	0.1	0.185	
	DTC124XET1		0.38	0.47	0.56	
	DTC123JET1		0.038	0.047	0.056	
	DTC144WET1D		1.7	2.1	2.6	

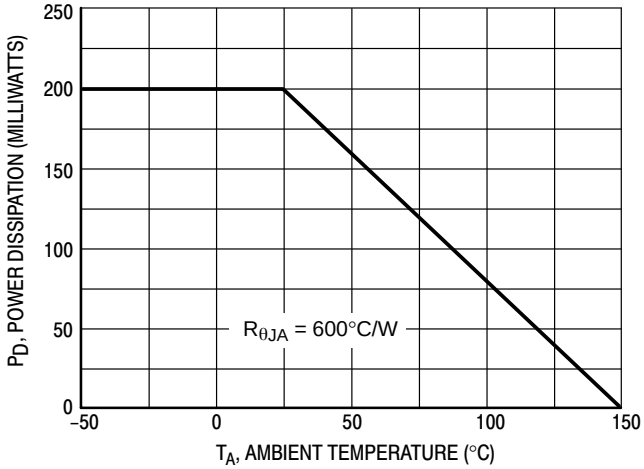


Figure 1. Derating Curve

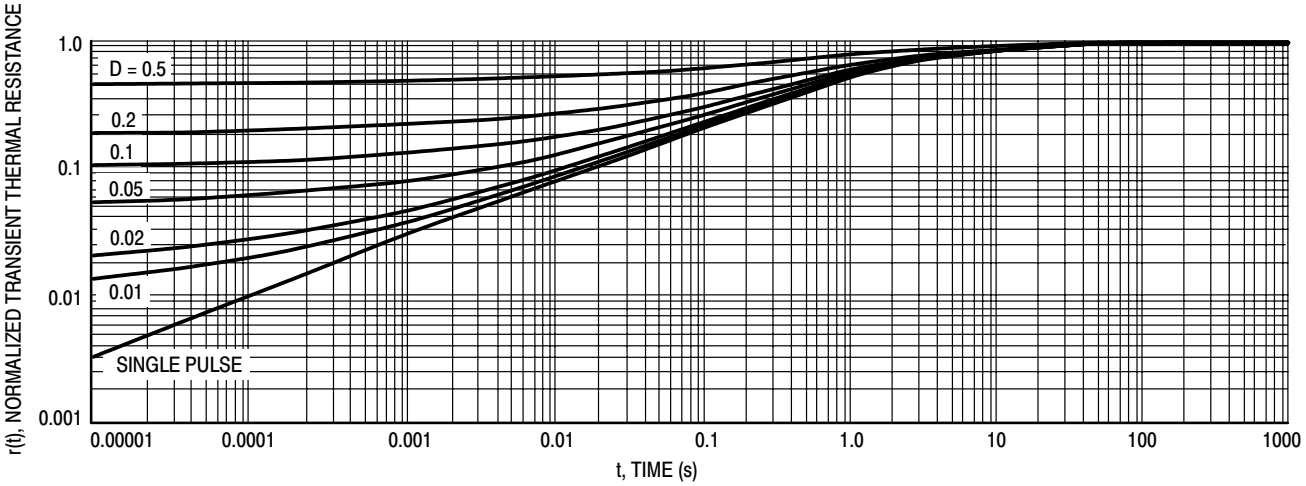


Figure 2. Normalized Thermal Response

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114EET1

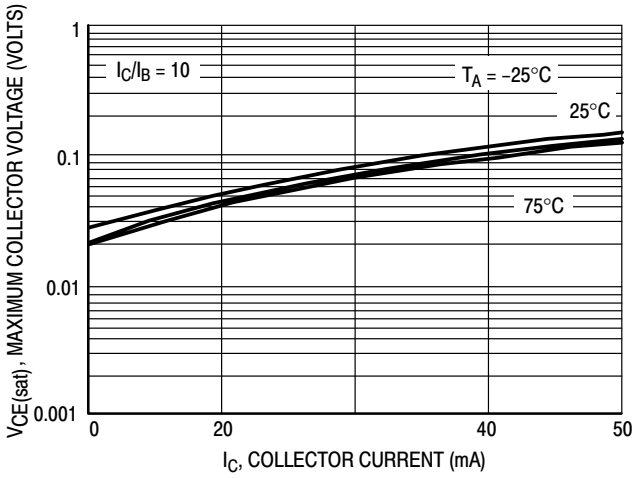


Figure 3. $V_{CE(sat)}$ versus I_C

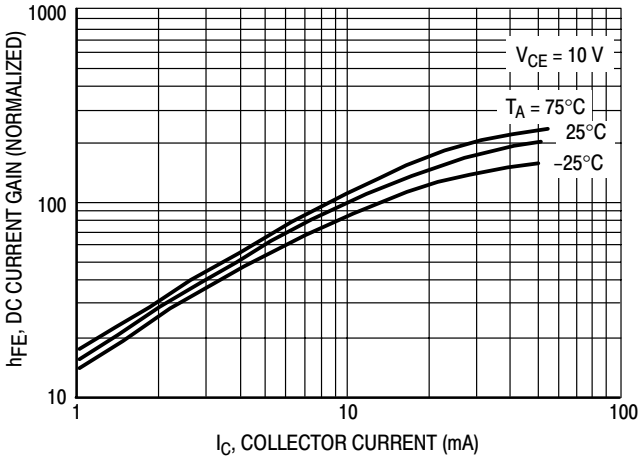


Figure 4. DC Current Gain

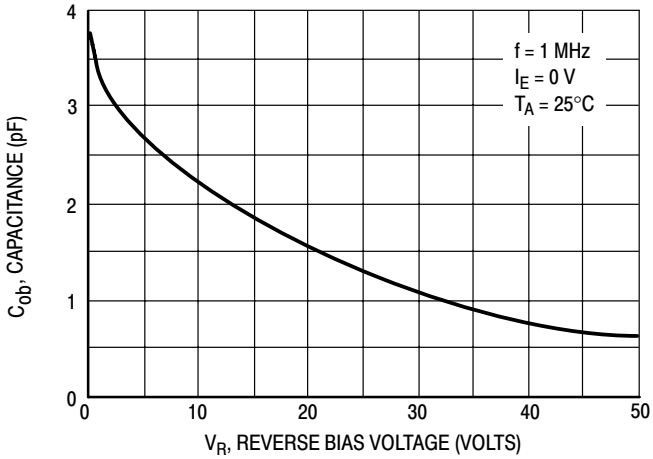


Figure 5. Output Capacitance

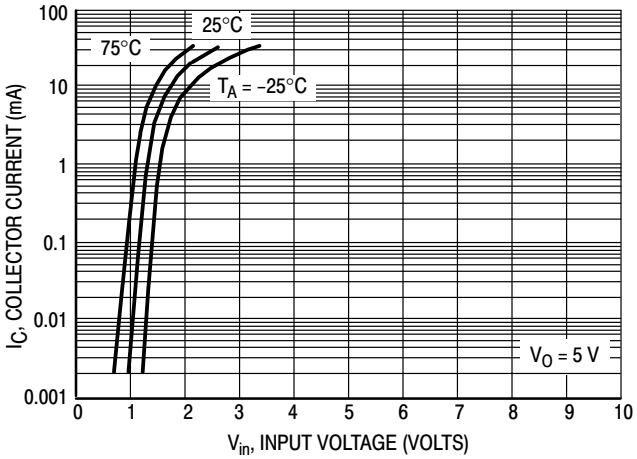


Figure 6. Output Current versus Input Voltage

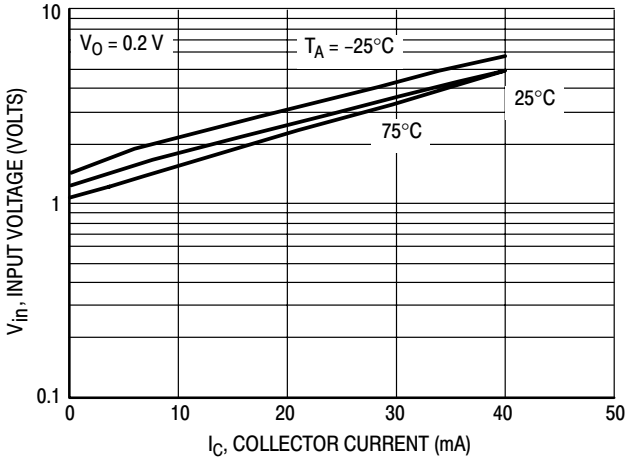


Figure 7. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC124EET1

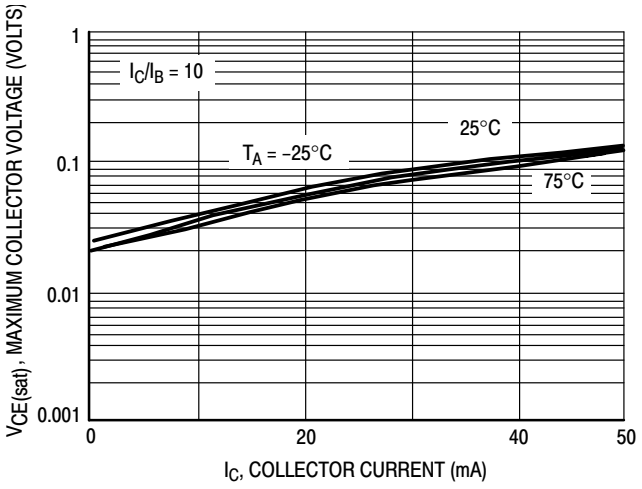


Figure 8. $V_{CE(sat)}$ versus I_C

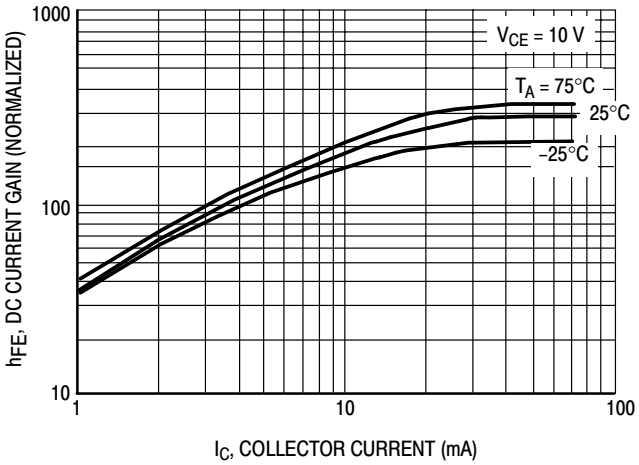


Figure 9. DC Current Gain

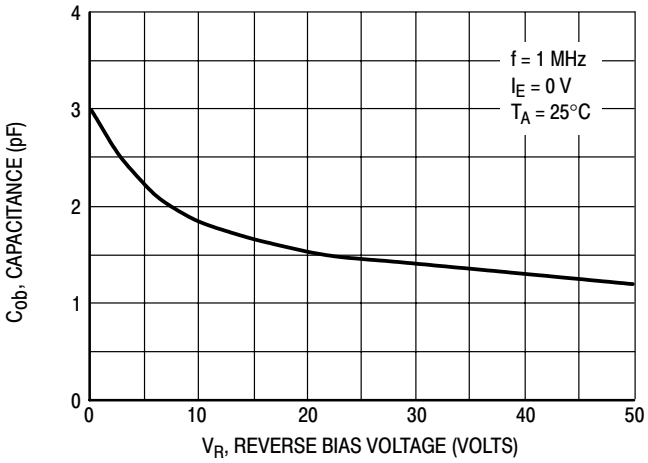


Figure 10. Output Capacitance

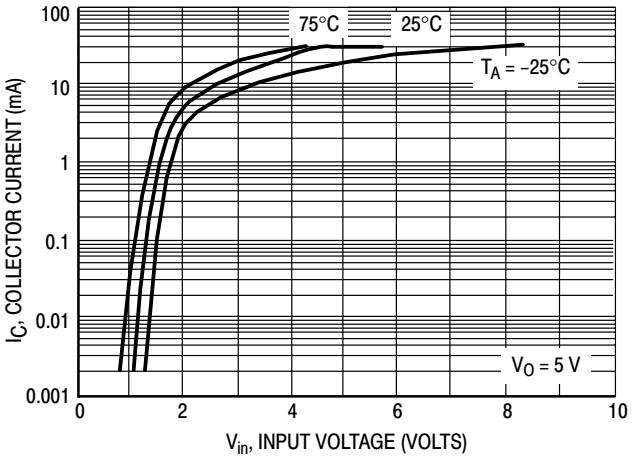


Figure 11. Output Current versus Input Voltage

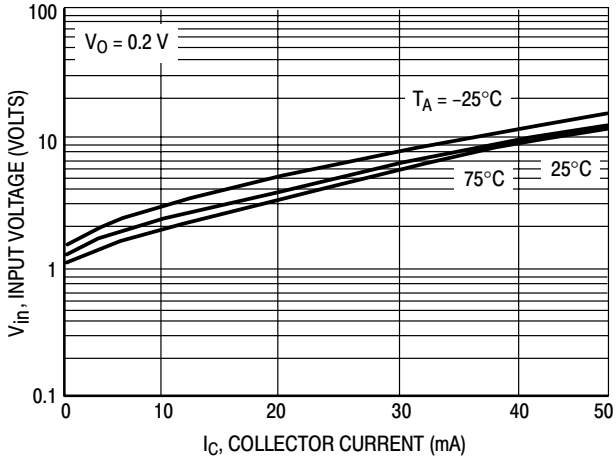


Figure 12. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC144EET1

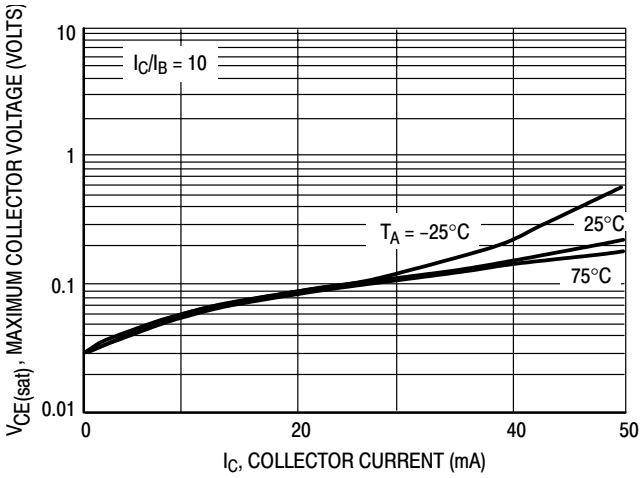


Figure 13. $V_{CE(sat)}$ versus I_C

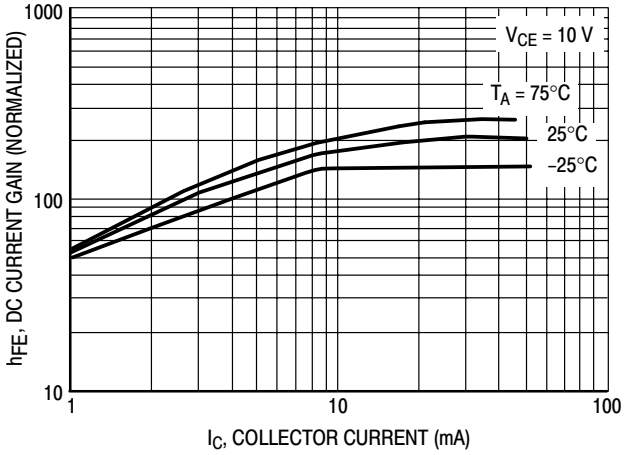


Figure 14. DC Current Gain

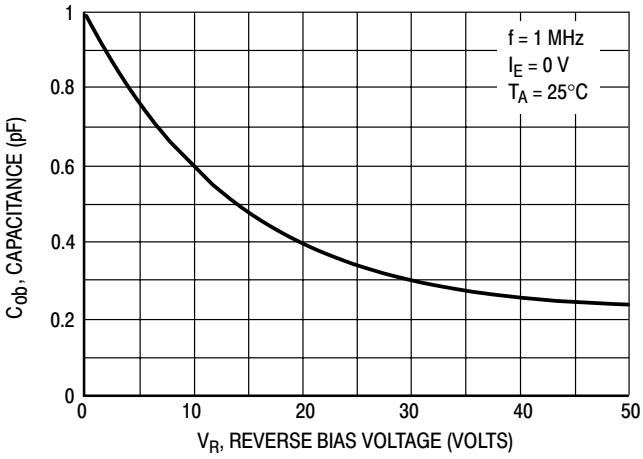


Figure 15. Output Capacitance

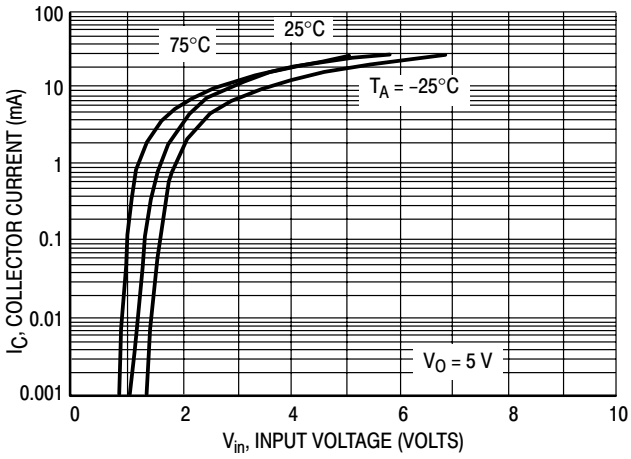


Figure 16. Output Current versus Input Voltage

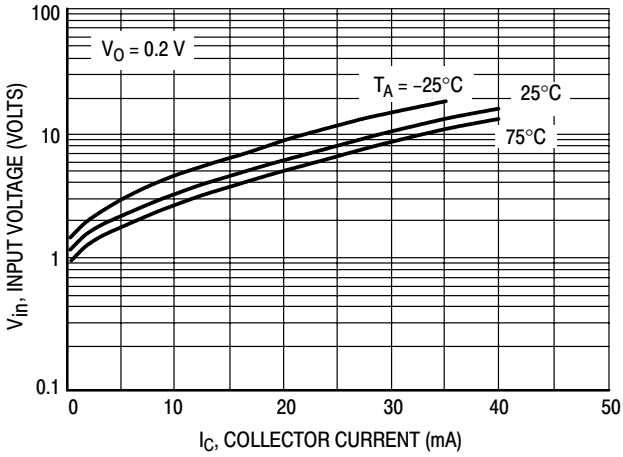


Figure 17. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114YET1

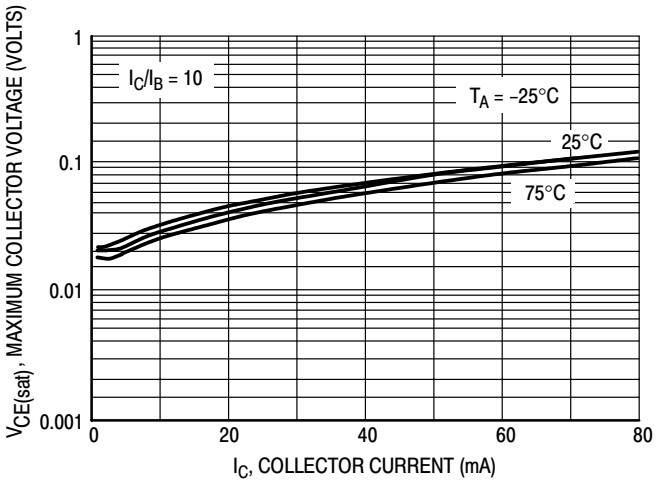


Figure 18. $V_{CE(sat)}$ versus I_C

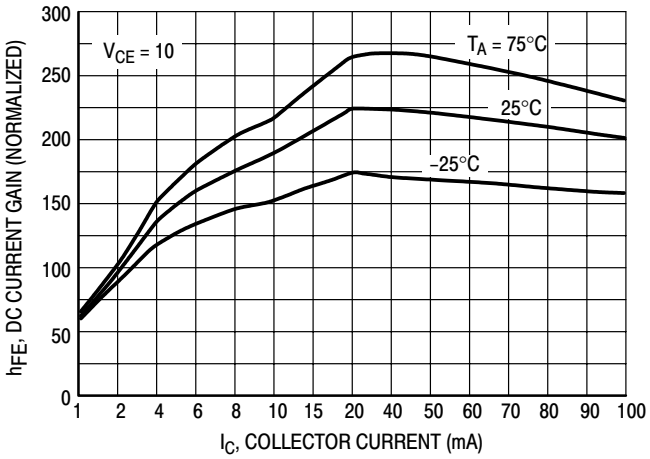


Figure 19. DC Current Gain

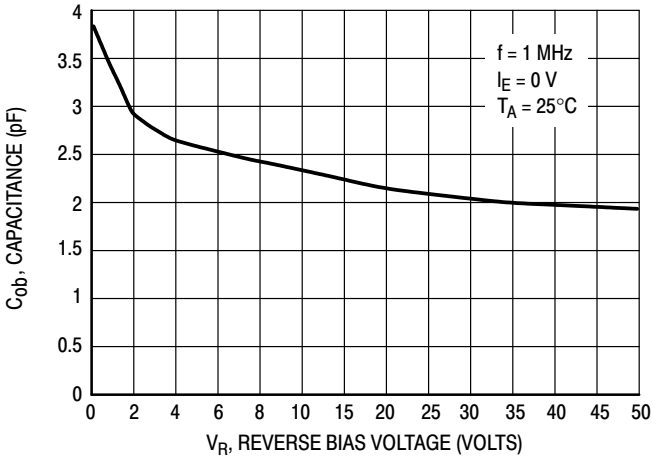


Figure 20. Output Capacitance

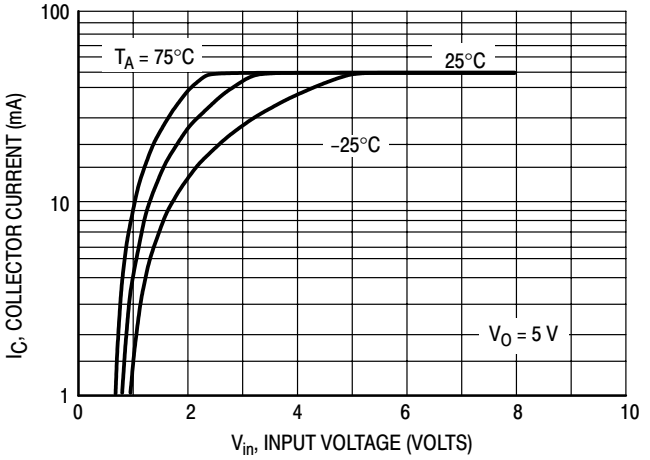


Figure 21. Output Current versus Input Voltage

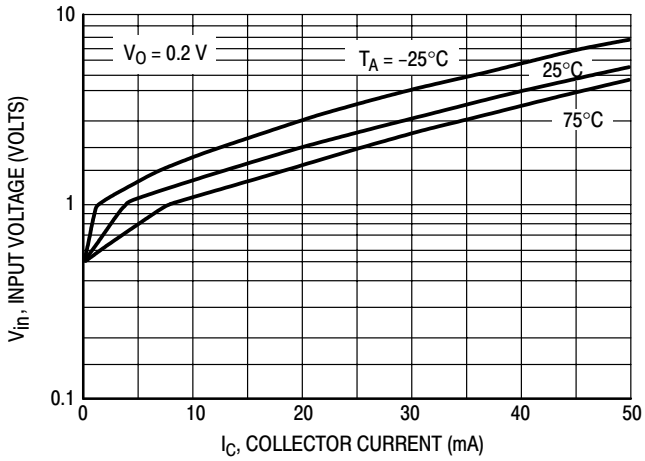


Figure 22. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

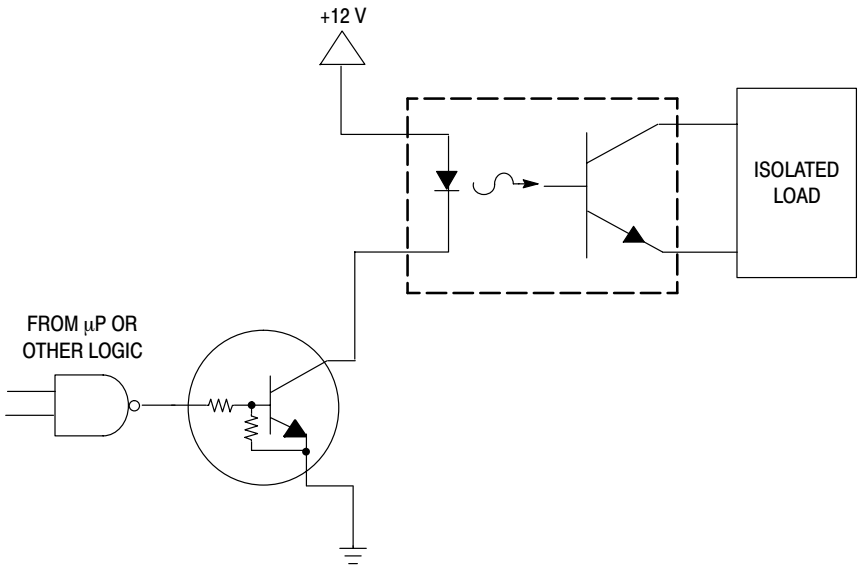


Figure 23. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

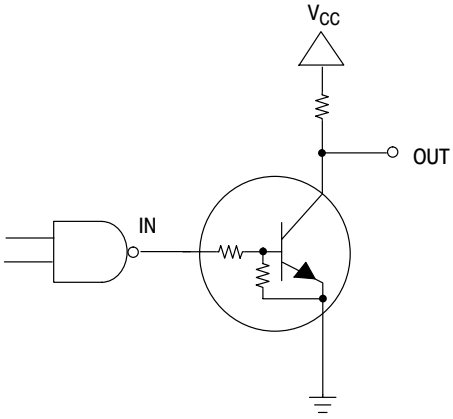


Figure 24. Open Collector Inverter: Inverts the Input Signal

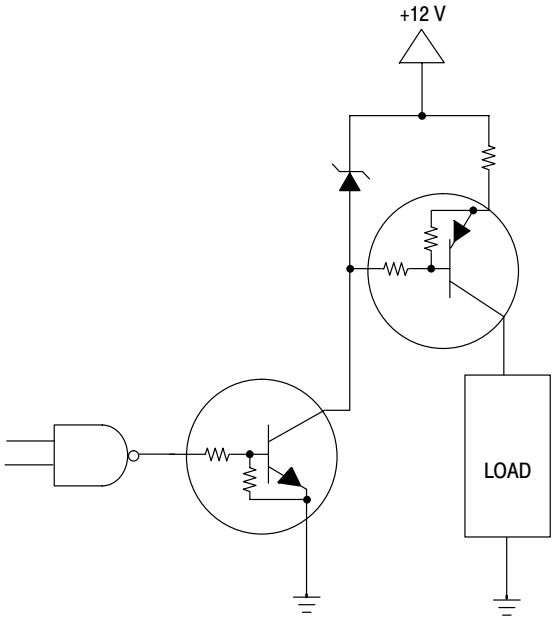
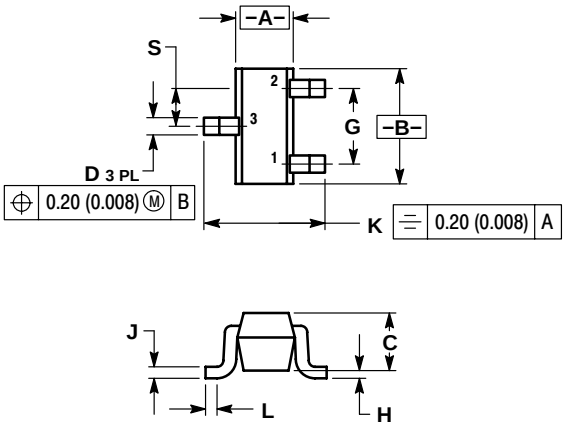


Figure 25. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

SC−75/SOT−416
CASE 463−01
ISSUE C

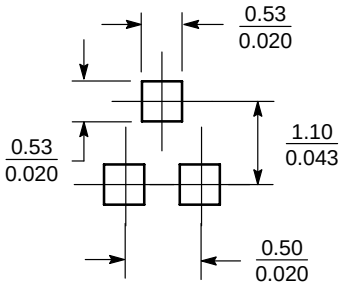


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
B	1.40	1.80	0.055	0.071
C	0.60	0.90	0.024	0.035
D	0.15	0.30	0.006	0.012
G	1.00 BSC		0.039 BSC	
H	−−−	0.10	−−−	0.004
J	0.10	0.25	0.004	0.010
K	1.45	1.75	0.057	0.069
L	0.10	0.20	0.004	0.008
S	0.50 BSC		0.020 BSC	

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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