256Kx32 Synchronous Pipline Burst SRAM 3.3V

FEATURES

- t_{KHQV} times of 3.5, 3.8 and 4.0ns
- 166, 150 and 133 MHz clock speed
- DSP Memory Solution
  - Texas Instruments' TMS320C6201
  - Texas Instruments' TMS320C67x
- Package:
  - 119 pin BGA, JEDEC MO-163
- 3.3V Operating Supply Voltage
- 3.5ns Output Enable access time
- Single Write Control and Output Enable Lines
- Single Chip Enable Line
- 56% space savings vs. monolithic TQFPs
- Multiple VCC and VSS pins
- Reduced inductance and capacitance

DESCRIPTION

The EDI2DL32256VxxBC is a 3.3V, 256Kx32 Synchronous Pipeline Burst SRAM constructed with two 256Kx16 die mounted on a multi-layer laminate substrate. The device is packaged in a 119 lead, 14mm by 22mm, BGA. It is available with clock speeds of166, 150 and 133 MHz. The device is a Pipeline Burst SRAM, allowing the user to develop a fast external memory for Texas Instruments' "C6x". In Burst Mode data from the first memory location is available in three clock cycles, while the subsequent data is available in one clock cycle (3/1/1/1). Subsequent burst addresses are generated by the TMS320C6x DSP. Individual address locations can also be read, allowing one memory access in 3 clock cycles. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE\), burst control input (ADSC\), byte write enables (BW0\ to BW3\) and Write Enable (BWE\).

Asynchronous inputs include the output enable (OE\), burst mode control (MODE), and sleep mode control (ZZ). The data outputs (DQ), enabled by OE\, are also asynchronous.

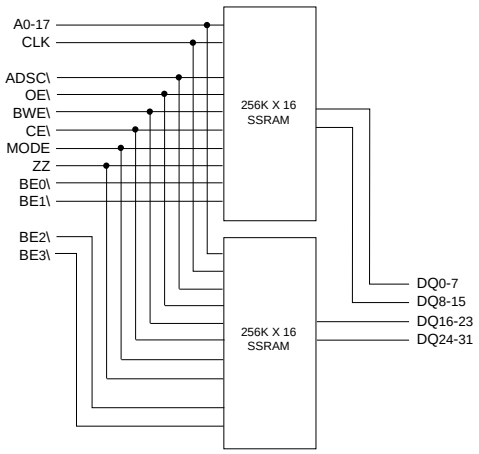
Address lines and the chip enable are registered with the address status controller (ADSC\) input pin.

FIG. 1

PIN CONFIGURATION

	1	2	3	4	5	6	7	
A	V_{DD}	A	A	NC	A	A	V_{DD}	A
B	NC	NC	A	ADSC\	A	A	NC	B
C	NC	A	A	V_{DD}	A	A	NC	C
D	DQ_{16}	NC	V_{SS}	NC	V_{SS}	NC	DQ_8	D
E	DQ_{18}	DQ_{17}	V_{SS}	CE\	V_{SS}	DQ_9	DQ_{10}	E
F	V_{DD}	DQ_{19}	V_{SS}	OE\	V_{SS}	DQ_{11}	V_{DD}	F
G	DQ_{21}	DQ_{20}	BE_2\	NC	BE_1\	DQ_{12}	DQ_{13}	G
H	DQ_{23}	DQ_{22}	V_{SS}	NC	V_{SS}	DQ_{14}	DQ_{15}	H
J	V_{DD}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DD}	J
K	DQ_{31}	DQ_{30}	V_{SS}	CLK	V_{SS}	DQ_6	DQ_7	K
L	DQ_{29}	DQ_{28}	BE_3\	NC	BE_0\	DQ_4	DQ_5	L
M	V_{DD}	DQ_{27}	V_{SS}	BWE\	V_{SS}	DQ_3	V_{DD}	M
N	DQ_{26}	DQ_{25}	V_{SS}	A_1	V_{SS}	DQ_1	DQ_2	N
P	DQ_{24}	NC	V_{SS}	A_0	V_{SS}	NC	DQ_0	P
R	NC	A	MODE	V_{DD}	NC	A	NC	R
T	NC	NC	A	A	A	NC	ZZ	T
U	V_{DD}	NC	NC	NC	NC	NC	V_{DD}	U
	1	2	3	4	5	6	7	

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Symbol	Type	Description
Various	A_{0-17}	Input Synchronous	Addresses: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
L5,G5 G3,L3	BE0\,BE1\, BE2\,BE3\	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ BE2\, BE3\ cycle. BE0\ controls DQ0-7. BE1\ controls DQ8-15. BE2\ controls DQ16-23. BE3\ controls DQ24-31
M4	BWE\	Input Synchronous	Byte Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
K4	CLK	Input Synchronous	Clock:This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clockís rising edge.
E4	CE\	Input Synchronous	Chip Enable: This active LOW inputs is used to enable the device.
F4	OE\	Input	Output Enable: This active LOW asynchronous input enables the data output drivers
B4	ADSC\	Input Synchronous	Address Status Controller: This active LOW input causes device to be deselected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
R3	MODE	Input	Static Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
T7	ZZ	Input Synchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect)
Various	DQ_{0-31}	Input/Output	Data Inputs/Outputs: First byte is DQ_{0-7}, second byte is DQ_{8-15}, third byte is DQ_{16-23}, fourth byte is DQ_{24-31}
Various	Vcc	Supply	Core power supply: +3.3V -5%/+5%
Various	Vss	Ground	Ground

TRUTH TABLE

Operation	Address Used	CE\	ADSC\	WRITE\	OE\	DQ
Deselected Cycle, Power Down	None	H	L	X	X	High-Z
WRITE Cycle, Begin Burst	External	L	L	L	X	D
READ Cycle, Begin Burst	External	L	L	H	L	Q
READ Cycle, Begin Burst	External	L	L	H	H	High-Z
READ Cycle, Suspend Burst	Current	X	H	H	L	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	High-Z
READ Cycle, Suspend Burst	Current	H	H	H	L	Q
READ Cycle, Suspend Burst	Current	H	H	H	H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	L	X	D
WRITE Cycle, Suspend Burst	Current	H	H	L	X	D

NOTE:

1. X means ìdonít careî, H means logic HIGH. L means logic LOW.
2a. WRITE\ = L, means [BE0*BE1*BE2*BE3\]*BWE\ equals LOW
2b. WRITE\ = H, means [BE0*BE1*BE2*BE3\]*BWE\ equals HIGH
3. All inputs except OE\ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle
5. For a write operation following a read operation, OE\ must be HIGH before the input data required setup time plus High-Z time for OE\ and staying HIGH though out the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-0.5V to 4.6V
V_{IN}	-0.5V to Vcc+0.5V
Storage Temperature	-55°C to +110°C
Junction Temperature	+110°C
Power Dissipation	3 Watts
Short Circuit Output Current (per I/O)	20 mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PARTIAL TRUTH TABLE

Function	BWE\	BE0\	BE1\	BE2\	BE\3
READ	H	X	X	X	X
WRITE one Byte (DQ_{0-7})	L	L	H	H	H
WRITE all Bytes	L	L	L	L	L

RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2	Vcc+0.3	V
Input Low Voltage	V_{IL}	-0.3	0.7	V
Supply Voltage	Vcc	3.135	3.465	V

CAPACITANCE

(f = 1MHz, V_{IN} = Vcc or Vss)

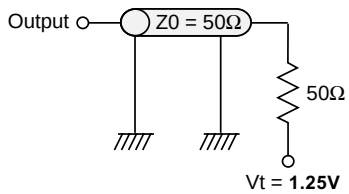
Parameter	Symbol	Max	Unit
Address Lines	C_A	TBD	pF
Data Lines	$C_{D/Q}$	TBD	pF
Control Lines	C_C	TBD	pF

DC ELECTRICAL CHARACTERISTICS

(f = 1MHz, V_{IN} = Vcc or Vss)

Parameter	Symbol	Conditions	Min	Max	Units
Power Supply Current: Operating	I_{CC1}	Device Selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} MIN; Vcc = MAX; outputs open		850	mA
CMOS Standby	I_{SB2}	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0		20	mA
TTL Standby	I_{SB3}	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; Vcc = MAX; CLK frequency = 0		40	mA
TTL Standby	I_{SB4}	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; Vcc = MAX; CLK cycle time ≥ t_{CK} MIN		40	mA
Input Leakage Current	I_{LI}	0V < V_{IN} < Vcc	-2	2	µA
Output Leakage Current	I_{LO}	Output(s) disabled, 0V ≤ V_{OUT} ≤ Vcc	-2	2	µA
Output High Voltage	V_{OH}	I_{OH} = -2.0mA	2.4		V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA		0.7	V

AC TEST CIRCUIT



AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	Vss to 2.5	V
Input Rise and Fall Times (max)	1.8	ns
Input and Output Timing Levels	1.25	V
Output Load	See figure, at left	

AC ELECTRICAL CHARACTERISTICS

Description	Symbol	3.5ns Min	3.5ns Max	3.8ns Min	3.8ns Max	4.0ns Min	4.0ns Max	Units
Clock								
Clock cycle time	t_{KHKH}	6		6.7		7.5		
Clock HIGH time	t_{KHKL}	2.4		2.6		2.8		
Clock LOW time	t_{KLKH}	2.4		2.6		2.8		
Output Times								
Clock to output valid	t_{KHQV}		3.5		3.8		4.0	
Clock to output in Low-Z	t_{KHQX}	0		0		0		
Clock to output in High-Z	t_{KHQZ}	1.5	6	1.5	6.7	1.5	7.5	
OE to output valid	t_{OELQV}		3.5		3.5		3.8	
OE to output in Low-Z	t_{OELQX}	0		0		0		
OE to output in High-Z	t_{OEHQZ}		3.5		3.5		3.8	
Setup Times								
Address Status Controller valid to Clock	t_{SCVKH}	1.5		1.5		1.5		
Address valid to Clock	t_{AVKH}	1.5		1.5		1.5		
Chip Enable valid to Clock	t_{EVKH}	1.5		1.5		1.5		
Write Enable (BWE\) valid to Clock	t_{WLKH}	1.5		1.5		1.5		
Data Valid to Clock	t_{DVKH}	1.5		1.5		1.5		
Hold Times								
Address Status Controller Hold time	t_{KHSCX}	0.5		0.5		0.5		
Address Hold time	t_{KHAX}	0.5		0.5		0.5		
Chip Enable Hold time	t_{KHEX}	0.5		0.5		0.5		
Write Enable (BWE\) Hold time	t_{KHWX}	0.5		0.5		0.5		
Data Hold time	t_{KHDX}	0.5		0.5		0.5		

FIG. 2 READ TIMING

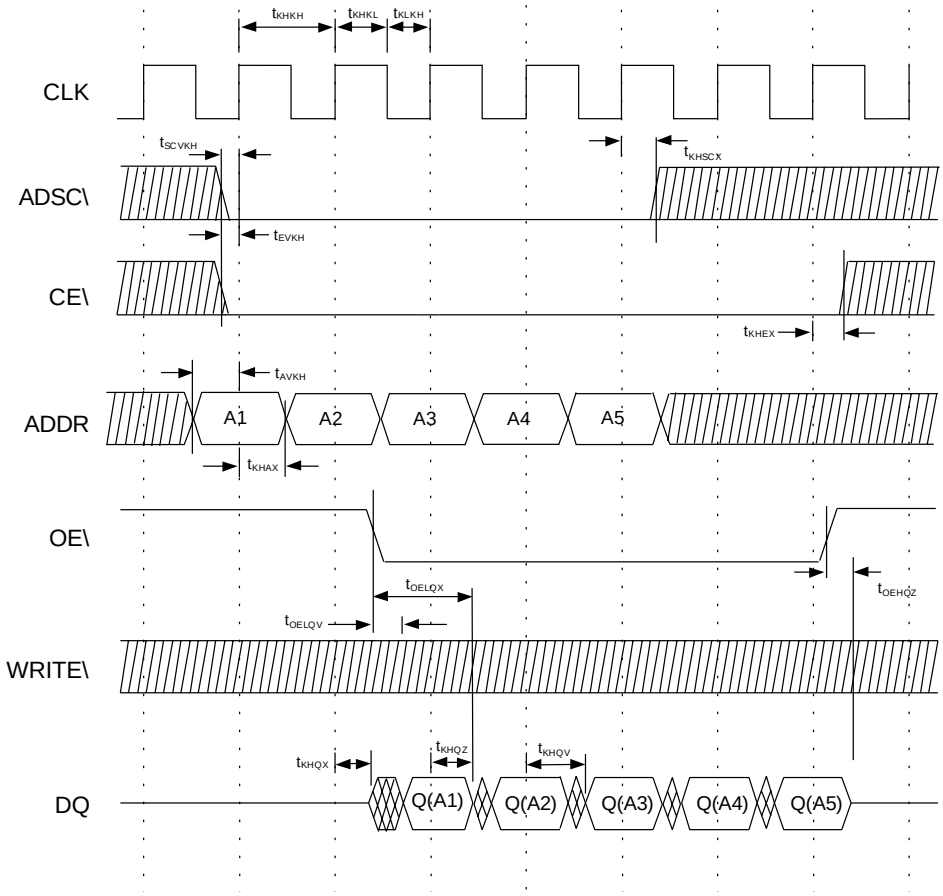
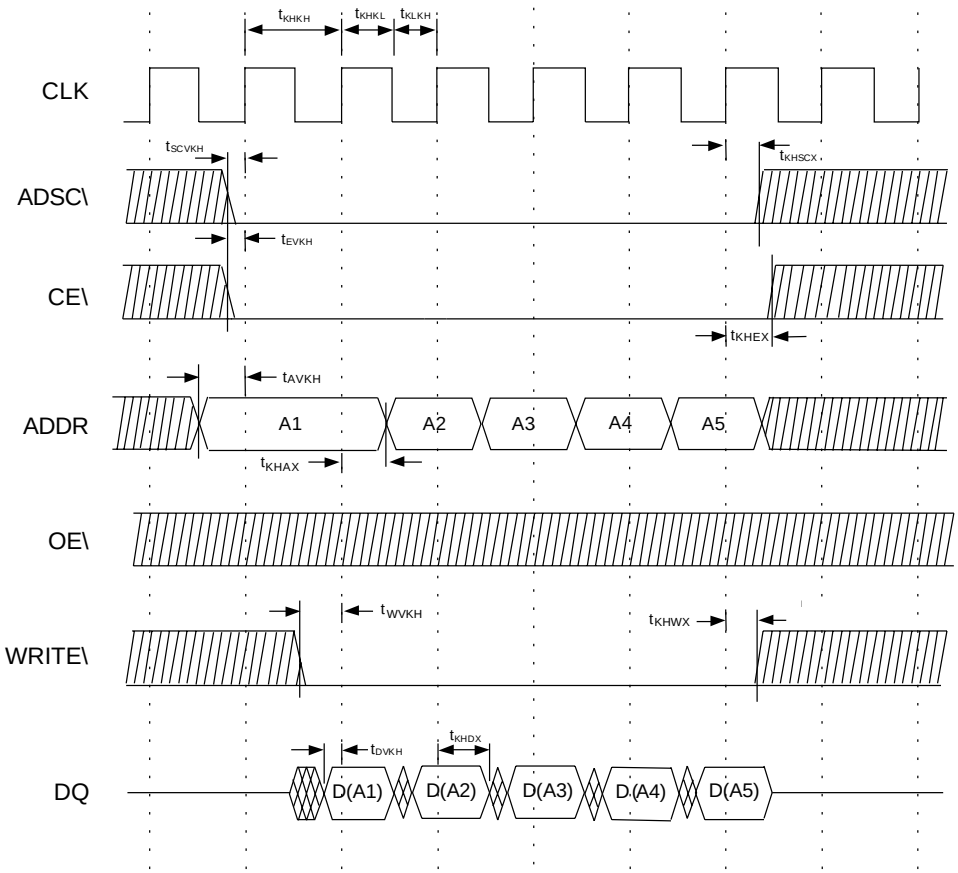


FIG. 3 WRITE TIMING



ORDERING INFORMATION

Commercial Temperature Range (0°C to +70°C)

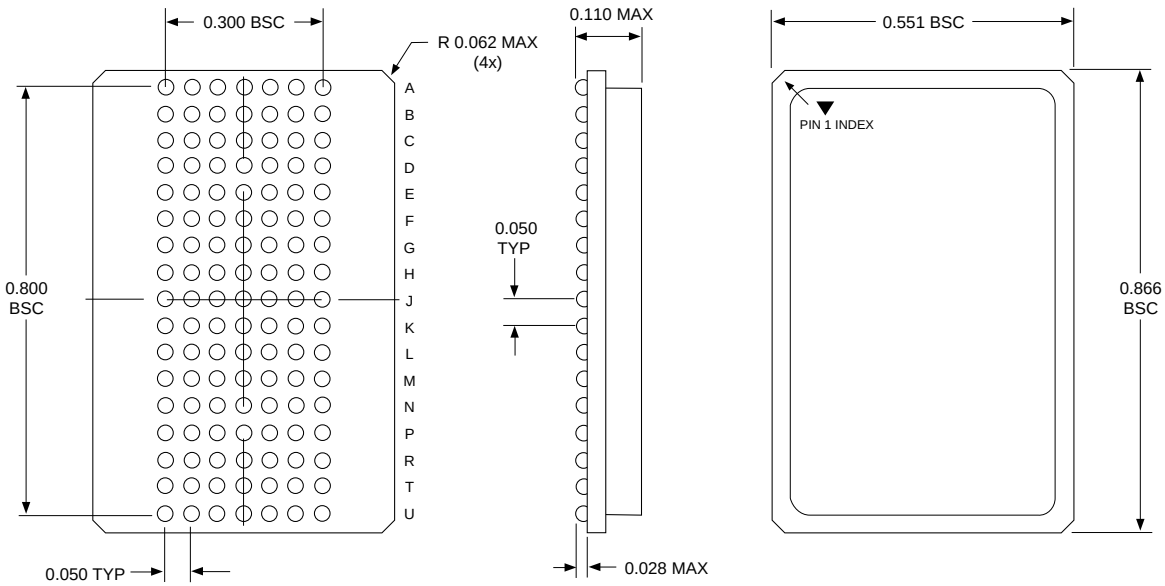
Part Number	t_{KQ} (ns)	Clock Frequency (MHz)	Package No.
EDI2DL32256V35BC	3.5	166	TBD
EDI2DL32256V38BC	3.8	150	TBD
EDI2DL32256V40BC	4.0	133	TBD

Industrial Temperature Range (-40°C to +85°C)

Part Number	t_{KQ} (ns)	Clock Frequency (MHz)	Package No.
EDI2DL32256V40BI	4.0	133	TBD

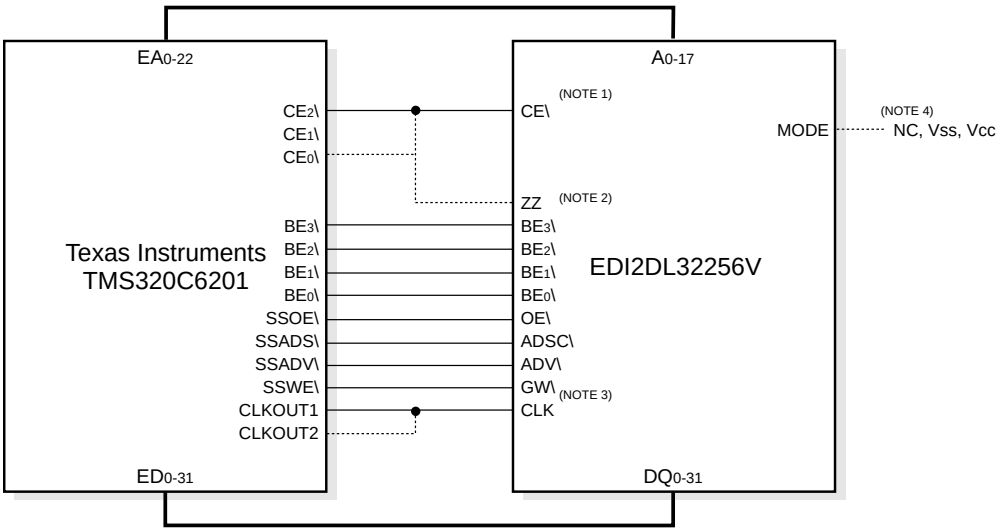
PACKAGE DESCRIPTION: 119 LEAD BGA

JEDEC MO-163



ALL DIMENSIONS ARE IN INCHES

FIG. 5
INTERFACING THE TEXAS INSTRUMENTS TMS320C6201 WITH THE EDI2DL32256V (256Kx32 SSRAM)



NOTES:

1. Either $\overline{CE}_0$ or $\overline{CE}_2$ can be used to enable the device.
2. When the ZZ pin is asserted HIGH, the device will be in CMOS standby mode regardless of the state of any other pins. While in standby mode the device will take one complete Clock cycle to become active again after a LOW is asserted on the ZZ pin. One possible option for the designer concerned about power is to tie the ZZ signal to the chip enable they are using for the device. Any time the chip is disabled (by driving the chip enable pin HIGH) the device will go into standby mode. Standby mode can also be achieved by tying the ZZ pin LOW or allowing it to float and meeting all the signal conditions specified in the data sheet.
3. Use CLKOUT1 for running the memory at the same clock speed as the C6x. Use CLKOUT2 for running the SBSRAM at one half the clock rate of the C6x.
4. The MODE pin can be tied to Vss (Linear Burst), tied to Vcc (Interleaved Burst) or allowed to float (Interleaved Burst).