128Kx8 MONOLITHIC SRAM, SMD 5962-89598

FEATURES

- Access Times of 70, 85, 100ns
- Available with Single Chip Selects (EDI88128) or Dual Chip Selects (EDI88130)
- 2V Data Retention (LP Versions)
- CS# and OE# Functions for Bus Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 128Kx8
- Industrial, Military and Commercial Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
  - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
  - 32 lead Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

The EDI88128C is a high speed, high performance, Monolithic CMOS Static RAM organized as 128Kx8.

The device is also available as EDI88130C with an additional chip select line (CS2) which will automatically power down the device when proper logic levels are applied.

The second chip select line (CS2) can be used to provide system memory security during power down in non-battery backed up systems and simplifiy decoding schemes in memory banking where large multiple pages of memory are required.

The EDI88128C and the EDI88130C have eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

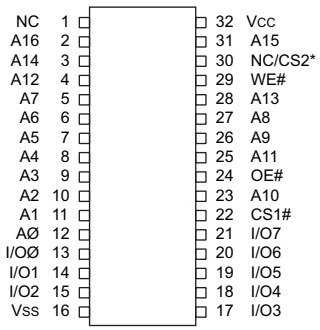
Low power versions, EDI88128LP and EDI88130LP, offer a 2V data retention function for battery back-up opperation. Military product is available compliant to Appendix A of MIL-PRF-38535.

FIGURE 1 – PIN CONFIGURATION

32 DIP

32 SOJ

Top View

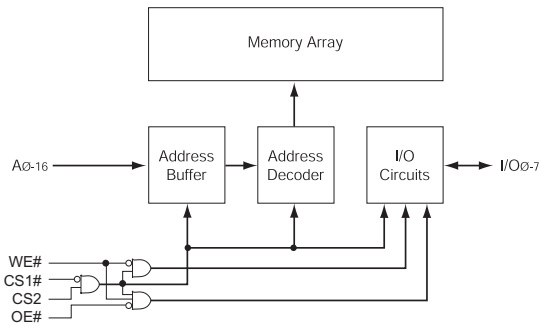


* Pin 30 is NC for 88128 or CS2 for 88130.

PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
WE#	Write Enable
CS1#, CS2	Chip Selects
OE#	Output Enable
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to V_{SS}	-0.5 to 7.0	V
Operating Temperature T_A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS1#	CS2#	WE#	Mode	Output	Power
X	H	X	X	Standby	High Z	Icc2, Icc3
X	X	L	X	Standby	High Z	Icc2, Icc3
X	X	L	X	Output Deselect	High Z	Icc1
H	L	H	H	Output Deselect	High Z	Icc1
L	L	H	H	Read	Data Out	Icc1
X	L	H	L	Write	Data In	Icc1

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	C_I	V_{IN} = V_{CC} or V_{SS}, f = 1.0MHz	12	pF
Input/Output Lines	C_O	V_{OUT} = V_{CC} or V_{SS}, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		-5	—	+5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}, CS1# ≥ V_{IH} and/or CS2# ≤ V_{IL}		-10	—	+10	µA
Operating Power Supply Current	I_{CC1}	WE#, CS1# = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle	(70-85ns)	—		120	mA
		CS2# = V_{IH}	(100ns)	—		110	mA
Standby (TTL) Power Supply Current	I_{CC2}	CS1# ≥ V_{IH} and/or CS2# ≤ V_{IL}, V_{IN} ≥ V_{IH} or ≤ V_{IL}		—		10	mA
Full Standby Power Supply Current	I_{CC3}	CS1# ≥ V_{CC} -0.2V and/or CS2# ≤ V_{CC}+0.2V	C	—	1	5	mA
		V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	LP	—	—	1	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	—	—	V

NOTE: DC test conditions : V_{IL} = 0.3V, V_{IH} = V_{CC} -0.3V

AC Characteristics – Read Cycle

V_{CC} = 5V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		85		100		ns
Address Access Time	t_{AVQV}	t_{AA}		70		85		100	ns
Chip Select Access Time	t_{ELQV}	t_{ACS}		70		85		100	ns
	t_{SHQV}	t_{ACS}		70		85		100	ns
Chip Select to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
	t_{SHQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		30		30		30	ns
	t_{SLQZ}	t_{CHZ}		30		30		30	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		25		30		50	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z (1)	t_{GHQZ}	t_{OHZ}	0	30	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

AC Test Conditions

Figure 1

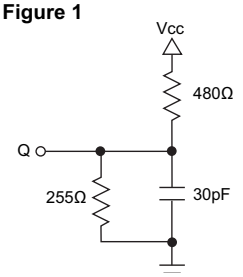
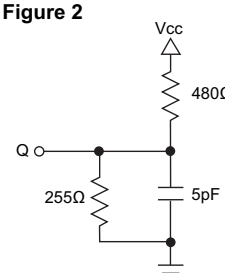


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2

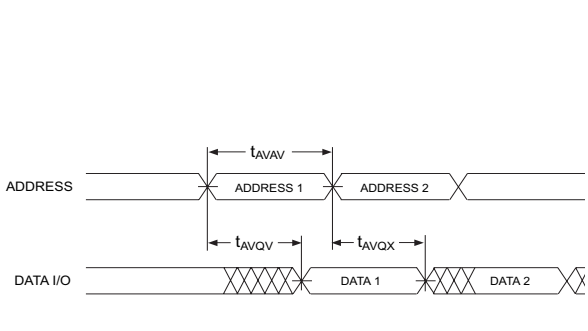
AC CHARACTERISTICS – WRITE CYCLE

V_{CC} = 5V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

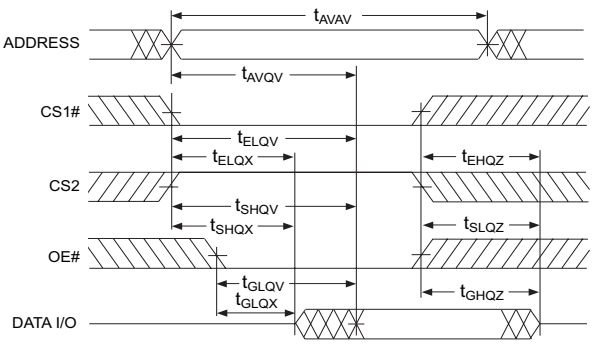
Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		85		100		ns
Chip Select to End of Write	t_{ELWH}	t_{CW}	60		75		85		ns
	t_{ELEH}	t_{CW}	60		75		85		ns
	t_{SHWH}	t_{CW}	60		75		85		ns
	t_{SHSL}	t_{CW}	60		75		85		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		ns
	t_{AVSH}	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	60		75		85		ns
Write Pulse Width	t_{WLWH}	t_{WP}	35		70		80		ns
	t_{WLEH}	t_{WP}	35		70		80		ns
	t_{WLSL}	t_{WP}	35		70		80		ns
Write Recovery Time	t_{WHAX}	t_{WR}	5		5		5		ns
	t_{EHAX}	t_{WR}	5		5		5		ns
	t_{SLAX}	t_{WR}	5		5		5		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		ns
	t_{SLDX}	t_{DH}	0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time	t_{DVWH}	t_{DW}	35		40		40		ns
	t_{DVEH}	t_{DW}	35		40		40		ns
	t_{DVSL}	t_{DW}	35		40		40		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	5		5		5		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – TIMING WAVEFORM — READ CYCLE

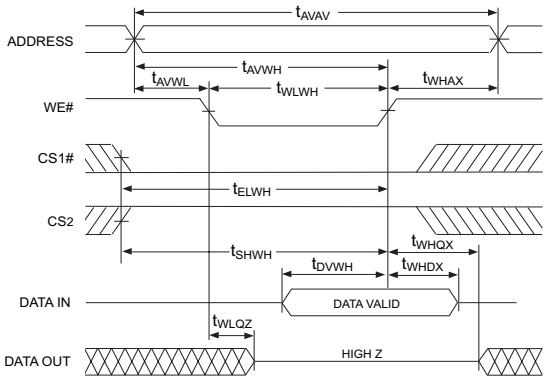


READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



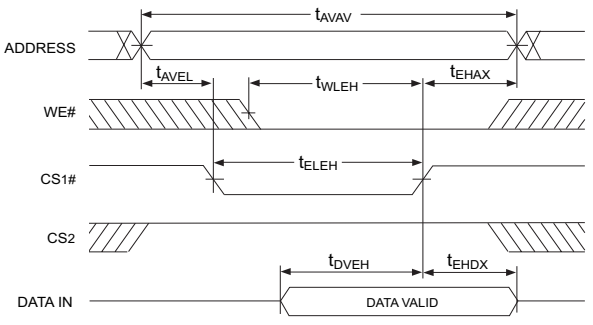
READ CYCLE 2 (WE# HIGH)

FIGURE 3 – WRITE CYCLE 1



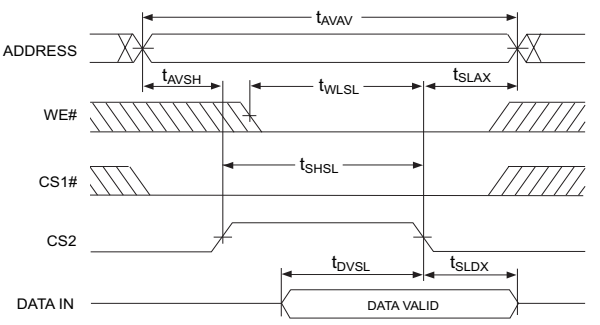
WRITE CYCLE 1 - LATE WRITE, WE# CONTROLLED

FIGURE 4 – WRITE CYCLE 2



WRITE CYCLE 2 - EARLY WRITE, CS1# CONTROLLED

WRITE CYCLE 3



WRITE CYCLE 3 - EARLY WRITE, CS2 CONTROLLED

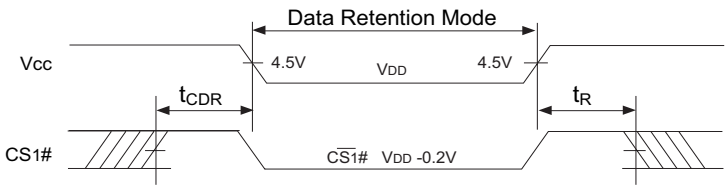
DATA RETENTION CHARACTERISTICS (EDI88128LP & EDI88130LP ONLY)

-55°C ≤ T_A ≤ +125°C

Characteristic Low Power Version only	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{DD}	V_{DD} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	CS1# ≥ V_{DD} -0.2V	–	–	400	µA
Chip Disable to Data Retention Time (1)	T_{CDR}	V_{IN} ≥ V_{DD} -0.2V	0	–	–	ns
Operation Recovery Time (1)	T_R	or V_{IN} ≤ 0.2V	T_{AVAV}*	–	–	ns

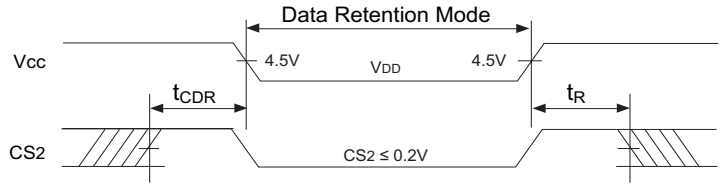
NOTE:
1. Parameter guaranteed by design, but not tested.
* Read Cycle Time

FIGURE 5 – DATA RETENTION – CS1# CONTROLLED



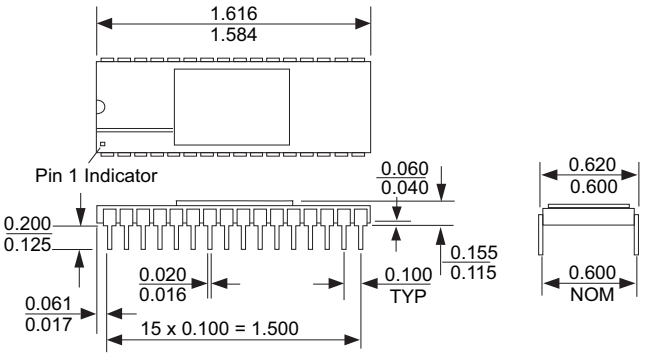
DATA RETENTION, CS1# CONTROLLED

FIGURE 6 – DATA RETENTION — CS2 CONTROLLED



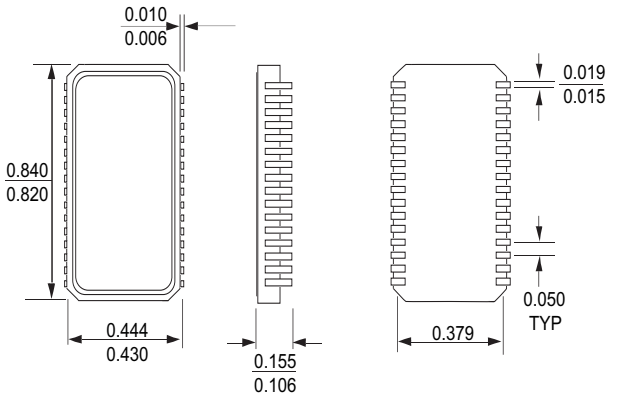
DATA RETENTION, CS2 CONTROLLED

PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600MILS WIDE)



ALL DIMENSIONS ARE IN INCHES

PACKAGE 140: 32 LEAD CERAMIC SOJ



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 128 C X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 128Kx8

8 130 = Dual Chip Select

TECHNOLOGY:

C = CMOS Standard Power

LP = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

N = 32 lead Ceramic SOJ (Package 140)

DEVICE GRADE:

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C