

512Kx8 Monolithic SRAM, CMOS

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
 - Access Times of 70, 85, 100ns
 - Data Retention Function (LP version)
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- 32 lead JEDEC Approved Evolutionary Pinout
 - Ceramic Sidebraced 600 mil DIP (Package 9)
 - Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

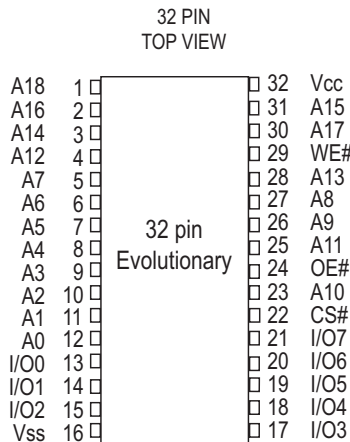
The EDI88512C is a 4 megabit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. Both the DIP and CSOJ packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128C. Pins 1 and 30 become the higher order addresses.

A Low Power version with Data Retention (EDI88512LP) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

* This product is subject to change without notice.

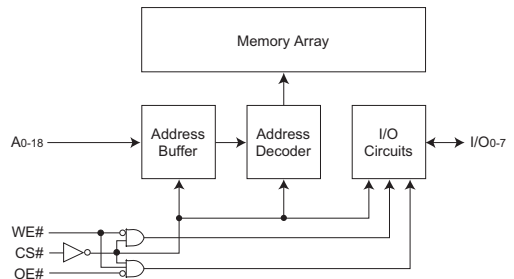
FIGURE 1 – PIN CONFIGURATION

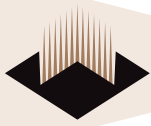


PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS#	Chip Selects
OE#	Output Enable
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T _A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T _J	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	I _{CC2} , I _{CC3}
H	L	H	Output Deselect	High Z	I _{CC1}
L	L	H	Read	Data Out	I _{CC1}
X	L	L	Write	Data In	I _{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	C _I	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	12	pF
Data Lines	C _O	V _{OUT} = V _{CC} or V _{SS} , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Typ*	Max	Units	
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}	—	—	±10	µA	
Output Leakage Current	I _{LO}	V _{IO} = 0V to V _{CC}	—	—	±10	µA	
Operating Power Supply Current	I _{CC1}	WE#, CS# = V _{IL} , I _{IO} = 0mA, Min Cycle (70-100ns)	—	45	75	mA	
Standby (TTL) Power Supply Current	I _{CC2}	CS# ≥ V _{IH} , V _{IN} ≤ V _{IL} , V _{IN} ≥ V _{IH}	—	3	10	mA	
Full Standby Power Supply Current	I _{CC3}	CS# ≥ V _{CC} - 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	C	—	—	5	mA
			LP	—	—	2	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	V	

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC TEST CONDITIONS

Figure 1

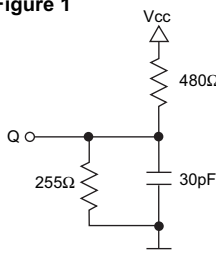
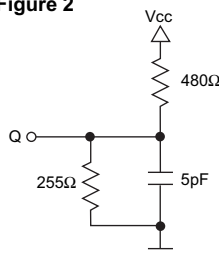
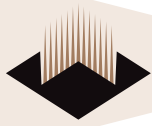


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{EHQZ} and t_{WLQZ}, C_L = 5pF Figure 2



AC CHARACTERISTICS – READ CYCLE

$V_{CC} = 5.0V, V_{SS} = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	70		85		100		ns
Address Access Time	t _{AVQV}	t _{AA}		70		85		100	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		70		85		100	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	10		10		10		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}		25		30		30	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	10		10		10		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		35		45		50	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	5		5		5		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}	0	25	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

$V_{CC} = 5.0V, V_{SS} = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		85		100		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	60		70		80		ns
	t _{ELEH}	t _{CW}	60		70		80		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	65		70		80		ns
	t _{AVEH}	t _{AW}	65		70		80		ns
Write Pulse Width	t _{WLWH}	t _{WP}	50		55		60		ns
	t _{WLEH}	t _{WP}	50		55		60		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	25	0	30	0	30	ns
Data to Write Time	t _{DVWH}	t _{DW}	40		40		40		ns
	t _{DVEH}	t _{DW}	30		35		40		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	5		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIGURE 2 – TIMING WAVEFORM - READ CYCLE

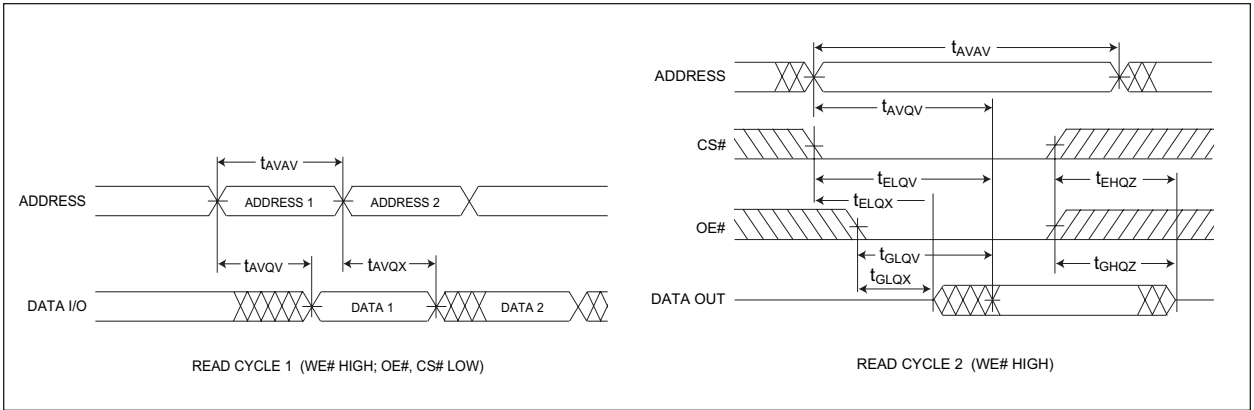


FIGURE 3 – WRITE CYCLE - WE# CONTROLLED

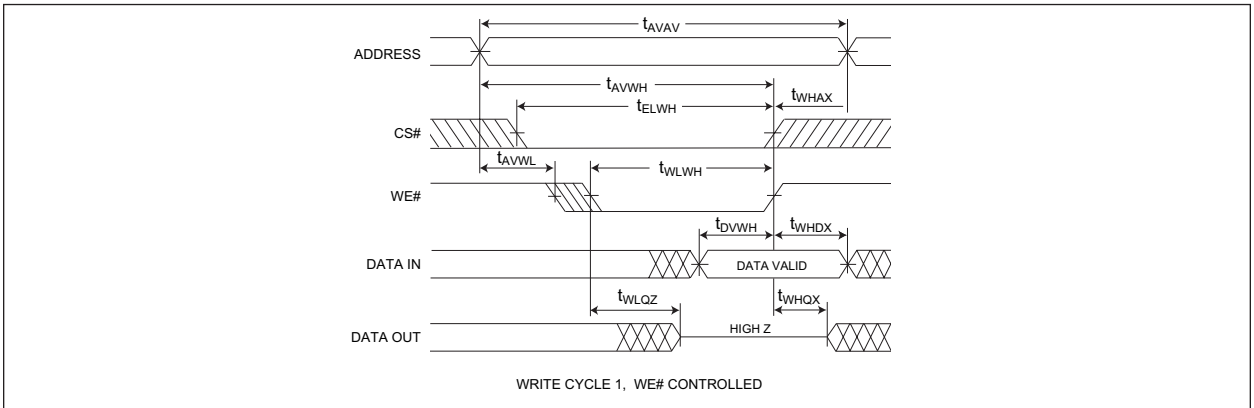
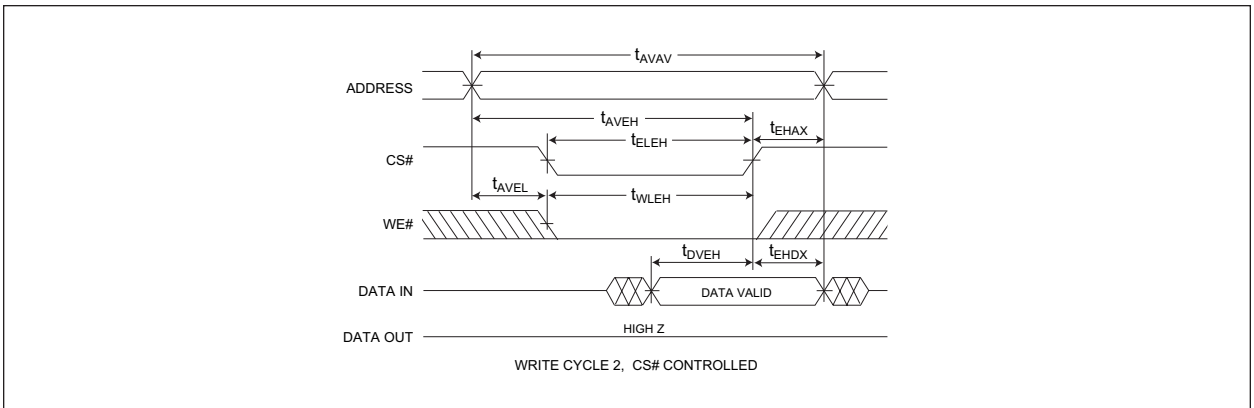
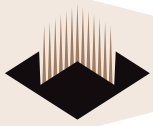


FIGURE 4 – WRITE CYCLE - CS# CONTROLLED



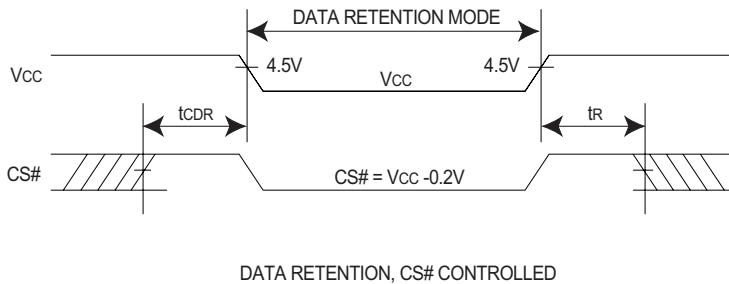


DATA RETENTION CHARACTERISTICS (EDI88512LP ONLY)

-55°C ≤ T_A ≤ +125°C

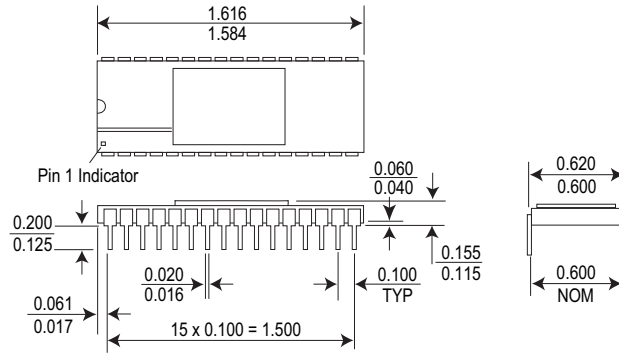
Characteristic	Sym	Conditions	Min	Typ	Max	Units
Low Power Version only						
Data Retention Voltage	V _{CC}	V _{CC} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I _{CCDR}	CS# ≥ V _{CC} - 0.2V	-	-	185	μA
Chip Disable to Data Retention Time	t _{CDR}	V _{IN} ≥ V _{CC} - 0.2V	0	-	-	ns
Operation Recovery Time	T _R	or V _{IN} ≤ 0.2V	t _{AVAV}	-	-	ns

FIGURE 5 – DATA RETENTION - CS# CONTROLLED



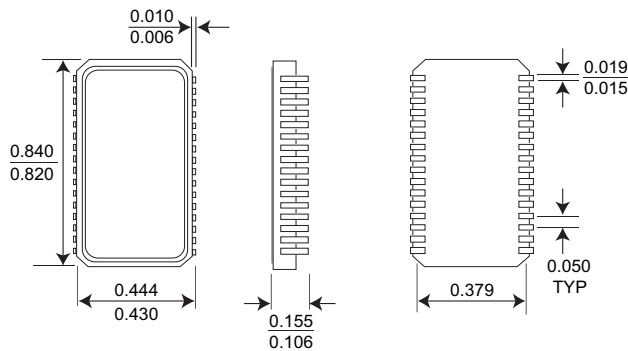


PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP



ALL DIMENSIONS ARE IN INCHES

PACKAGE 140: 32 LEAD CERAMIC SOJ



ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 8512 C X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 512Kx8 _____

TECHNOLOGY: _____

C = CMOS Standard Power

LP = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

N = 32 lead Ceramic SOJ (Package 140)

DEVICE GRADE: _____

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C