512Kx32 SRAM Module.3.3V

FEATURES

- DSP Memory Solution
  - ADSP-21060L (SHARC)
  - ADSP-21062L (SHARC)
  - Texas Instruments TMS320LC31
- RISC Memory Solution
  - MPC860 (Power Quic)
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17, and 20ns
  - Individual Byte Enables
  - User configuration organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC MO-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +3.3V (±5%) Supply Operation

DESCRIPTION

The EDI8L32512V is a high speed, 3.3V, 16 megabit SRAM. The device is available with access times of 12, 15, 17 and 20ns allowing the creation of a no wait state DSP and RISC microprocessor memory solutions.

The device can be configured as a 512K x 32 and used to create a single chip external data memory solution for TI's TMS320LC31 (figure 5), or Analog's SHARC™ DSP (figure 6).

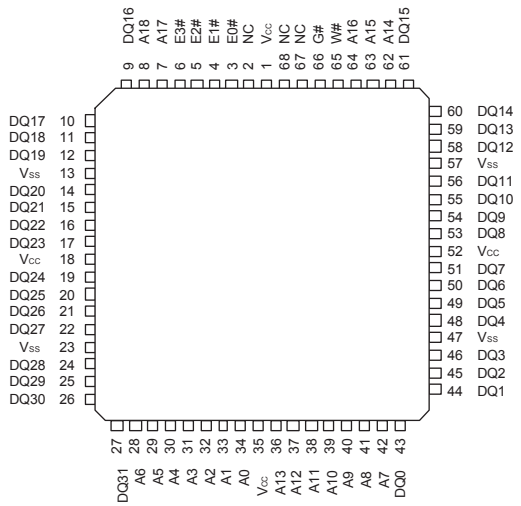
The device provides a 56% space savings when compared to four 512Kx8, 36 pin SOJs. In addition the EDI8K32512V has only a 10pF load on the data lines vs. 32 pF for four plastic SOJs.

The device provides a memory upgrade of the EDI8F32256V (256K x 32) or the EDI8L32128V (128K x 32) (figure 8). Alternatively, the device's chip enables can configure it as a 1M x 16. A 1M x 48 program memory array for Analog's CHARC DSP is created using three devices (figure 7). If this memory is too deep, two 512K x 24s (EDI8L24512V) can be used to create a 512K x 48 array or two 128K x 24s (EDI8L24128V) can be used to create a 128K x 48 array.

Note: Soldier Reflow Temperature should not exceed 260°C for 10 seconds.

FIG. 1

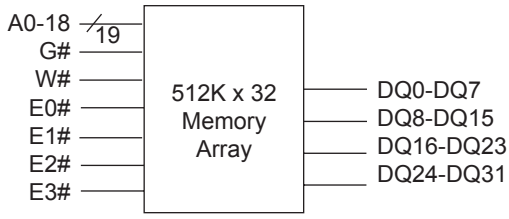
PIN CONFIGURATIONS



PIN DESCRIPTION

A0-A18	Address Inputs
E0#-E3#	Chip Enables (One per Byte)
W#	Master Write Enable
G#	Master Output Enable
DQ0-DQ31	Common Data Input/Output
V_{CC}	Power (+3.3V±5%)
V_{SS}	Ground
NC	No Connectiona

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature t_A (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current	20 mA
Junction Temperature, t_J	-175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	--	+0.8	V

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	10	pF
Chip Enable Line	E0-3	8	pF
Write & Output Enable Line	W#, G#	30	pF

TRUTH TABLE

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	$I_{CC}2$, $I_{CC}3$
L	H	H	Output Deselect	HIGH Z	$I_{CC}1$
L	H	L	Read	D_{OUT}	$I_{CC}1$
L	L	X	Write	D_{IN}	$I_{CC}1$

DC ELECTRICAL CHARACTERISTICS

(V_{CC}= 3.3V, t_A = 25°C)

Parameter	Sym	Conditions	12 & 15			17 & 20			Units
			Min	Typ	Max	Min	Typ	Max	
Operating Power Supply Current	$I_{CC}1$	W# = V_{IL}, II/O = 0mA, Min Cycle	--	440	800	--	440	640	mA
Standby (TTL) Power Supply Current	$I_{CC}2$	E# ≥ V_{IH}, V_{IN} ≤ V_{IL} or V_{IN} ≥ V_{IH}	--	100	300	--	100	200	mA
Full Standby Power CMOS Supply Current	$I_{CC}3$	E# ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}=0.2V or V_{IN} ≤ 0.2V	--	60	80	--	60	100	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	--	--	±20	--	--	±10	µA
Output Leakage Current	I_{LO}	V I/O = 0V TO V_{CC}	--	--	±20	--	--	±10	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	--	--	2.4	--	--	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA	--	--	0.4	--	--	0.4	V

AC TEST CONDITIONS

Figure 1

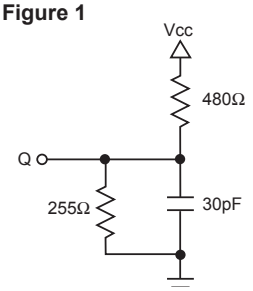
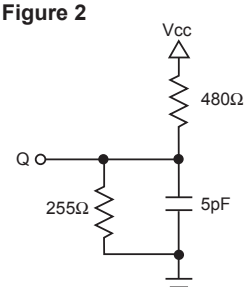


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(Note: For t_{EHQZ},t_{GHQZ} and t_{WLQZ}, CL = 5pF, Figure 2)

AC CHARACTERISTICS READ CYCLE

(V_{CC} = 3.3V, V_{SS} = 0V, t_A = 0°C to -70°C)

Parameter	Symbol		12ns		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	12		15		17		20		ns
Address Access Time	t_{AVQV}	t_{AA}		12		15		17		20	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		10		12		15		20	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		6		7		8		9	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		7		8		9	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	3		3		3		3		ns
Output Disable to Output in High (1)	t_{GHQZ}	t_{OHZ}		6		7		8		9	ns

Notes: 1. Parameter is guaranteed by design but not tested.

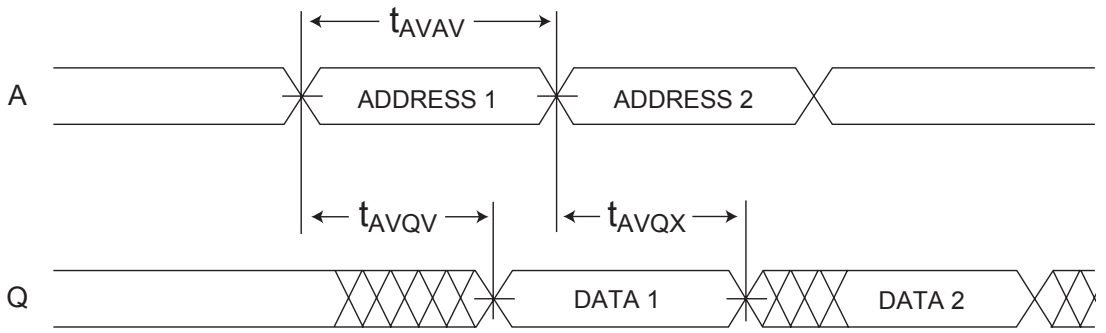
AC CHARACTERISTICS WRITE CYCLE

(V_{CC} = 3.3V, V_{SS} = 0V, t_A = 0°C to -70°C)

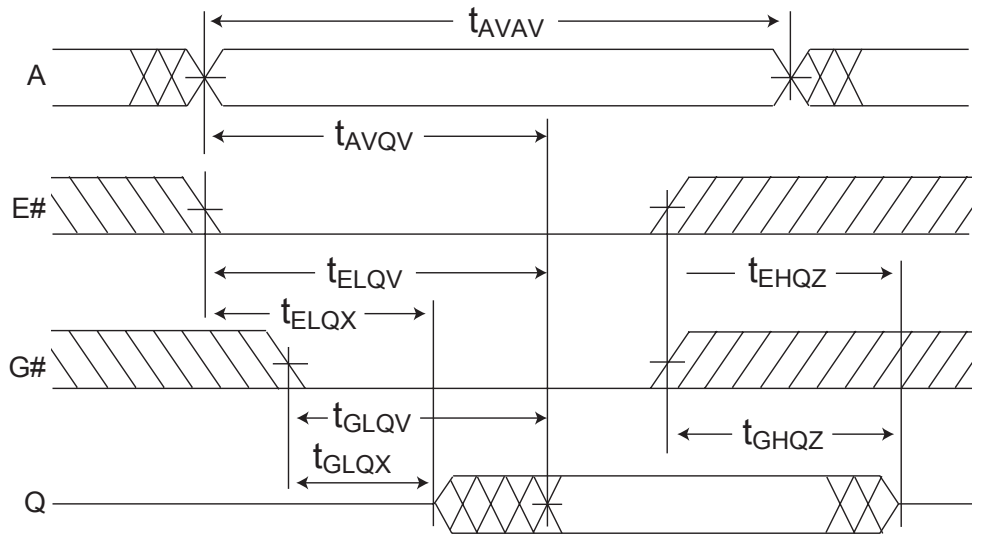
Parameter	Symbol		12ns		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	12		15		17		20		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	8		10		11		12		ns
	t_{ELEH}	t_{CW}	8		10		11		12		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	8		10		11		12		ns
	t_{AHEH}	t_{AW}	8		10		11		12		ns
Write Pulse Width	t_{WLWH}	t_{WP}	8		10		11		12		ns
	t_{ELEH}	t_{WP}	8		10		11		12		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time	t_{DVWH}	t_{DW}	6		7		8		9		ns
	t_{DVEH}	t_{DW}	6		7		8		9		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 2
TIMING WAVEFRONT - READ CYCLE

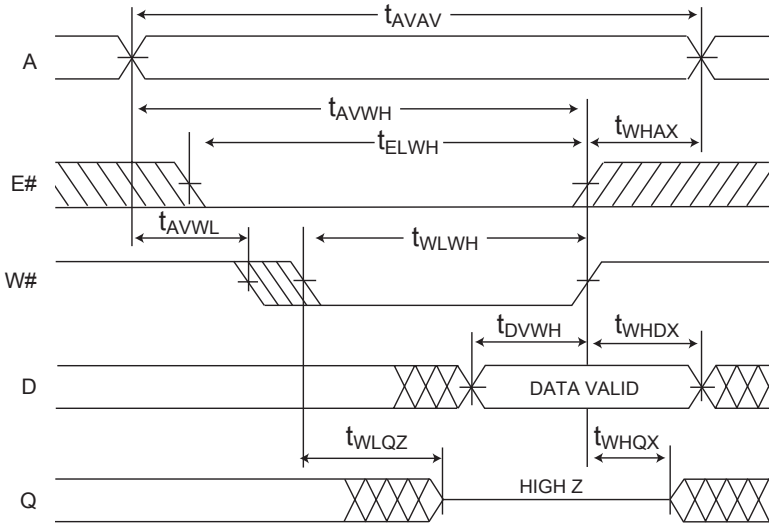


READ CYCLE 1 (W# HIGH; G#, E# LOW)



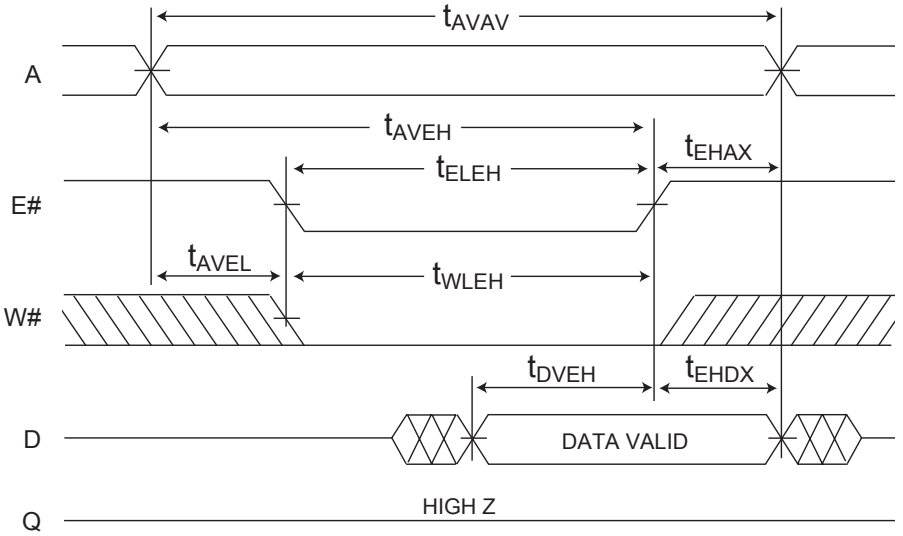
READ CYCLE 2 (W# HIGH)

FIG. 3
WRITE CYCLE - W# CONTROLLED



WRITE CYCLE 1, W# CONTROLLED

FIG. 4
WRITE CYCLE - E# CONTROLLED



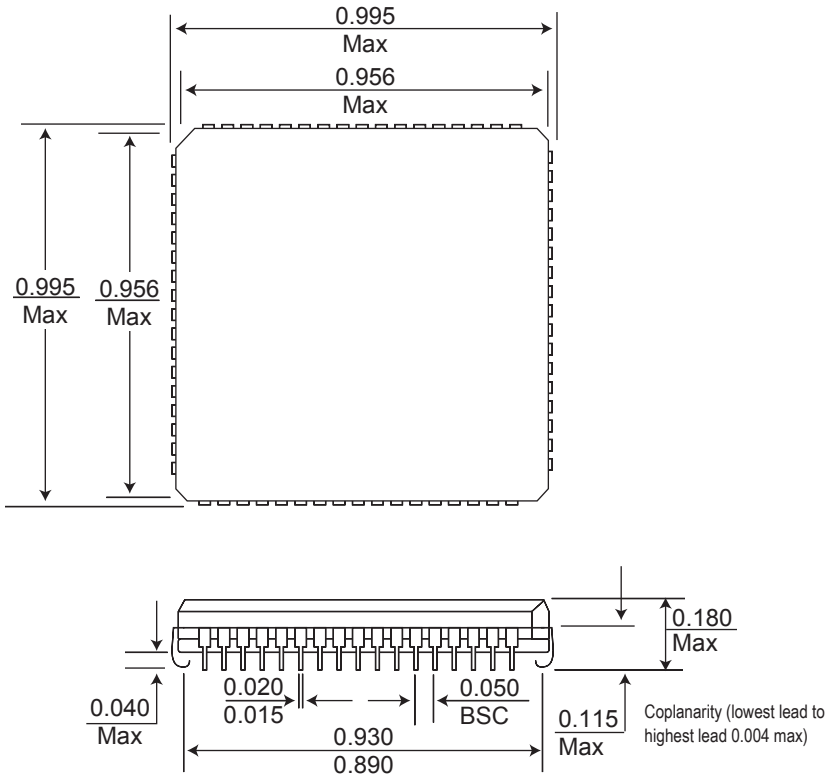
WRITE CYCLE 2, E# CONTROLLED

ORDERING INFORMATION

Commercial Temperature Range (0°C to +70°C)		
Part Number	Speed (ns)	Package No.
EDI8L32512V12AC	12	99
EDI8L32512V15AC	15	99
EDI8L32512V17AC	17	99
EDI8L32512V20AC	20	99

Industrial Temperature Range (-40°C to +85°C)		
Part Number	Speed (ns)	Package No.
EDI8L32512V15AI	15	99
EDI8L32512V17AI	17	99
EDI8L32512V20AI	20	99

PACKAGE 99" 68 LEAD PLCC
JEDEC MO-47AE



ALL DIMENSIONS ARE IN INCHES

FIG 5.

INTERFACING THE TEXAS INSTRUMENTS TMS 320LC32 WITH THE EDI8L32512V (512K X 32)

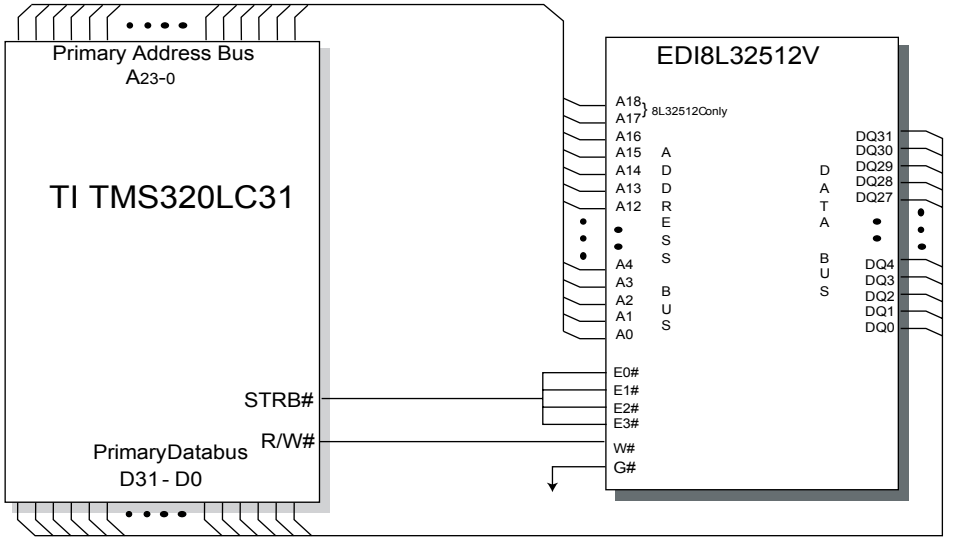


FIG 6.

INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512V (512K X 32 ARRAY).

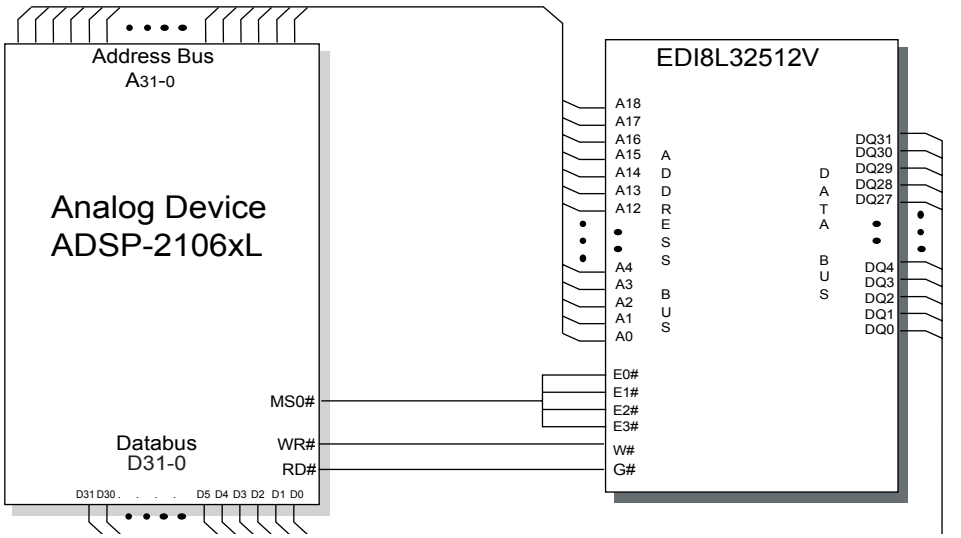


FIG 7.

INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512V (1M X 48 ARRAY)

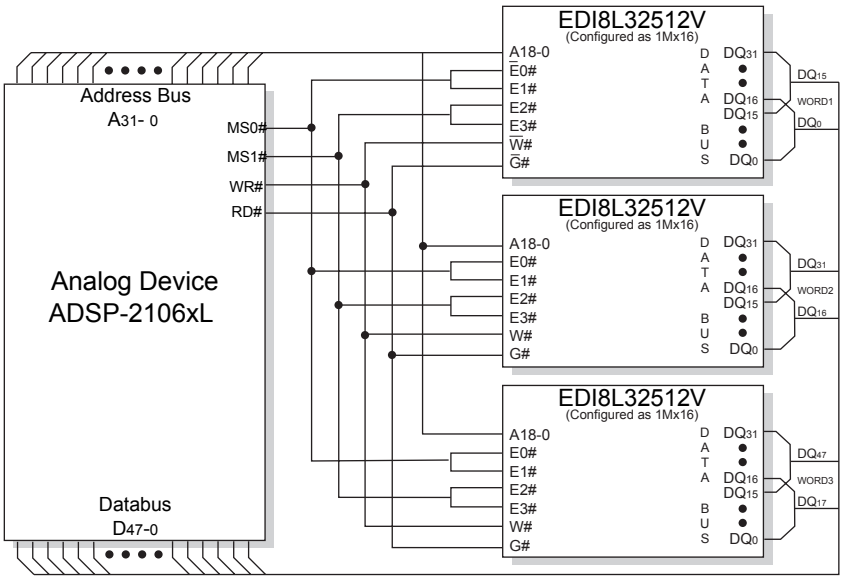


FIG 8.

MCM-L UPGRADE PATH

512Kx32 8L32512V

256Kx32 8L32256V

128Kx32 8L32128V