



EDI8M8130C/P90/100/120/150

High Performance Megabit SRAM Module

128Kx8 Static RAM CMOS, Module

The EDI8M8130C/P is a 1024K bit CMOS Static RAM Module based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The Military screened product is available in both Standard (C) and Low Power (P) versions.

The EDI8M8130C/P has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. The \bar{E} and S lines perform the chip enable functions that automatically power down the device when proper logic levels are applied.

All inputs and outputs are TTL compatible and operate from a 5V supply. Fully asynchronous, the EDI8M8130C/P requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

Features

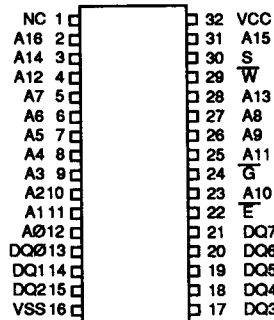
128Kx8 bit CMOS Static Random Access Memory

- Access Times 90, 100, 120 and 150ns
- \bar{E} , S, and \bar{G} Functions for Bus Control
- Data Retention Function
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Jedec Approved Pinout

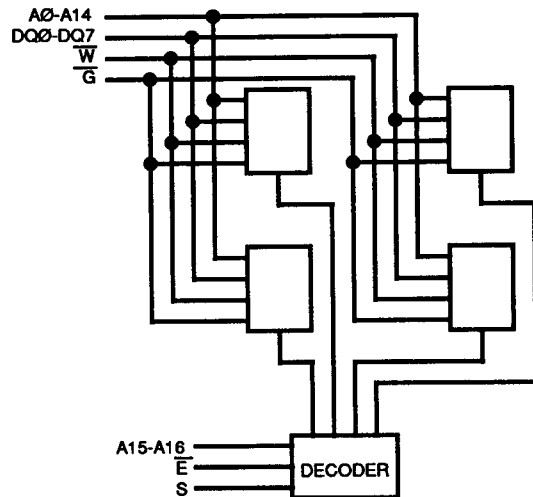
- 32 Pin Ceramic Dual-in-line Package
- Single +5V ($\pm 10\%$) Supply Operation

Pin Configurations and Block Diagram



Pin Names

| | |
|-----------|-------------------------|
| A0-A16 | Address Inputs |
| \bar{E} | Chip Enable |
| S | Chip Select |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| DQ0-DQ7 | Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |



Absolute Maximum Ratings*

Voltage on any pin relative to VSS-0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Commercial0°C to +70°C
 Military-55°C to +125°C
 Storage Temperature (Ambient/Ceramic).....-65°C to +150°C
 Power Dissipation 1 Watt
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

| Parameter | Sym | Conditions | Min | Typ* | Max | Units | |
|------------------------------------|------|--|-----|------|-----|-------|----|
| Operating Power Supply Current | ICC1 | $\bar{W}, \bar{E} = VIL, I/O = 0mA, \text{Min Cycle}$ $S = VIH, \text{Min Cycle}$ | -- | 70 | 95 | mA | |
| Standby (TTL) Power Supply Current | ICC2 | $\bar{E} \geq VIH \text{ or } S \leq VIL$ | -- | 10 | 25 | mA | |
| Full Standby Power Supply Current | ICC3 | $\bar{E} \geq VCC-0.2V \text{ or } S \leq 0.2V$ $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$ | C | -- | 1 | 3 | mA |
| | | | P | -- | 50 | 900 | µA |
| Input Leakage Current | IIL | $VIN = 0V \text{ to } VCC$ | -- | -- | ±10 | µA | |
| Output Leakage Current | IOL | $V I/O = 0V \text{ to } VCC; \bar{E}, \bar{G} = VIH \text{ or } S = VIL$ | -- | -- | ±10 | µA | |
| Output High Voltage | VOH | $I_{OH} = -4.0mA$ | 2.4 | -- | -- | V | |
| Output Low Voltage | VOL | $I_{OL} = 8.0mA$ | -- | -- | 0.4 | V | |

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

| G | \bar{E} | S | \bar{W} | Mode | Output | Power |
|---|-----------|---|-----------|-----------------|--------|------------|
| X | H | X | X | Standby | High Z | ICC2, ICC3 |
| X | X | L | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | H | Output Deselect | High Z | ICC1 |
| L | L | H | H | Read | DOUT | ICC1 |
| X | L | H | L | Write | DIN | ICC1 |

Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-----|------|-----|-----|-------|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | 6.0 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load 1TTL, CL = 30pF
 (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|--|------|-----|------|
| Input Capacitance (Except DQ Pins) | CI | 50 | pF |
| Capacitance Control (DQ Pins) | CD/Q | 43 | pF |
| Input Capacitance Control Lines (\bar{E}, S) | CC | 10 | pF |
| Input Capacitance \bar{W} Line | CW | 50 | pF |

Note: These parameters are sampled, not 100% tested.

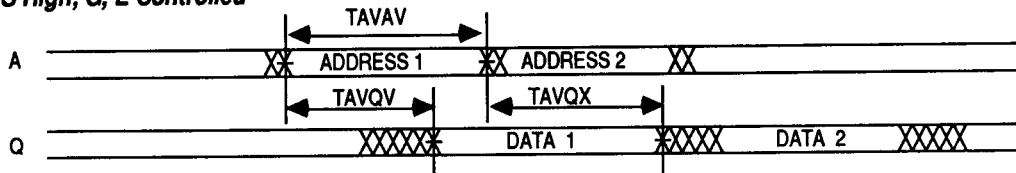
AC Characteristics
Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

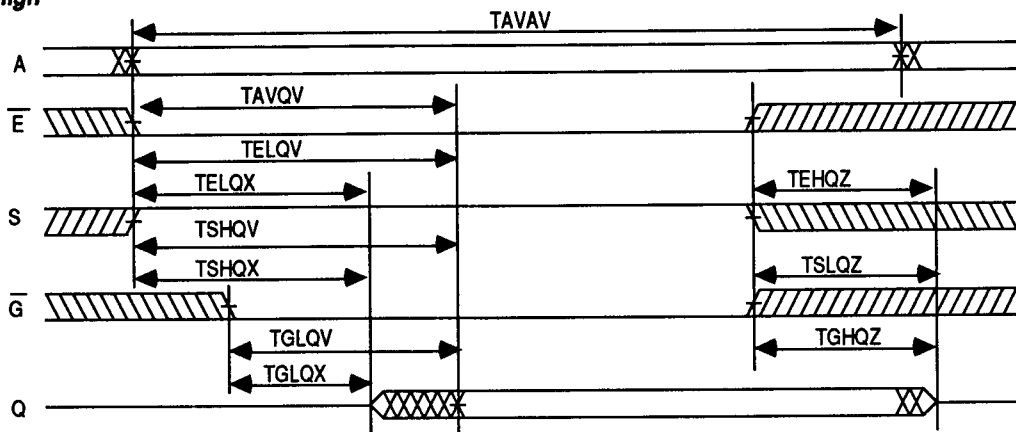
| Parameter | Symbol | 90ns | | 100ns | | 120ns | | 150ns | | Units | |
|--|--------|-----------|-----|-------|-----|-------|-----|-------|-----|-------|----|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | TAVAV | 90 | | 100 | | 120 | | 150 | | ns | |
| Address Access Time | TAVQV | | 90 | | 100 | | 120 | | 150 | ns | |
| Chip Enable Access Time | TELQV | \bar{E} | 90 | | 100 | | 120 | | 150 | ns | |
| | TSHQV | S | 90 | | 100 | | 120 | | 150 | ns | |
| Chip Enable to Output in Low Z (1) | TELQX | \bar{E} | 30 | | 30 | | 30 | | 30 | ns | |
| | TSHQX | S | 30 | | 30 | | 30 | | 30 | ns | |
| Chip Disable to Output in High Z (1) | TEHQZ | \bar{E} | | 30 | | 30 | | 40 | | 50 | ns |
| | TSLQZ | S | | 30 | | 30 | | 40 | | 50 | ns |
| Output Hold from Address Change | TAVQX | | 10 | | 10 | | 10 | | 10 | ns | |
| Output Enable to Output Valid | TGLQV | | | 50 | | 50 | | 60 | | 70 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | | 10 | | 10 | | 10 | | 10 | ns | |
| Output Disable to Output in High Z (1) | TGHQZ | | | 30 | | 30 | | 40 | | 50 | ns |

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W, S High; G, E Controlled



Read Cycle 2
W High



AC Characteristics

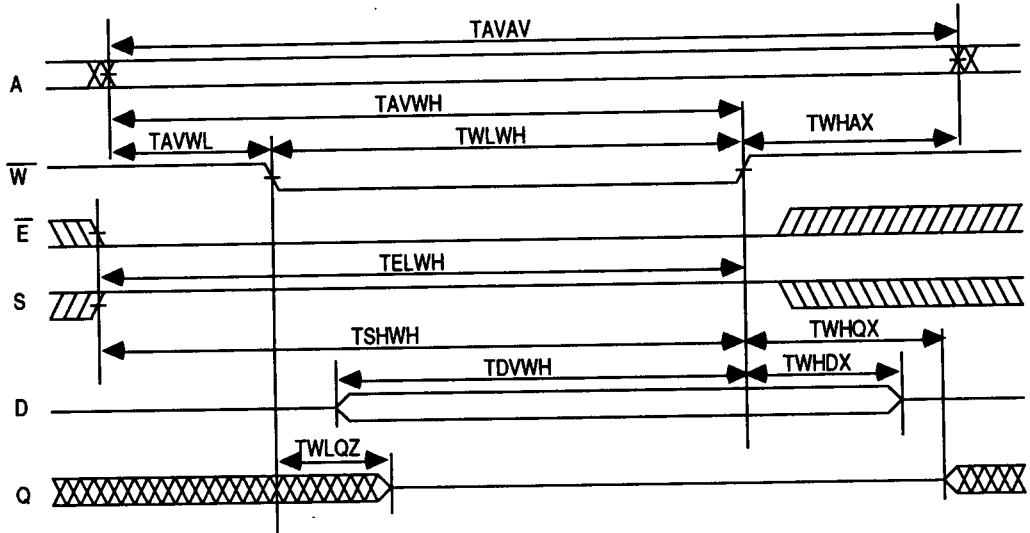
Write Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

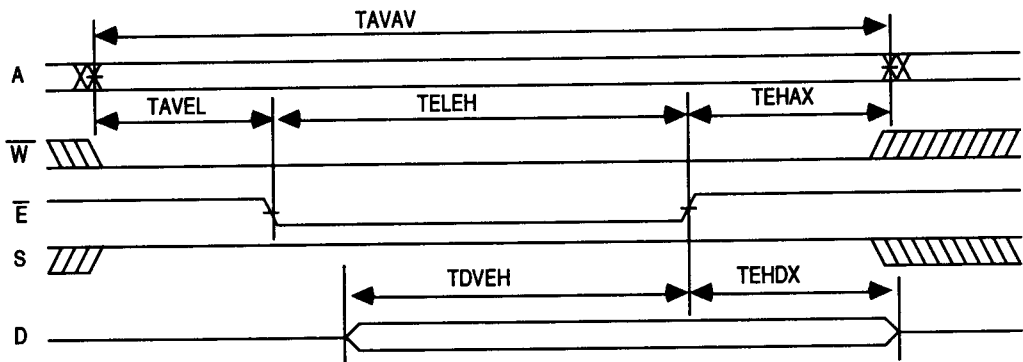
| Parameter | Symbol | | 90ns | | 100ns | | 120ns | | 150ns | | Units |
|--|--------|----------------|------|-----|-------|-----|-------|-----|-------|-----|-------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 90 | | 100 | | 120 | | 150 | | ns |
| Chip Enable to | TELWH | \overline{E} | 80 | | 80 | | 90 | | 110 | | ns |
| End of Write | TSHWH | S | 80 | | 80 | | 90 | | 110 | | ns |
| Address Setup Time | TAVWL | \overline{W} | 20 | | 20 | | 20 | | 20 | | ns |
| | TAVEL | \overline{E} | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVSH | S | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | | 80 | | 80 | | 90 | | 110 | | ns |
| Write Pulse Width | TWLWH | \overline{W} | 60 | | 60 | | 70 | | 80 | | ns |
| | TELEH | \overline{E} | 60 | | 60 | | 70 | | 80 | | ns |
| | TSHSL | S | 60 | | 60 | | 70 | | 80 | | ns |
| Write Recovery Time | TWHAX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| | TSLAX | S | 20 | | 20 | | 20 | | 20 | | ns |
| Data Hold Time | TWHDX | \overline{W} | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHDX | \overline{E} | 20 | | 20 | | 20 | | 20 | | ns |
| | TSLDX | S | 20 | | 20 | | 20 | | 20 | | ns |
| Write to Output in High Z (1) | TWLQZ | | 0 | 35 | 0 | 35 | 0 | 35 | 0 | 45 | ns |
| Data to Write Time | TDVWH | \overline{W} | 35 | | 35 | | 40 | | 50 | | ns |
| | TDVEH | \overline{E} | 35 | | 35 | | 40 | | 50 | | ns |
| | TDVSL | S | 35 | | 35 | | 40 | | 50 | | ns |
| Output Active from End of Write (1) | TWHQX | | 0 | | 0 | | 0 | | 0 | | ns |

Note 1: Parameter guaranteed, but not tested.

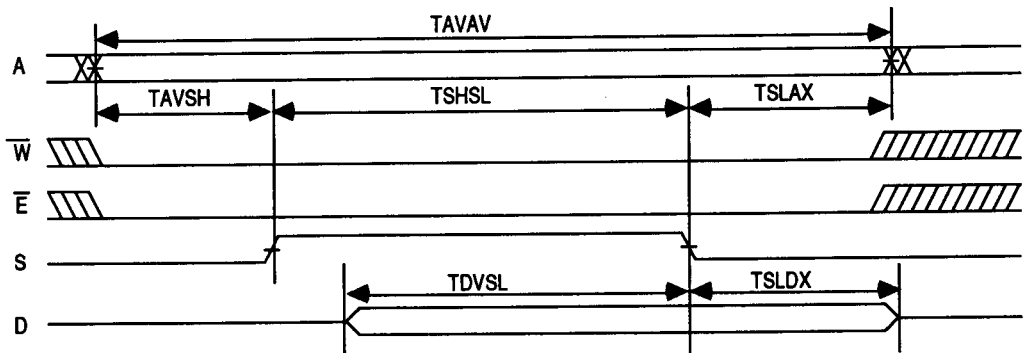
**Write Cycle 1
Late Write, \bar{W} Controlled**



**Write Cycle 2
Early Write, \bar{E} Controlled**



**Write Cycle 3
Early Write, S Controlled**



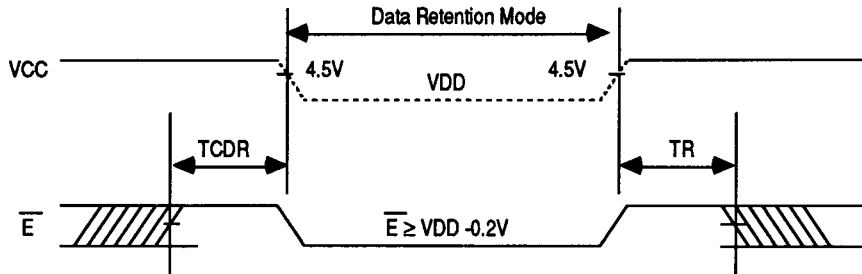
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

| Characteristic | Sym | Test Conditions | Min | Typ | Max | Unit | |
|-------------------------------------|-------|---------------------------|--------|-----|-----|------|---------|
| Data Retention Voltage | VDD | VDD = 2.0V | 2 | -- | -- | V | |
| Data Retention Quiescent Current | ICCDR | $\bar{E} \geq VDD - 0.2V$ | C | -- | 500 | 1500 | μA |
| | | $S \leq 0.2V$ | P | -- | 100 | 500 | μA |
| Chip Disable to Data Retention Time | TCDR | VIN \geq VDD - 0.2V | 0 | -- | -- | ns | |
| Operation Recovery Time | TR | or VIN \leq 0.2V | TAVAV* | -- | -- | ns | |

*Read Cycle Time

Data Retention \bar{E} Controlled



Data Retention S Controlled

