256Kx8 Static RAM CMOS, Module

PRELIMINARY

T-46-23-14

The EDI8M8257C is a 2048K bit CMOS Static RAM based on two 128Kx8 Static RAMs mounted on a multi-layered ceramic substrate.

Functional equivalence to the monolithic two megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address (A17) to select one of the128Kx8 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the two megabit device, to ensure compatibility with future monolithics.

The product is also available with Low Power and Data Retention (EDI8M8257LP).

All inputs and out puts are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8257C requires no clocks or refreshing for operation.

EDI Military Modules are built with RAMs that are compliant to MIL-STD-883, paragraph 1.2.1.

Features

256Kx8 bit CMOS Static Random Access Memory

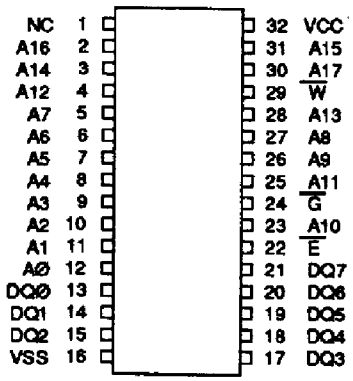
- Access Times:
  - Commercial: 25 thru 150ns
  - Military: 35 thru 150ns
- Data Retention Function (EDI8M8257LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

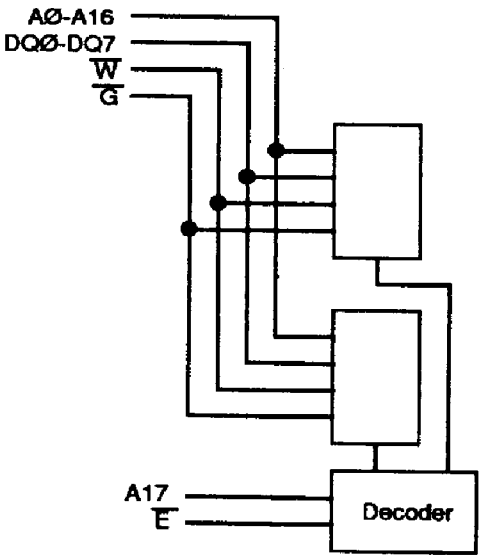
32 pin DIP, JEDEC Approved Pinout

- Ceramic LCCs on Ceramic 1.6" Substrate, No. 155
- Plastic SOJs on Ceramic Substrate, No. 65
- Plastic SOICs on Ceramic Substrate, No. 97

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
- Commercial ..... 0°C to +70°C
- Industrial ..... -40°C to +85°C
- Military ..... -55°C to +125°C

Storage Temperature
- Plastic ..... -55°C to +125°C
- Ceramic ..... -65°C to +150°C

Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions T-46-23-

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load 25-70ns ..... 1TTL, CL = 30pF
85-150ns ..... 1TTL, CL = 100pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Temp Range	Min	Typ*			Max			Units
					25-30	35-70	85-150	25-30	35-70	85-150	ns
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	C/I	--	240	145	70	300	200	130	mA
			Mil	--	--	155	80	--	210	130	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL VIN ≥ VIH	C/I	--	30	25	10	80	60	35	mA
			Mil	--	--	45	20	--	90	40	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	C/I-C		8	5	2	25	10	5	mA
			C/I-LP	--	--	--	40	--	--	400	µA
			Mil-C	--	--	10	5	--	20	10	mA
			Mil-LP	--	--	--	2	--	--	5	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--			±10			µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--			±10			µA
Output High Voltage	VOH	IOH = -1.0mA (≤70ns = -4.0mA)		2.4	--			--			V
Output Low Voltage	VOL	IOL = 2.1mA (≤70ns = 8.0mA)		--	--			0.4			V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	30	pF
Chip Enable Line	CC	20	pF
Write and Output Enable Lines	CW	30	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

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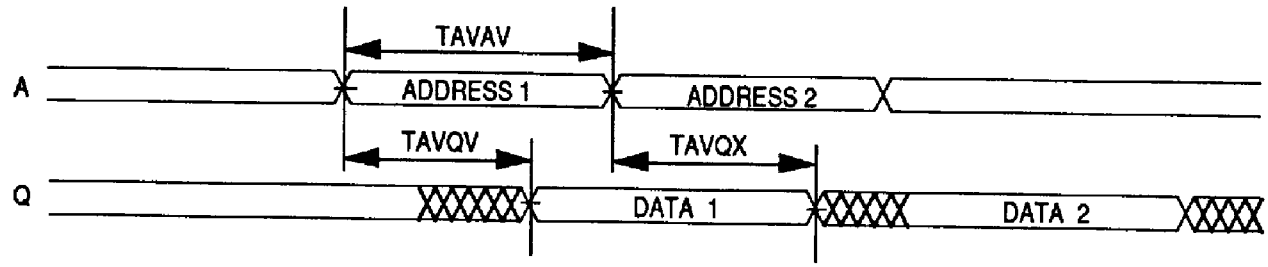
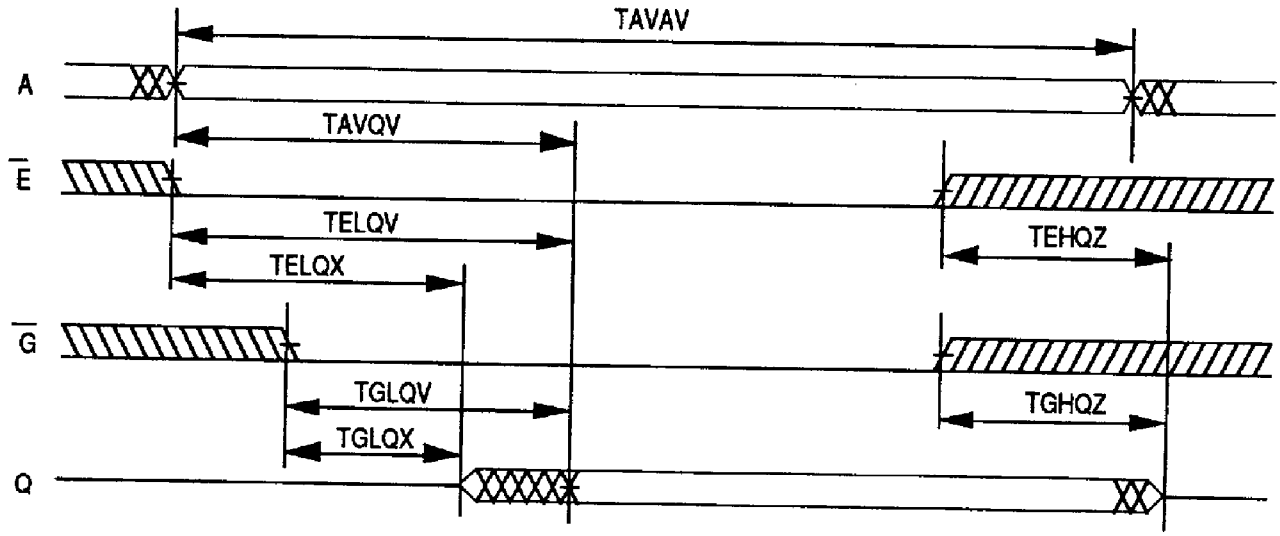
Parameter	Symbol		25ns		30ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	25		30		35		45		55		ns
Address Access Time	TAVQV	TAA		25		30		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		25		30		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		12		15		20		25		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		10		10		15		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		10		12		20		25		25	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Read Cycle

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Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	70		85		100		120		150		ns
Address Access Time	TAVQV	TAA		70		85		100		120		150	ns
Chip Enable Access Time	TELQV	TACS		70		85		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		25		35		40		45		50	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		25		45		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		25		35		40		45		50	ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

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Parameter	Symbol		25ns		30ns		35ns		45ns		55ns		
	JEDEC	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	25		30		35		45		55		ns
Chip Enable to End of Write	TELWH	TCW	20		25		30		35		40		ns
	TELEH	TCW	20		25		30		35		40		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	20		25		30		35		40		ns
	TAVEH	TAW	20		25		30		35		40		ns
Write Pulse Width	TWLWH	TWP	20		20		25		35		40		ns
	TWLEH	TWP	20		20		25		35		40		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	15	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	TDW	12		15		15		25		25		ns
	TDVEH	TDW	12		15		15		25		25		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

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Parameter	Symbol		70ns		85ns		100ns		120ns		150ns		
	JEDEC	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	70		85		100		120		150		ns
Chip Enable to End of Write	TELWH	TCW	45		70		80		100		110		ns
	TELEH	TCW	45		70		80		100		110		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	45		70		80		100		110		ns
	TAVEH	TAW	45		70		80		100		110		ns
Write Pulse Width	TWLWH	TWP	45		70		80		100		110		ns
	TWLEH	TWP	45		70		80		100		110		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	25	0	35	0	40	0	45	0	50	ns
Data to Write Time	TDVWH	TDW	30		35		40		45		50		ns
	TDVEH	TDW	30		35		40		45		50		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

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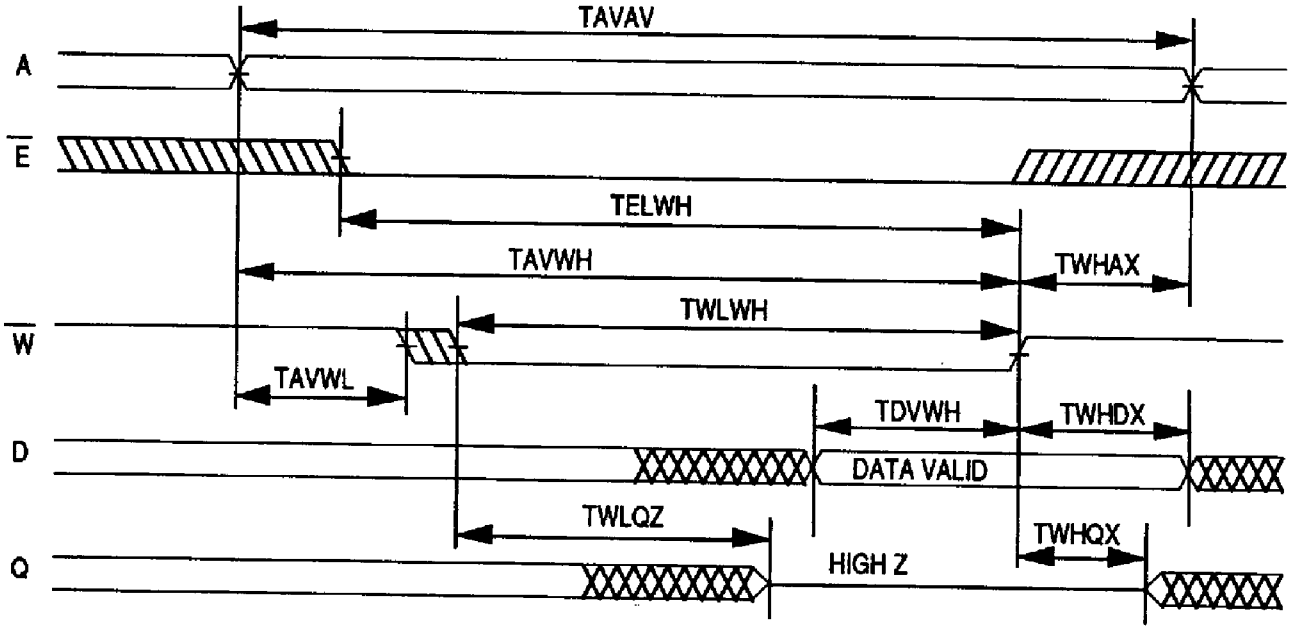
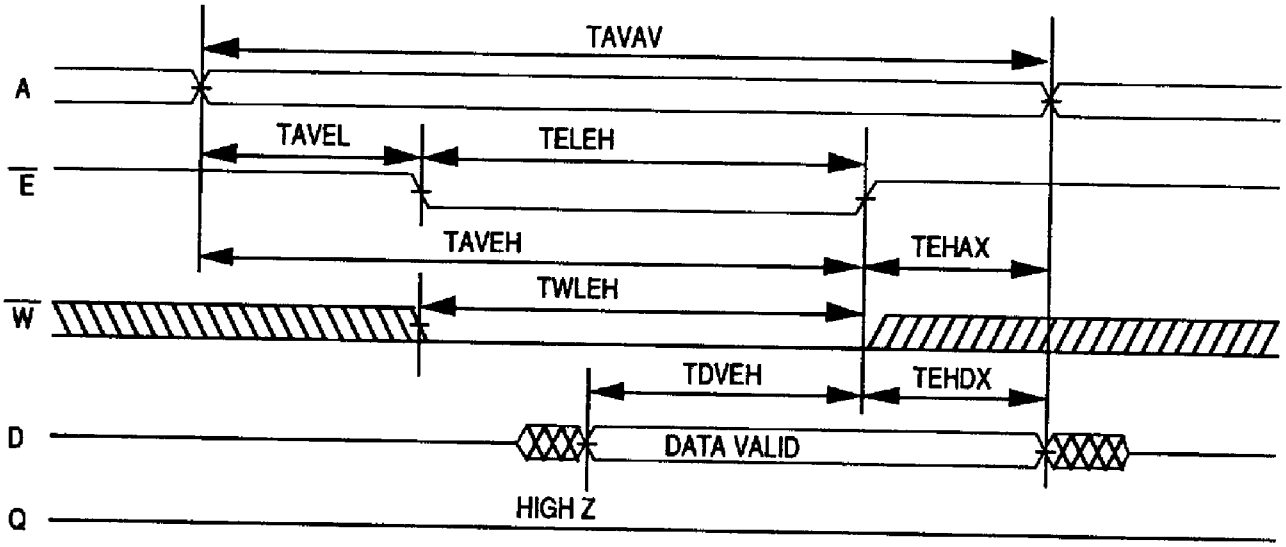
Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



Data Retention Characteristics

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max			Unit
						70°C	85°C	125°C	
Data Retention Voltage	VDD	$\overline{E} \geq$ VDD -0.2V VIN ≥VDD -0.2V or VIN ≤0.2V		2	--	--	--	--	V
Data Retention Quiescent Current	ICCDR		2V	--	10	125	185	850	µA
			3V	--	20	200	250	1100	µA
Chip Disable to Data Retention Time	TCDR			0		--	--	--	ns
Operation Recovery Time	TR			5		--	--	--	ms

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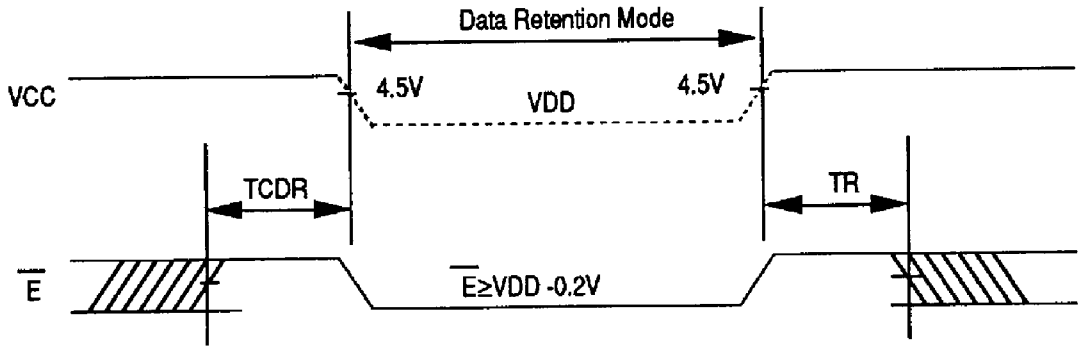
Data Retention
$\overline{E}$ Controlled



Ordering Information

Commercial

Standard Power Part No.	Speed (ns)	Leads	Package Style	No.
EDI8M8257C25M6C	25	32	0.6 DIP	65
EDI8M8257C30M6C	30	32	0.6 DIP	65
EDI8M8257C35M6C	35	32	0.6 DIP	65
EDI8M8257C45M6C	45	32	0.6 DIP	65
EDI8M8257C55M6C	55	32	0.6 DIP	65
EDI8M8257C70M6C	70	32	0.6 DIP	65
EDI8M8257C85P6C	85	32	0.6 DIP	97
EDI8M8257C100P6C	100	32	0.6 DIP	97
EDI8M8257C120P6C	120	32	0.6 DIP	97
EDI8M8257C150P6C	150	32	0.6 DIP	97
Low Power with Data Retention				
EDI8M8257LP85P6C	85	32	0.6 DIP	97
EDI8M8257LP100P6C	100	32	0.6 DIP	97
EDI8M8257LP120P6C	120	32	0.6 DIP	97
EDI8M8257LP150P6C	150	32	0.6 DIP	97

Military

Standard Power Part No.	Speed (ns)	Leads	Package Style	No.
EDI8M8257C35C6B	35	32	0.6 DIP	155
EDI8M8257C45C6B	45	32	0.6 DIP	155
EDI8M8257C55C6B	55	32	0.6 DIP	155
EDI8M8257C70C6B	70	32	0.6 DIP	155
EDI8M8257C85C6B	85	32	0.6 DIP	155
EDI8M8257C100C6B	100	32	0.6 DIP	155
EDI8M8257C120C6B	120	32	0.6 DIP	155
EDI8M8257C150C6B	150	32	0.6 DIP	155
Low Power with Data Retention				
EDI8M8257LP85C6B	85	32	0.6 DIP	155
EDI8M8257LP100C6B	100	32	0.6 DIP	155
EDI8M8257LP120C6B	120	32	0.6 DIP	155
EDI8M8257LP150C6B	150	32	0.6 DIP	155