

**OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT**
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

December 1995, Rev. C

FN7047

85MHz Current Feedback Amplifier



The EL2130 is a wideband current mode feedback amplifier optimized for gains between -10 and +10 while

operating on $\pm 5V$ power supplies. Built using Elantec's Complementary Bipolar process, this device exhibits -3dB bandwidths in excess of 85MHz at unity gain and 75MHz at a gain of two. The EL2130 is capable of output currents in excess of 50mA giving it the ability to drive either double or single terminated 50 Ω coaxial cables.

Exhibiting a Differential Gain of 0.03% and a Differential Phase of 0.1 $^\circ$ at NTSC and PAL frequencies, the EL2130 is an excellent low cost solution to most video applications.

In addition, the EL2130 exhibits very low gain peaking, typically below 0.1dB to frequencies in excess of 40MHz as well as 50ns settling time to 0.2% making it an excellent choice for driving flash A/D converters.

The device is available in the plastic 8-pin narrow-body small outline (SO) and the 8-pin mini DIP packages, and operates over the temperature range of 0 $^\circ C$ to +75 $^\circ C$

Features

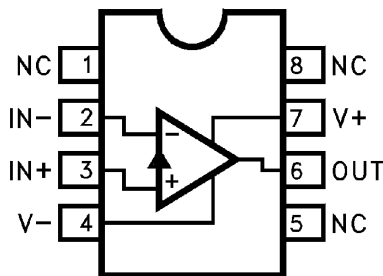
- -3dB bandwidth = 85MHz, $A_V = 1$
- -3dB bandwidth = 75MHz, $A_V = 2$
- NTSC/PAL dG $\leq 0.03\%$, dP $\leq 0.1^\circ$
- 50mA output current
- Drives $\pm 2.5V$ into 100 Ω load
- Low voltage noise = 4nV \sqrt{Hz}
- Current mode feedback
- Low cost

Applications

- Video amplifier
- Video distribution amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coaxial cable driver

Pinout

**EL2130
(8-PIN PDIP, SO)
TOP VIEW**



Manufactured under U.S. Patent No. 4,893,091.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2130CN	0 $^\circ C$ to +75 $^\circ C$	8-Pin PDIP	MDP0031
EL2130CS	0 $^\circ C$ to +75 $^\circ C$	8-Pin SO	MDP0027

EL2130

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

V_S	Supply Voltage	$\pm 6\text{V}$
V_{IN}	Input Voltage	$\pm V_S$
ΔV_{IN}	Differential Input Voltage	$\pm 6\text{V}$
P_D	Maximum Power Dissipation	See Curves

I_{IN}	Input Current	$\pm 10\text{mA}$
I_{OP}	Output Short Circuit Duration	$\leq 5\text{ sec}$
T_A	Operating Temperature Range	0°C to $+75^\circ\text{C}$
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	-65°C to $+150^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

$V_S = \pm 5\text{V}$; $R_L = \infty$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		25°C		2.0	10	mV
			T_{MIN}, T_{MAX}			15	mV
V_{OS}/T	Offset Voltage Drift				7		$\mu\text{V}/^\circ\text{C}$
$+I_{IN}$	+Input Current		25°C		5.5	15	μA
			T_{MIN}, T_{MAX}			25	μA
$-I_{IN}$	+Input Current		25°C		10	40	μA
			T_{MIN}, T_{MAX}			50	μA
$+R_{IN}$	+Input Resistance		25°C	1.0	2.0		$\text{M}\Omega$
C_{IN}	+Input Capacitance		25°C		1.0		pF
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 2.5\text{V}$	25°C	50	60		dB
$-ICMR$	Input Current Common Mode Rejection	$V_{CM} = \pm 2.5\text{V}$	25°C		5	10	$\mu\text{A}/\text{V}$
			T_{MIN}, T_{MIN}			20	$\mu\text{A}/\text{V}$
PSRR	Power Supply Rejection Ratio	$\pm 4.5\text{V} \leq V_S \leq \pm 6\text{V}$	25°C	60	70		dB
$+IPSR$	+Input Current Power Supply Rejection	$\pm 4.5\text{V} \leq V_S \leq \pm 6\text{V}$	25°C		0.1	0.5	$\mu\text{A}/\text{V}$
			T_{MIN}, T_{MIN}			1.0	$\mu\text{A}/\text{V}$
$-IPSR$	-Input Current Power Supply Rejection	$\pm 4.5\text{V} \leq V_S \leq \pm 6\text{V}$	25°C		0.5	5.0	$\mu\text{A}/\text{V}$
			T_{MIN}, T_{MIN}			8.0	$\mu\text{A}/\text{V}$
R_{OL}	Transimpedance	$V_{OUT} = \pm 2.5\text{V}$, $R_L = 100\Omega$	25°C	80	145		V/mA
			T_{MIN}, T_{MAX}	70			V/mA
A_{VOL}	Open Loop DC Voltage Gain	$V_{OUT} = \pm 2.5\text{V}$, $R_L = 100\Omega$	25°C	60	66		dB
			T_{MIN}, T_{MAX}	56			dB
V_O	Output Voltage Swing	$R_L = 100\Omega$	25°C	3	3.5		V
I_{OUT}	Output Current		25°C	30	50		mA
R_{OUT}	Output Resistance		25°C		5		Ω
I_S	Quiescent Supply Current		Full		17	21	mA
I_{SC}	Short Circuit Current		25°C		85		mA

EL2130

Closed-Loop AC Electrical Specifications

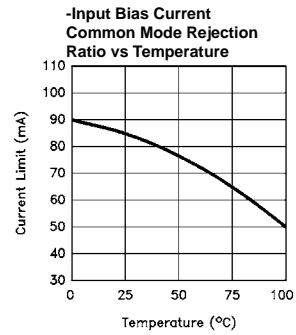
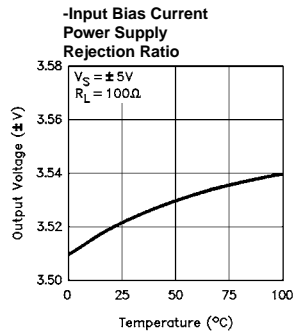
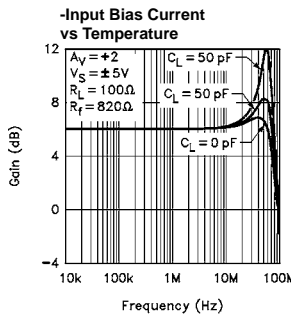
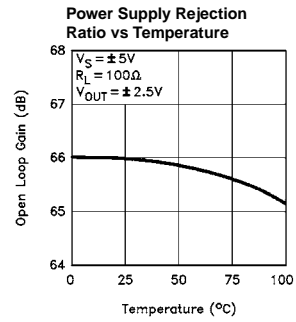
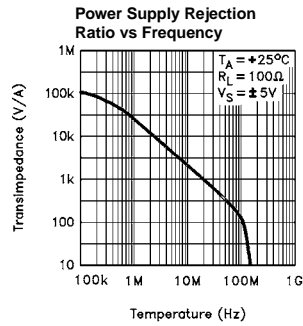
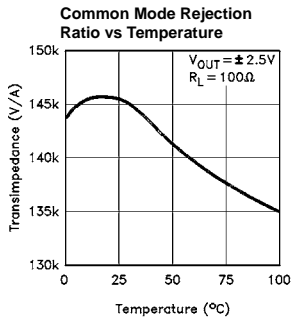
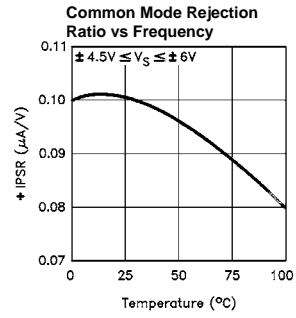
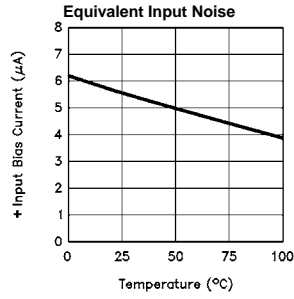
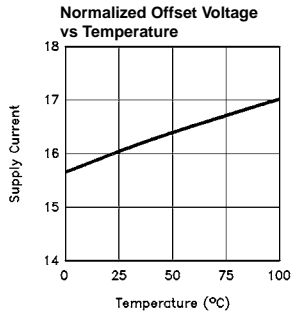
$V_S = \pm 5V$, $A_V = +2$, $R_F = R_G = 820\Omega$, $R_L = 100\Omega$, $T_A = 25^\circ C$

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
SR	Slew Rate (Note 1)	$V_O = 5V_{P-P}$		625		V/ μs
t_R	Rise Time	$V_O = 200mV$		4.6		ns
t_F	Fall Time	$V_O = 200mV$		4.6		ns
t_{PD}	Prop Delay	$V_O = 200mV$		4.0		ns
SSBW	3dB Bandwidth	$V_O = 100mV$		75		MHz
dG	NTSC/PAL Diff Gain			0.03		%
dP	NTSC/PAL Diff Phase			0.10		deg ($^\circ$)
GFPL	Gain Flatness	$f < 40MHz$		0.08		dB

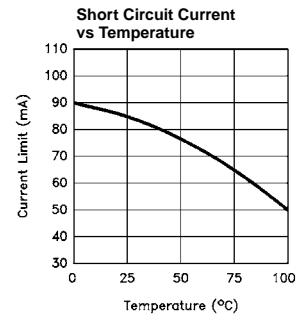
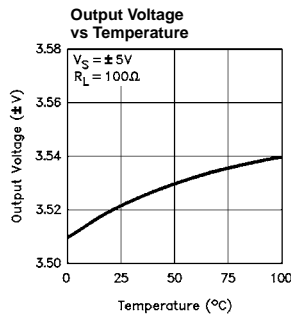
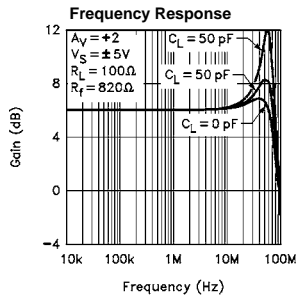
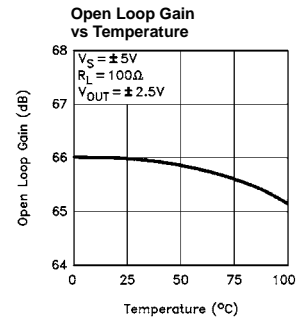
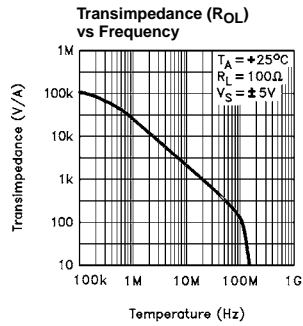
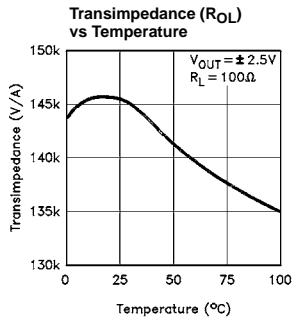
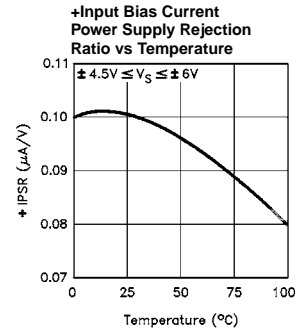
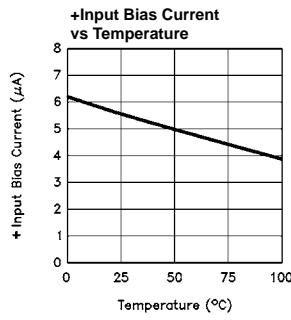
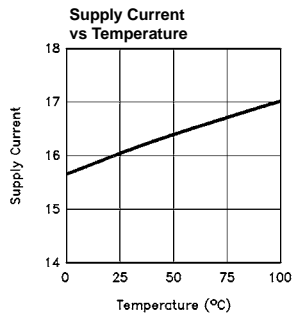
NOTE:

1. Slew rate is measured with $V_O = 5V_{P-P}$ between -1.25V and +1.25V and +1.25V and -1.25V.

Typical Performance Curves

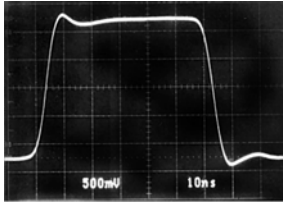


Typical Performance Curves (Continued)



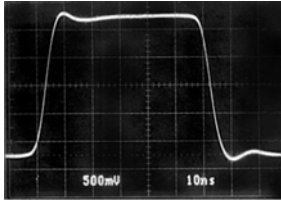
Typical Performance Curves (Continued)

Large Signal Response



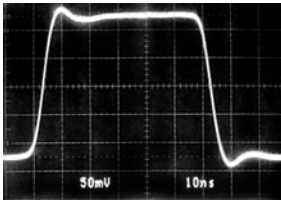
$A_V = +1$, $R_F = 820\Omega$
 $R_L = 100\Omega$, $C_L = 12pF$

Large Signal Response



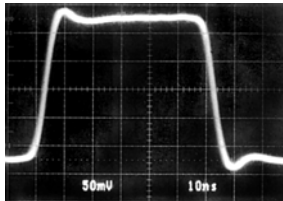
$A_V = +2$, $R_F = 820\Omega$
 $R_L = 100\Omega$, $C_L = 12pF$

Small Signal Response



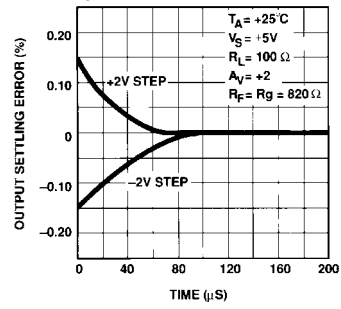
$A_V = +1$, $R_F = 820\Omega$
 $R_L = 100\Omega$, $C_L = 12pF$

Small Signal Response

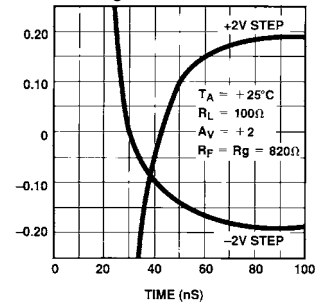


$A_V = +2$, $R_F = 820\Omega$
 $R_L = 100\Omega$, $C_L = 12pF$

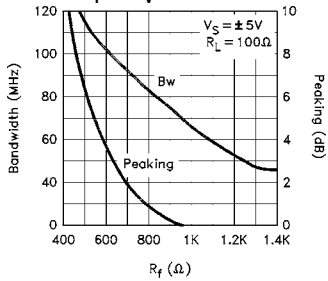
Long-Term Output Settling Error vs Time, $V_S = \pm 5V$



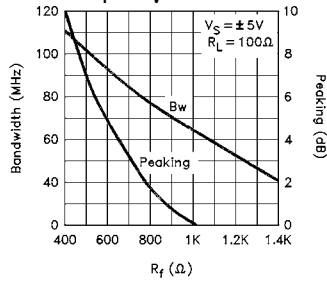
Short Term Output Settling Error vs Time, $V_S = \pm 5V$



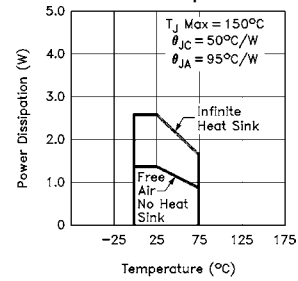
Bandwidth and Peaking vs R_F for $A_V = +1$



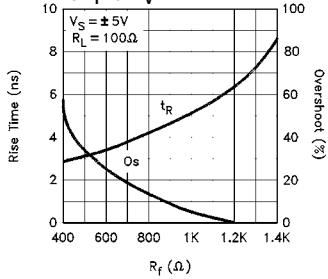
Bandwidth and Peaking vs R_F for $A_V = +2$



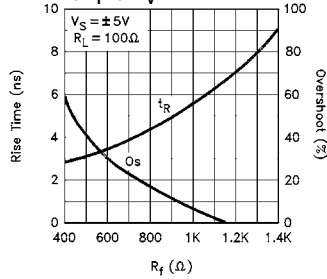
8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



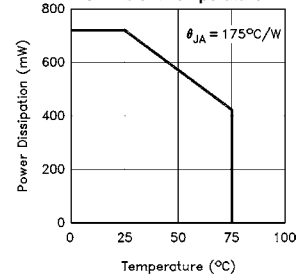
Rise Time and Overshoot vs R_F for $A_V = +1$



Rise Time and Overshoot vs R_F for $A_V = +2$



8-Pin SO Maximum Power Dissipation vs Ambient Temperature



Applications Information

Power Supply Bypassing

The EL2130 will exhibit ringing or oscillation if the power supply leads are not adequately bypassed. 0.1 μ F ceramic disc capacitors are suggested for both supply pins at a distance no greater than 1/2 inch from the device. Surface mounting chip capacitors are strongly recommended.

Lead Dress

A ground plane to which decoupling capacitors and gain setting resistors are terminated will eliminate overshoot and ringing. However, the ground plane should not extend to the vicinity of both the non-inverting and inverting inputs (pins 3 and 2) which would add capacitance to these nodes, and lead lengths from these pins should be made as short as possible.

Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Video Characteristics and Applications

Frequency domain testing is performed at Elantec using a computer controlled HP model 8656B Signal Generator and an HP Model 4195A Network/Spectrum Analyzer. The DUT test board is built using microwave/strip line techniques, and solid coaxial cables route the stimulus to the DUT socket. Signals are routed to and from the DUT test fixture using subminiature coaxial cable.

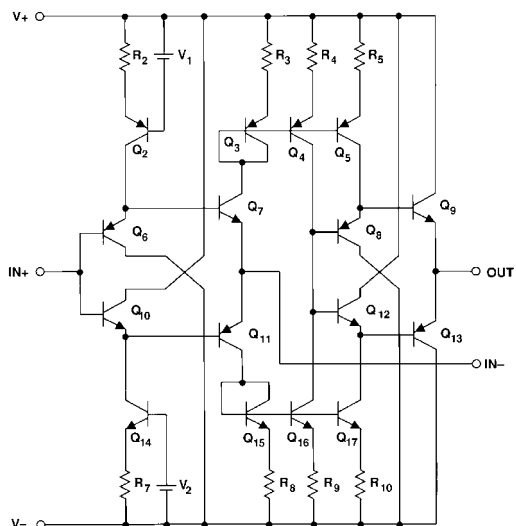
Differential Gain and Phase are tested at a noise gain of 2 with 100 Ω load. Gain and Phase measurements are made with a DC input reference voltage at 0V and compared to those made at V_{REF} equal to 0.7V at frequencies extending to 30MHz.

The EL2130 is capable of driving 100 Ω to a minimum of 2.5V peak which means that it can naturally drive double terminated (50 Ω) coaxial cables.

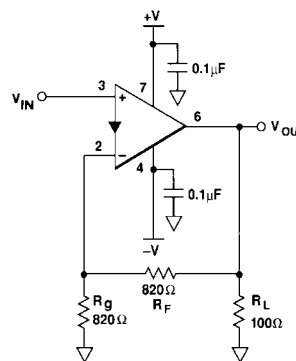
Capacitive Loads

As can be seen from the Bode plot, the EL2130 will peak into capacitive loads greater than 20pF. In many applications such as flash A/Ds, capacitive loading is unavoidable. In these cases, the use of a snubber network consisting of a 100 Ω resistor in series with 47pF capacitor from the output to ground is recommended.

Equivalent Circuit



AC Test Circuit



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com