High Performance Pin Driver

The EL7156 high performance pin driver with 3-state is suited to many ATE and level-shifting applications. The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads.

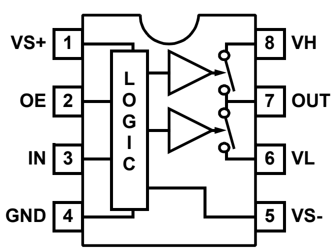
The output pin OUT is connected to input pins V_H or V_L respectively, depending on the status of the IN pin. When the OE pin is active low, the output is placed in the 3-state mode. The isolation of the output FETs from the power supplies enables V_H and V_L to be set independently, enabling level-shifting to be implemented. Related to the EL7155, the EL7156 adds a lower supply pin V_S- and makes V_L an isolated and independent input. This feature adds applications flexibility and improves switching response due to the increased enhancement of the output FETs.

This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and on-resistance characteristics.

Available in the 8 Ld SO and 8 Ld PDIP packages, the EL7156 is specified for operation over the full -40°C to +85°C temperature range.

Pinout

EL7156
(8 LD PDIP, SO)
TOP VIEW



Features

- Clocking speeds up to 40MHz
- 15ns tr/tf at 2000pF C_{LOAD}
- 0.5ns rise and fall times mismatch
- 0.5ns T_{ON}-T_{OFF} prop delay mismatch
- 3.5pF typical input capacitance
- 3.5A peak drive
- Low on resistance of 3.5Ω
- High capacitive drive capability
- Operates from 4.5V to 16.5V
- Pb-free plus anneal available (RoHS compliant)

Applications

- ATE/burn-in testers
- Level shifting
- IGBT drivers
- CCD drivers

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL7156CN	EL7156CN	-	8 Ld PDIP	MDP0031
EL7156CNZ (Note)	EL7156CNZ	-	8 Ld PDIP* (Pb-free)	MDP0031
EL7156CS	7156CS	-	8 Ld SO	MDP0027
EL7156CS-T7	7156CS	7"	8 Ld SO	MDP0027
EL7156CS-T13	7156CS	13"	8 Ld SO	MDP0027
EL7156CSZ (Note)	7156CSZ	-	8 Ld SO (Pb-free)	MDP0027
EL7156CSZ-T7 (Note)	7156CSZ	7"	8 Ld SO (Pb-free)	MDP0027
EL7156CSZ-T13 (Note)	7156CSZ	13"	8 Ld SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ to V_S-) . . . .+18V
Input Voltage . . . . V_S- -0.3V, V_S +0.3V
Continuous Output Current 200mA
Storage Temperature Range . . . .-65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C
Operating Junction Temperature . . . . 125°C
Power Dissipation . . . . see curves

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_H = +15V, V_L = 0V, V_S- = 0V, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic ‘1’ Input Voltage		2.4			V
I_{IH}	Logic ‘1’ Input Current	$V_{IH} = V_S+$		0.1	10	µA
V_{IL}	Logic ‘0’ Input Voltage				0.8	V
I_{IL}	Logic ‘0’ Input Current	V_{IL} = 0V		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OVH}	ON Resistance V_H to OUT	I_{OUT} = -200 mA		2.7	4.5	Ω
R_{OVL}	ON Resistance V_L to OUT	I_{OUT} = +200 mA		3.5	5.5	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUT = V_H/V_L		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		1.3	3	mA
I_{VH}	Off Leakage at V_H and V_L	V_H, V_L = 0V		4	10	µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	C_L = 2000pF		14.5		ns
t_F	Fall Time	C_L = 2000pF		15		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 2000pF		0.5		ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000pF		9.5		ns
t_{D-2}	Turn-On Delay Time	C_L = 2000pF		10		ns
$t_{D\Delta}$	t_{D-1}-t_{D-2} Mismatch	C_L = 2000pF		0.5		ns
t_{D-3}	3-state Delay Enable			10		ns
t_{D-4}	3-state Delay Disable			10		ns

Electrical Specifications

$V_S+ = +5V$, $V_H = +5V$, $V_L = -5V$, $V_S- = -5V$, $T_A = 25°C$, unless otherwise specified

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{IH}	Logic '1' Input Voltage		2.0			V
I_{IH}	Logic '1' Input Current	$V_{IH} = V_S+$		0.1	10	µA
V_{IL}	Logic '0' Input Voltage				0.8	V
I_{IL}	Logic '0' Input Current	$V_{IL} = 0V$		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
OUTPUT						
R_{OVH}	ON Resistance V_H to OUT	$I_{OUT} = -200mA$		3.4	5	Ω
R_{OVL}	ON Resistance V_L to OUT	$I_{OUT} = +200mA$		4	6	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUT = V_H/V_L		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_S+		1	2.5	mA
V_H	Off Leakage at V_H and V_L	V_H, $V_L = 0V$		4	10	µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	$C_L = 2000pF$		17		ns
t_F	Fall Time	$C_L = 2000pF$		17		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	$C_L = 2000pF$		0		ns
t_{D-1}	Turn-Off Delay Time	$C_L = 2000pF$		11.5		ns
t_{D-2}	Turn-On Delay Time	$C_L = 2000pF$		12		ns
$t_{D\Delta}$	t_{D-1}-t_{D-2} Mismatch	$C_L = 2000pF$		0.5		ns
t_{D-3}	3-state Delay Enable			10		ns
t_{D-4}	3-state Delay Disable			10		ns

Typical Performance Curves

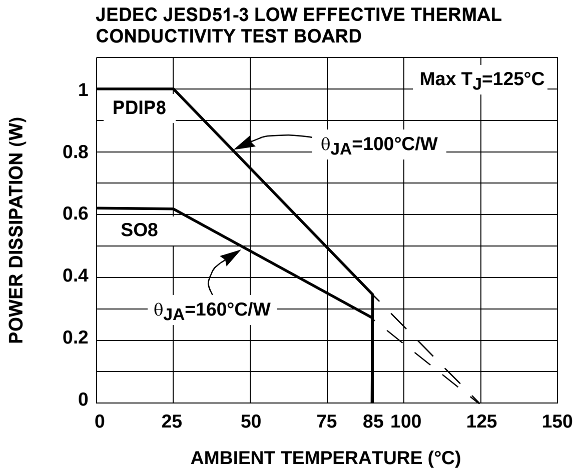


FIGURE 1. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

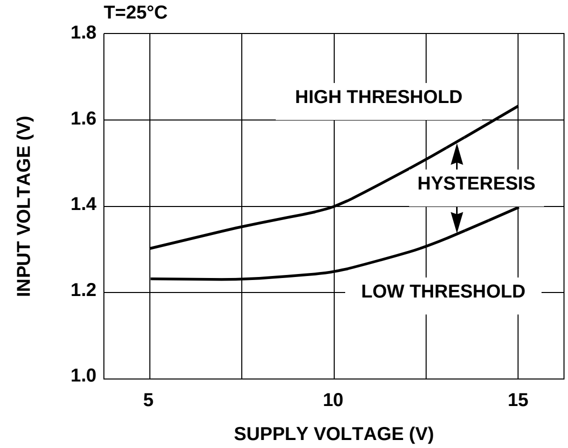


FIGURE 2. INPUT THRESHOLD vs SUPPLY VOLTAGE

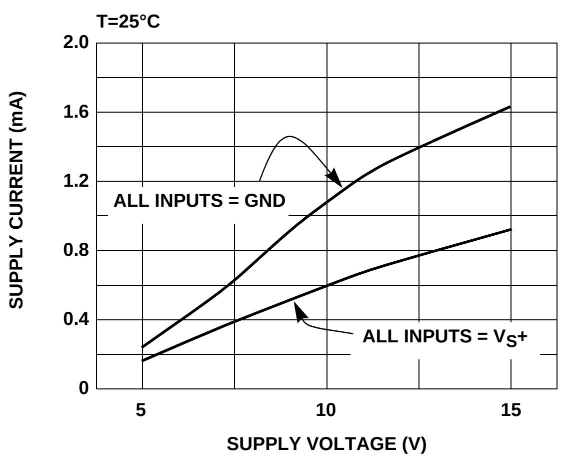


FIGURE 3. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

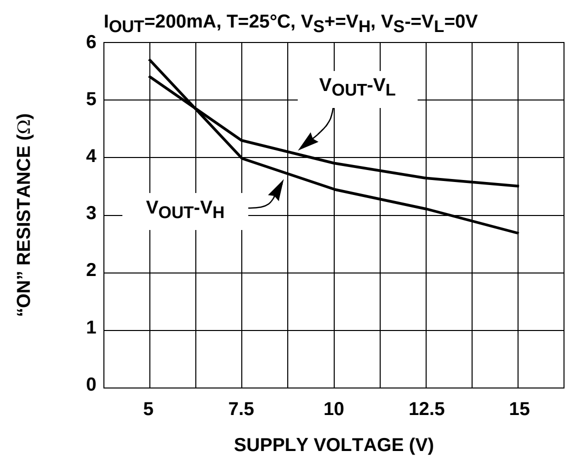


FIGURE 4. "ON" RESISTANCE vs SUPPLY VOLTAGE

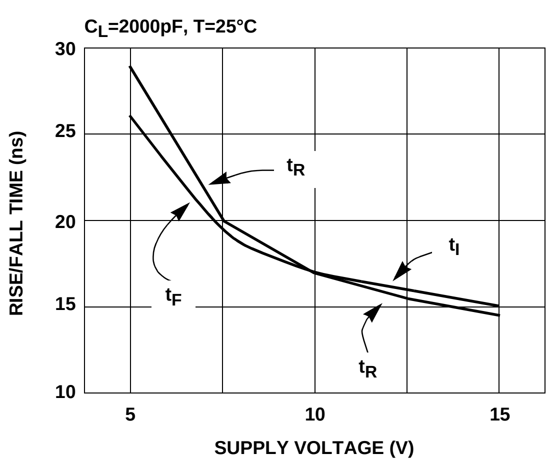


FIGURE 5. RISE/FALL TIME vs SUPPLY VOLTAGE

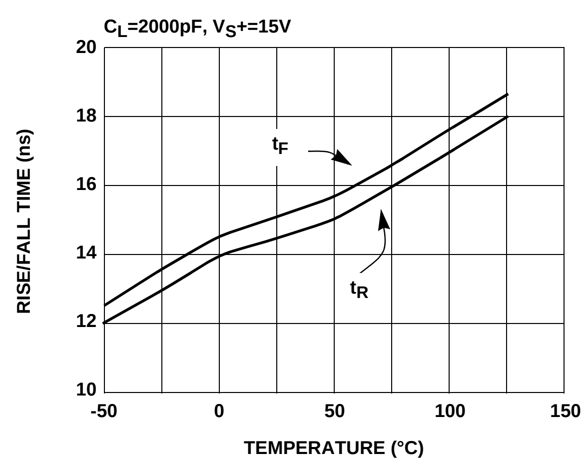


FIGURE 6. RISE/FALL TIME vs TEMPERATURE

Typical Performance Curves (Continued)

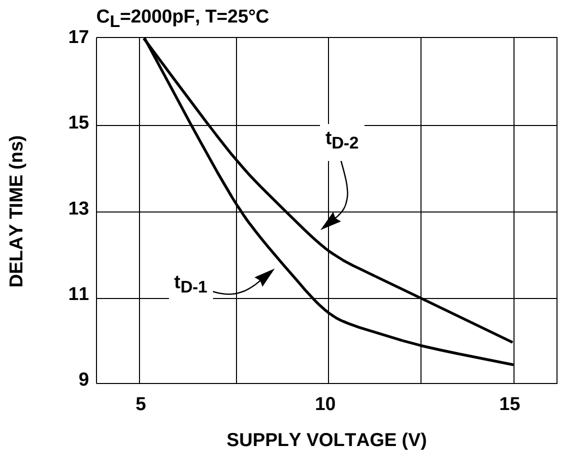


FIGURE 7. PROPAGATION DELAY vs SUPPLY VOLTAGE

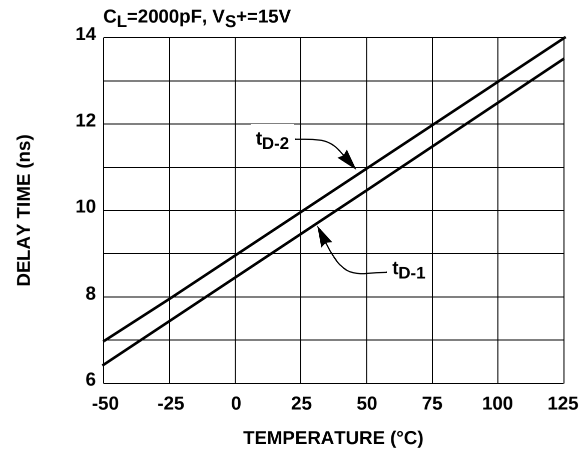


FIGURE 8. PROPAGATION DELAY vs TEMPERATURE

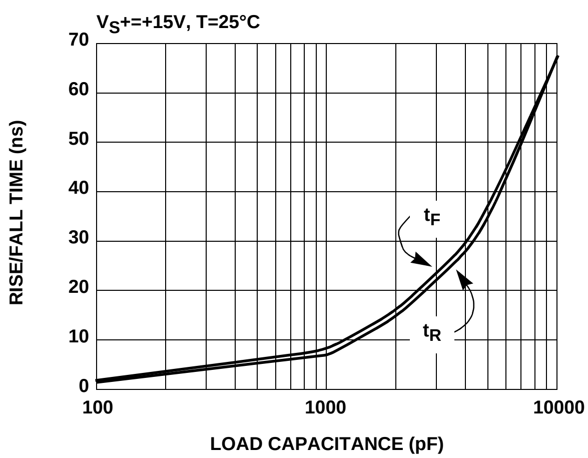


FIGURE 9. RISE/FALL TIME vs LOAD CAPACITANCE

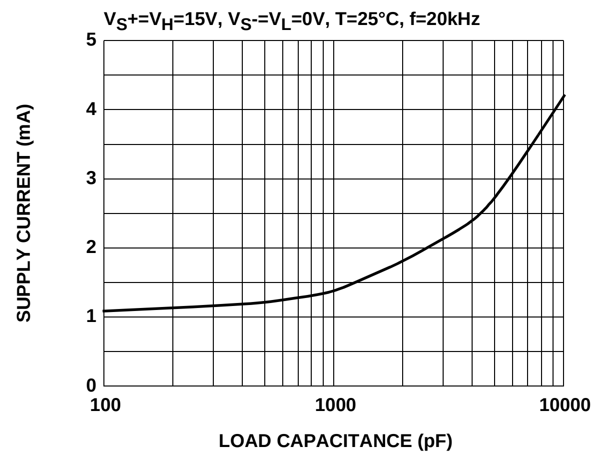


FIGURE 10. SUPPLY CURRENT vs LOAD CAPACITANCE

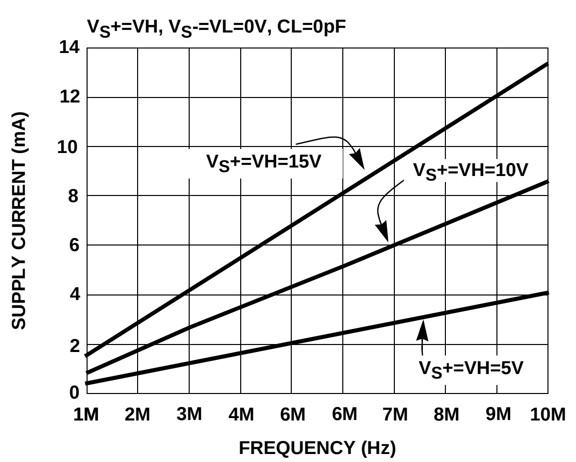


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

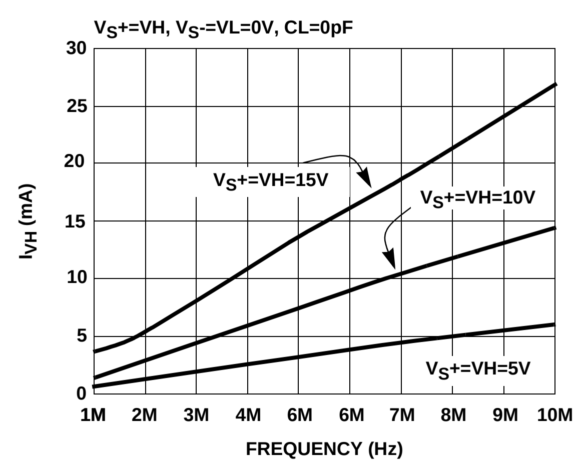


FIGURE 12. V_H SUPPLY CURRENT vs FREQUENCY

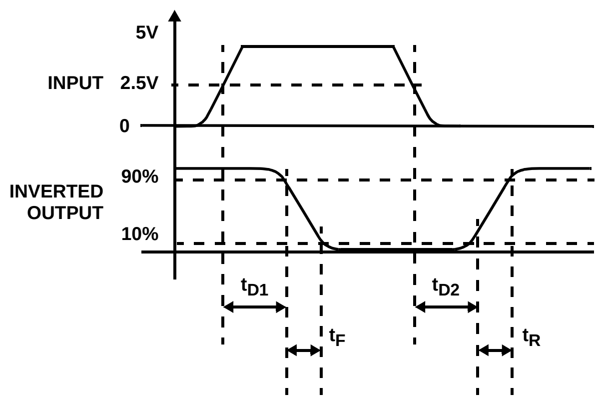
Truth Table

OE	IN	OUT
0	0	3-state
0	1	3-state
1	0	V_H
1	1	V_L

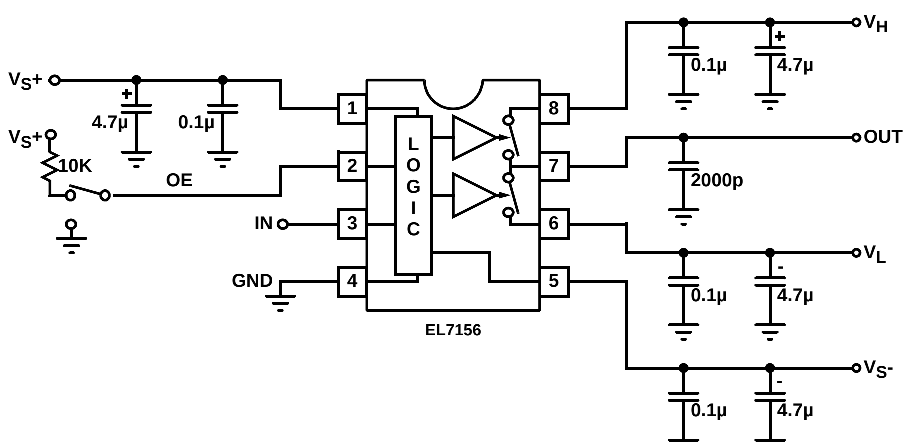
Operating Voltage Range

PIN	MIN	MAX
GND - V_S-	-5	0
V_S+ - V_S-	5	16.5
V_H - V_L	0	16.5
V_S+ - V_H	0	16.5
V_S+ - GND	5	16.5
V_L - V_S-	0	16.5
3-state Output	V_L	V_H

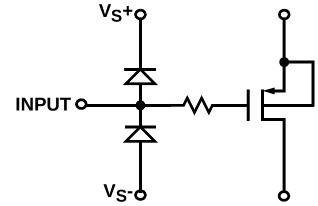
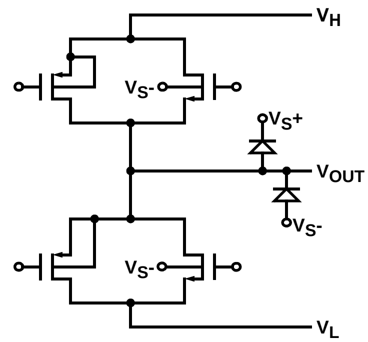
Timing Diagram



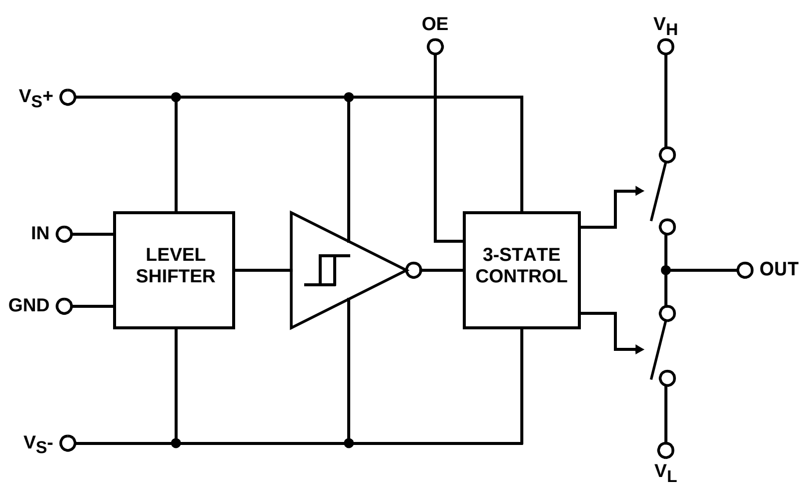
Standard Test Configuration



Pin Descriptions

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VS+	Positive Supply Voltage	
2	OE	Output Enable	 CIRCUIT 1
3	IN	Input	Reference Circuit 1
4	GND	Ground	
5	VS-	Negative Supply Voltage	
6	VL	Lower Output Voltage	
7	OUT	Output	 CIRCUIT 2
8	VH	High Output Voltage	

Block Diagram



Applications Information

Product Description

The EL7156 is a high performance 40MHz pin driver. It contains two analog switches connecting V_H and V_L to OUT. Depending on the value of the IN pin, one of the two switches will be closed and the other switch open. An output enable (OE) is also supplied which opens both switches simultaneously.

Due to the topology of the EL7156, both the V_H and V_L pins can be connected to any voltage between the V_S+ and V_S- pins, but V_H must be greater than V_L in order to prevent turning on the body diode at the output stage.

The EL7156 is available in both the 8 Ld SO and the 8 Ld PDIP packages. The relevant package should be chosen depending on the calculated power dissipation.

3-state Operation

When the OE pin is low, the output is 3-state (floating.) The output voltage is the parasitic capacitance's voltage. It can be any voltage between V_H and V_L, depending on the previous state. At 3-state, the output voltage can be pushed to any voltage between V_H and V_L. The output voltage can't be pushed higher than V_H or lower than V_L since the body diode at the output stage will turn on.

Supply Voltage Range and Input Compatibility

The EL7156 is designed for operation on supplies from 5V to 15V (4.5V to 16.5V maximum). The table on page 6 shows the specifications for the relationship between the V_S+, V_S-, V_H, V_L, and GND pins.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V_S+) of 5V, the EL7156 is also compatible with TTL inputs.

Power Supply Bypassing

When using the EL7156, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7156 necessitate the use of a bypass capacitor between the supplies (V_S+ & V_S-) and GND pins. It is recommended that a 2.2µF tantalum capacitor be used in parallel with a 0.1µF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the V_H and V_L pins have some level of bypassing, especially if the EL7156 is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7156 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + (C_{VS} \times V_S^2 \times f) + [(C_{INT} + C_L) \times V_{OUT}^2 \times f]$$

where:

- V_S is the total power supply to the EL7156 (from V_S+ to GND)
- V_{OUT} is the swing on the output (V_H - V_L)
- C_{VS} is the integral capacitance due to V_S+
- C_{INT} is the integral load capacitance due to V_H
- I_S is the quiescent supply current (3mA max)
- f is frequency

TABLE 1. INTEGRAL CAPACITANCE

V_S+=V_H(V)	C_{VS}(pF)	C_{INT}(pF)
5	80	120
10	85	145
15	90	180

Having obtained the application's power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T_{JMAX}:

$$\theta_{JA} = \frac{T_{JMAX} - T_{MAX}}{PD}$$

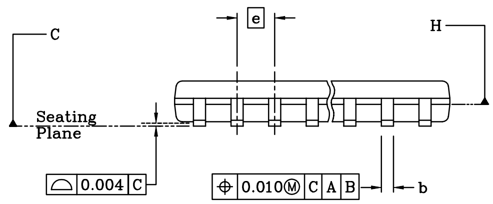
where:

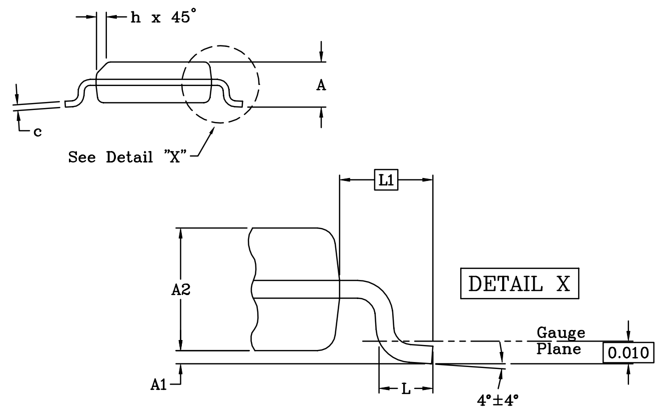
- T_{JMAX} is the maximum junction temperature (125°C)
- T_{MAX} is the maximum operating temperature
- PD is the power dissipation calculated above
- θ_{JA} thermal resistance on junction to ambient

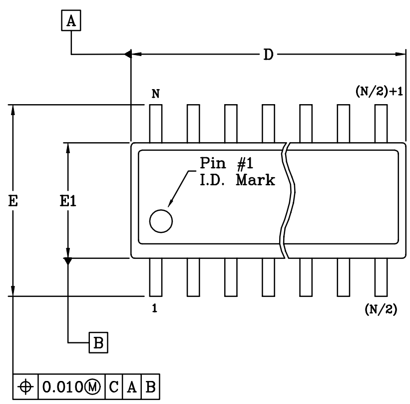
θ_{JA} is 160°C/W for the SO8 package and 100°C/W for the PDIP8 package when using a standard JEDEC JESD51-3 single-layer test board. If T_{JMAX} is greater than 125°C when calculated using the equation above, then one of the following actions must be taken:

- Reduce θ_{JA} the system by designing more heat-sinking into the PCB (as compared to the standard JEDEC JESD51-3)
- Use the PDIP8 instead of the SO8 package
- De-rate the application either by reducing the switching frequency, the capacitive load, or the maximum operating (ambient) temperature (T_{MAX})

SO Package Outline Drawing







DIMENSION TABLE

Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:

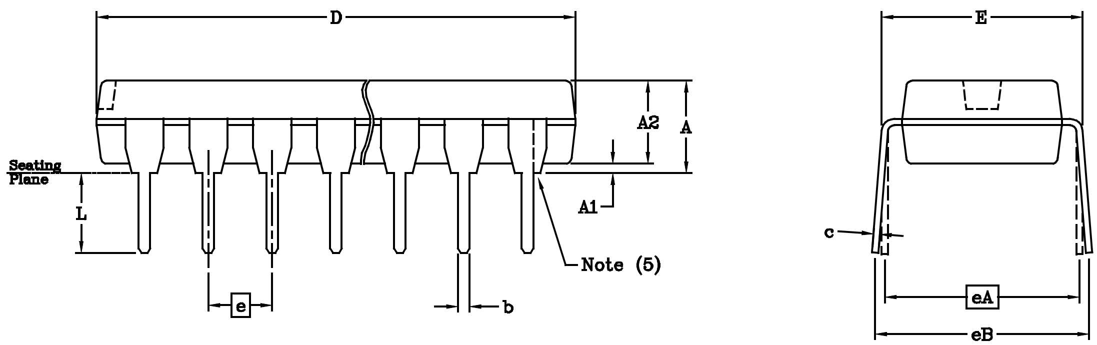
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

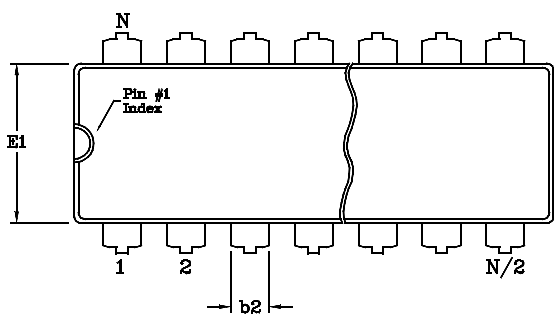
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

PDIP Package Outline Drawing





DIMENSION TABLE						
Symbol	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	Tolerance
A	0.210	0.210	0.210	0.210	0.210	MAX.
A1	0.015	0.015	0.015	0.015	0.015	MIN.
A2	0.130	0.130	0.130	0.130	0.130	+/- 0.005
b	0.018	0.018	0.018	0.018	0.018	+/- 0.002
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002
D (1)	0.375	0.750	0.750	0.890	1.020	+/- 0.010
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010
E1 (2)	0.250	0.250	0.250	0.250	0.250	+/- 0.005
e	0.100	0.100	0.100	0.100	0.100	Basic
eA	0.300	0.300	0.300	0.300	0.300	Basic
eB	0.345	0.345	0.345	0.345	0.345	+/- 0.025
L	0.125	0.125	0.125	0.125	0.125	+/- 0.010
N	8	14	16	18	20	Reference

Notes:

(1) Plastic or metal protrusions of 0.010" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.

(4) Dimension eB is measured with the lead tips unconstrained.

(5) 8 and 16 lead packages have half end-leads as shown.

Drawing #: MDP0031	PACKAGE OUTLINE DRAWING
Rev: B	PLASTIC DUAL INLINE PACKAGE (PDIP) FAMILY
Date: 2/26/99	
Units: Inches	élantec Semiconductor, Inc.
JEDEC Reg: MS-001	HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>