August 21, 1998 FN7294

Programmable CPU Power Supply Unit

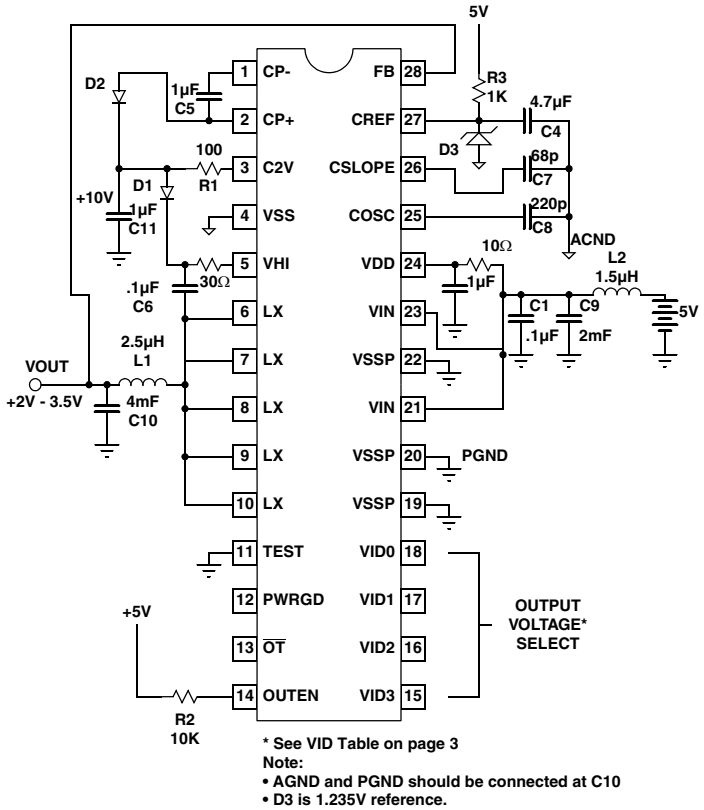
The EL7560 is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 5V to 3V application.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The output voltage is adjustable using a 4-bit parallel interface. A power OK signal "PWRGD' pulls high when the FB pin is within -7% of the programmed value.

Pinout

EL7560
(28-PIN SOIC)
TOP VIEW



*** See VID Table on page 3**
Note:
• AGND and PGND should be connected at C10
• D3 is 1.235V reference.

Features

- 3.3V @ 12.4amps continuous
- Internal FETs
- >90% efficiency
- Synchronous switching
- 4-bit digitally adjustable output voltage
- User adjustable slope compensation
- Internal soft start
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1MHz
- 1% output accuracy
- Sync function
- Power good signal

Applications

- PC motherboards
- Local high power CPU supplies

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL7560CM	-40°C to +85°C	28-Pin SOIC	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{IN}, V_{DD}) 5.5V
Output Pins . . . . . -0.3V below GND, +0.3V above V_{DD}
Instantaneous Peak Output Current 16A
Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .135°C
Power Dissipation 3W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

$V_{DD} = V_{IN} = 5V$, $C_{OSC} = 1nF$, $C_{SLOPE} = 68pF$, $T_A = 25°C$, unless otherwise specified (Note 1)

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
V_{2X}	Voltage Doubler Output	V_{DD}=5V, I_{LOAD}=20mA	8.0	9	9.5	V
DAC_{LSB}	DAC Resolution		0.095		0.105	V
F_{OSC}	Oscillator Initial Accuracy		105	120	135	kHz
F_{OSCTC}	Oscillator Tempco	0°C<T_A<125°C		±0.1		%/°C
V_{RAMP}	Oscillator Ramp Amplitude			1.2		V
M_{SS}	Soft Start Slope	F_{OSC}=500kHz		0.3		V/msec
I_{VID}	VID Pull Up Current	VID = 0V	9	13	18	µA
I_{CSLOPE}	C_{SLOPE} Charging Current		32	40	48	µA
I_{DD}	Supply Current	OUTEN=4V F_{OSC}=120kHz		25	35	mA
I_{DDOFF}	Stdby Current	OUTEN=0V		3	5	mA
R_{DSON}	Composite FET Resistance		18		25	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.1		mΩ/°C
V_{OUT}	Output Initial Acurracy	VID=0111	2.765	2.8	2.835	V
V_{RANGE}	Output Voltage Range	VID=1110 to 0000	2.065		3.535	V
I_{LMAX}	Maximum current	V_{OUT}=0		14.0		amps
V_{OUT-TC}	Output Tempco	0°C<T_A<70°C		±1		%
$V_{OUT-LINE}$	Output Line Regulation	V_{OUT}=2.8, 4.5V_{DD}<5.5, V_{DD}=V_{IN}	-1		1	%
$V_{OUT-LOAD}$	Output Load Regulation	0.3A<I_{LOAD}<12.4A	-1		1	%
$V_{OUT-TOT}$	Output Total Variation		-2		2	%
OT_{OFF}	Over Temperature Threshold			135		°C
OT_{HYS}	Over Temperature Hysteresis			50		°C
V_{PWRGD}	Power Good Threshold with Respect to Desired OutputVoltage	VID=0111	-9	-7	-5	%
V_{DD-ON}	Minimum V_{DD} form Startup				4	V
V_{DD-OFF}	Maximum V_{DD} for Shutdown		3.75			V

NOTE:

1. The oscillator and voltage doubler operate normally when V_{DD} exceeds V_{DD-ON} threshold, independent of the OUTEN logic level.

Voltage Identification Codes

P6 PINS				
V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{DC}
1	1	1	1	0, No CPU
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

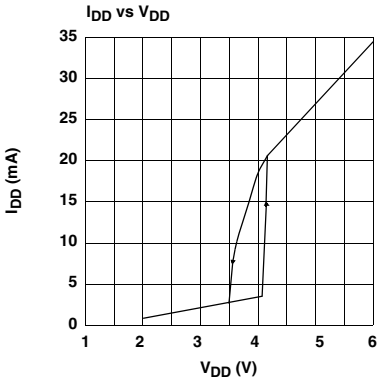
EL7560 Pin Descriptions

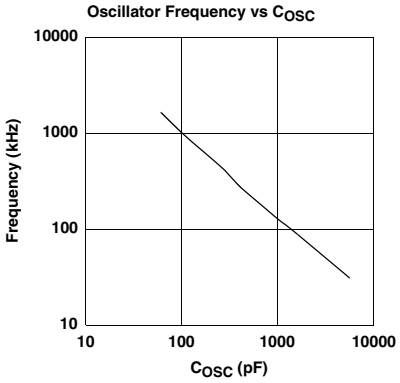
PIN NUMBER	NAME	DESCRIPTION
1	C_{P-}	Negative input for the charge pump bootstrap capacitor. (Note 1)
2	C_{P+}	Positive input for the charge pump bootstrap capacitor. (Note 1)
3	C2V	Voltage doubler output. Pin requires at least a 1µF capacitor to GND. (Note 1)
4	V_{SS}	Ground return for the control circuitry.
5	V_{HI}	Positive supply for the high side driver. This pin is bootstrapped from the LX pin with a 0.1µF capacitor.
6	LX	Common connection between the two large internal FETs. External inductor connection.
7	LX	Same as pin 6.
8	LX	Same as pin 6.
9	LX	Same as pin 6.
10	LX	Same as pin 6.
11	TEST	This is test pin and **must remain grounded at all times**
12	PWRGD	Pin pulls high when the FB pin is within - 7%(typ) of its programmed value.
13	$\overline{OT}$	Overtemperature indicator. Pulls low when the die temperature exceeds 135°C. Pin has 10mA pull-up.
14	$\overline{OT}$	A logic high on OUTEN enables the regulator (Note 1)
15	VID3	Bit 3(MSB) of the output voltage select DAC.
16	VID2	Bit 2 of the output voltage select DAC.
17	VID1	Bit 1 of the output voltage select DAC.
18	VID0	Bit 0(LSB) of the output voltage select DAC.
19	V_{SSP}	Ground return to the buck regulator.
20	V_{SSP}	Same as pin 19.
21	V_{IN}	Positive power supply input to the buck regulator.
22	V_{SSP}	Same as pin 19.
23	V_{IN}	Same as pin 21.
24	V_{DD}	Pin supplies power to the internal control circuitry.
25	C_{OSC}	Oscillator timing capacitor. Oscillator Frequency is approximately: $F_{OSC}(Hz)=0.0001/C_{OSC}(F)$. The duty cycle is approximately 5%. (Note 1)
26	C_{SLOPE}	Slope compensation capacitor.
27	C_{REF}	External reference input pin.
28	FB	Voltage feedback pin for the buck regulator.

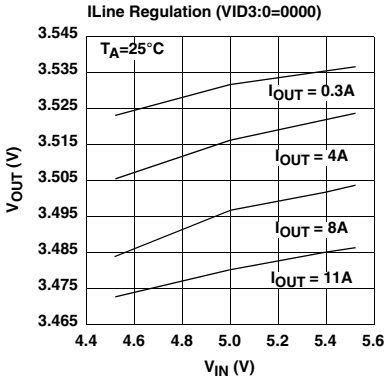
NOTE:

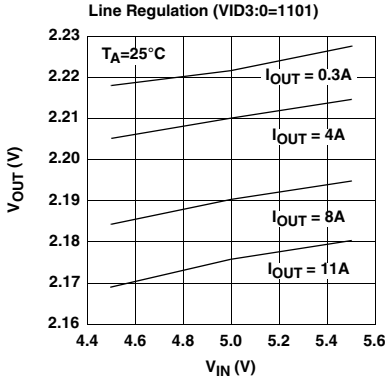
1. The oscillator and voltage doubler operate normally when V_{DD} exceeds V_{DD-ON} threshold, independent of the OUTEN logic level.

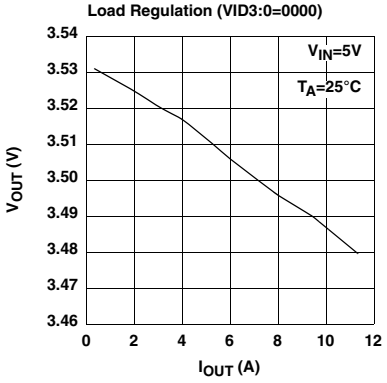
Typical Performance Curves

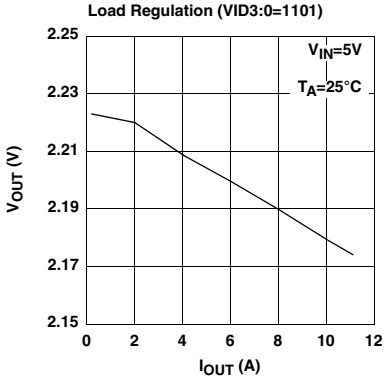




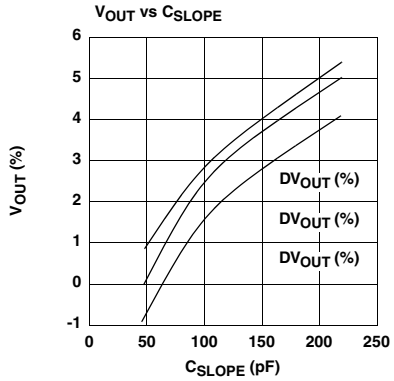


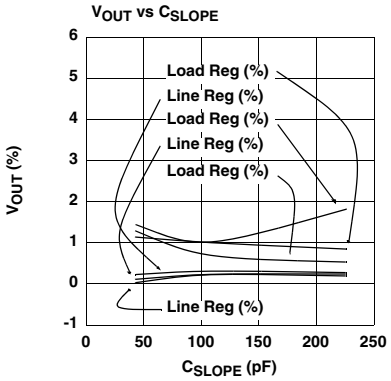


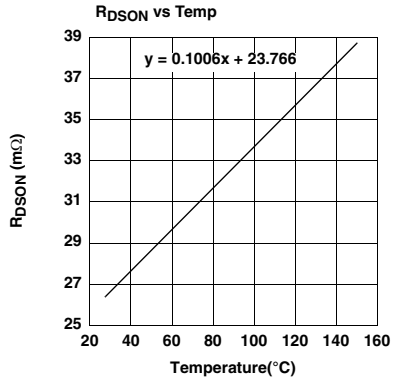


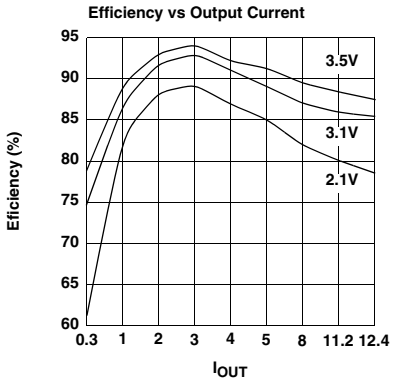


Typical Performance Curves (Continued)

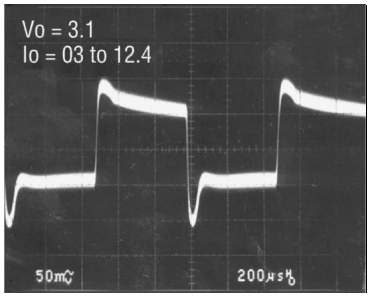




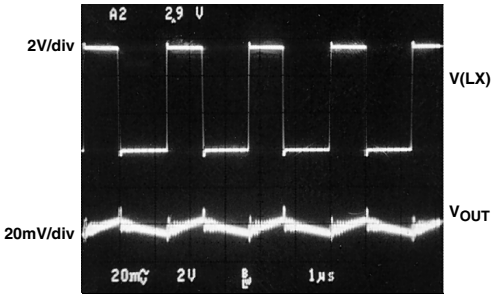




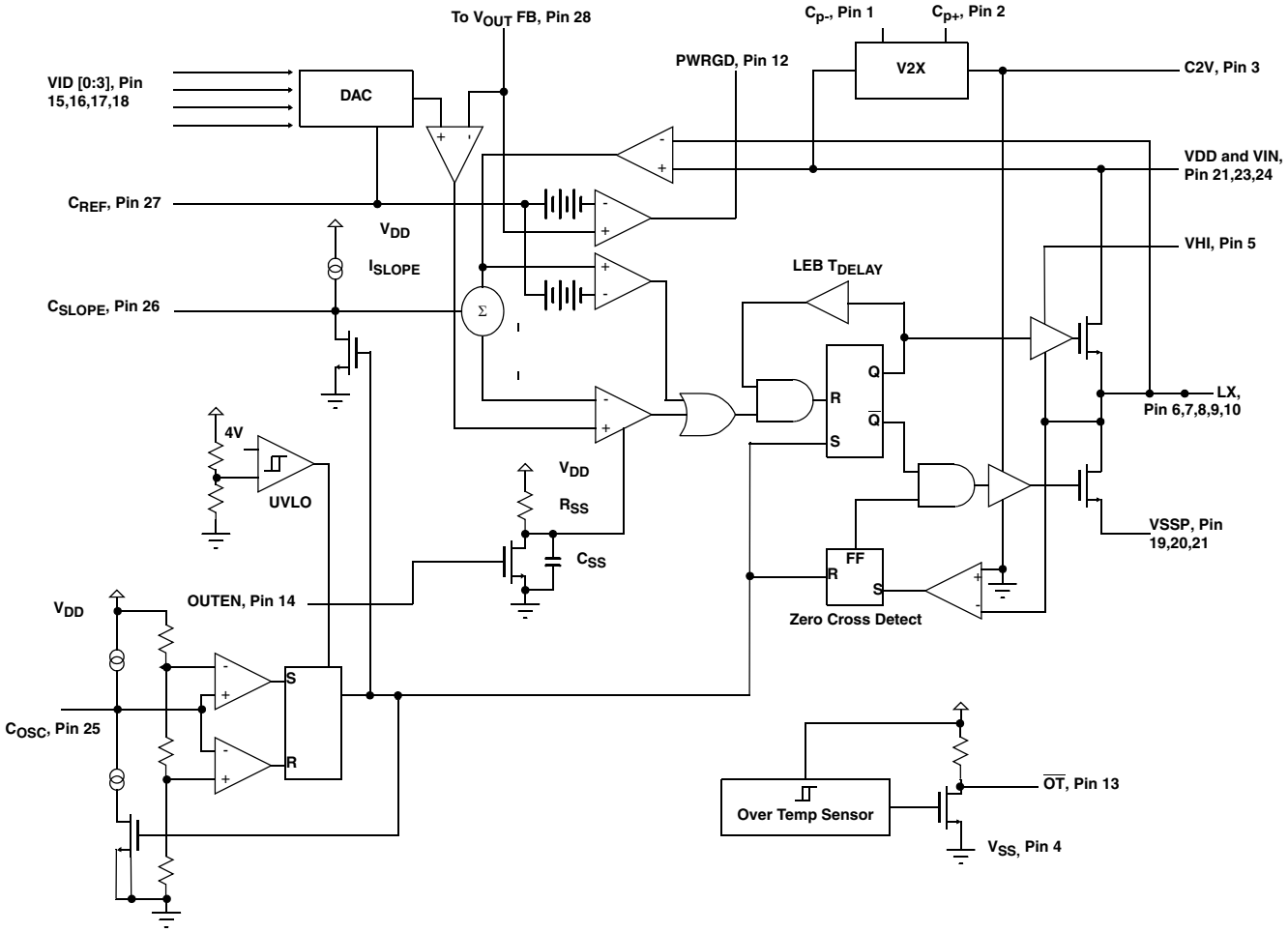
Transient Load Step
0.3Amp to 12.4Amp



Switching Waveforms I_{LOAD} = 2A



EL7560 Functional Block Diagram



Thermal considerations and power dissipation:

To achieve the maximum 12.4A continuous output current, the EL7560 is packaged in a 28 pin HSOP (Heat-Slug SO Package). Within the package, the EL7560 die is attached to one side of a copper slug. The other side of the slug is coincident with the package top surface, and is therefore exposed to the ambient environment. The copper slug provides an exceptionally low thermal resistance (θJC) of typically 7°C/W. To obtain low junction to ambient thermal resistance (θJA), a heatsink is required to provide heat transfer path from the die to the ambient. The EL7560 power dissipation is a direct function of the “on” resistance of the internal power FETs (Rds-on) and the output current. For the maximum 12.4A output current and the worse case Rds-on at 125°C (35mΩ), the power dissipation is $Iout^2$*R = 5.38W. To maintain 12.4A continuous output current operation at the maximum 70°C ambient temperature, the die temperature must be kept below the 135°C thermal shut down temperature. This requires a θJA of 12°C/W. To help achieve such a low θJA with practical size heatsink, airflow is also required. Application note #13 shows the 11°C/W thermal resistance can be achieved with the Wakefield heatsink #8052-60 and minimum 200LFM airflow.