3-Channel DC/DC Converter

The EL7583 is a 3-channel DC/DC converter IC which is designed primarily for use in TFT-LCD applications. It features a PWM boost converter with 2.7V to 14V input capability and 5V to 17V output, which powers the column drivers and provides up to 470mA @ 12V, 370mA @ 15V from 5V supply. A pair of charge pump control circuits provide regulated outputs of V_{ON} and V_{OFF} supplies at 8V to 40V and -5V to -40V, respectively, each at up to 60mA.

The EL7583 features adjustable switching frequency, adjustable soft start, and a separate output V_{ON} enable control to allow selection of supply start-up sequence. An over-temperature feature is provided to allow the IC to be automatically protected from excessive power dissipation.

The EL7583 is available in a standard 20 Ld TSSOP package and the Pb-free 20 Ld HTSSOP package. Both are specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL7583IR	7583IR	-	20 Ld TSSOP	MDP0044
EL7583IR-T7	7583IR	7”	20 Ld TSSOP	MDP0044
EL7583IR-T13	7583IR	13”	20 Ld TSSOP	MDP0044
EL7583IREZ (See Note)	7583IREZ	-	20 Ld HTSSOP (Pb-free)	MDP0048
EL7583IREZ-T7 (See Note)	7583IREZ	7”	20 Ld HTSSOP (Pb-free)	MDP0048
EL7583IREZ-T13 (See Note)	7583IREZ	13”	20 Ld HTSSOP (Pb-free)	MDP0048

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

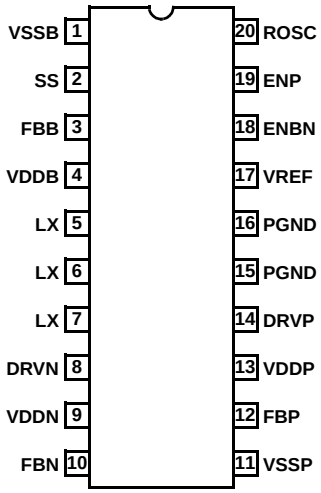
- TFT-LCD display supply
  - Boost regulator
  - V_{ON} charge pump
  - V_{OFF} charge pump
- 2.7V to 14V V_{IN} supply
- 5V < V_{BOOST} < 17V
- 5V < V_{ON} < 40V
- -40V < V_{OFF} < 0V
- V_{BOOST} = 12V @ 470mA
- V_{BOOST} = 15V @ 370mA
- High frequency, small inductor DC/DC boost circuit
- Over 90% efficient DC/DC boost converter capability
- Adjustable frequency
- Adjustable soft-start
- Adjustable outputs
- Small parts count
- Pb-free plus anneal available (RoHS compliant)

Applications

- TFT-LCD panels
- PDAs

Pinout

EL7583
(20 LD TSSOP/HTSSOP)
TOP VIEW



REFER TO PCB LAYOUT GUIDELINE

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

V_{IN} Input Voltage 14V
V_{DDB}, V_{DDP}, V_{DDN} 18V
LX Voltage 18V
Maximum Continuous Output Current 0.5A
Storage Temperature . . . . . .-65°C to +150°C
Die Junction Temperature . . . . . .125°C
Power Dissipation . . . . . See Curves
Operating Ambient Temperature . . . . . .-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{IN} = 3.3V, V_{BOOST} = 12V, R_{OSC} = 100kΩ, T_A = 25°C Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC BOOST CONVERTER						
IQ1_B	Quiescent Current - Shut-down	ENBN = ENP = 0V		0.8	10	µA
IQ2_B	Quiescent Current - Switching	ENBN = V_{DDB}		4.8	8	mA
V(FBB)	Feedback Voltage		1.275	1.300	1.325	V
V_{REF}	Reference Voltage		1.260	1.310	1.360	V
V_{ROSC}	Oscillator Set Voltage		1.260	1.325	1.390	V
I(FBB)	Feedback Input Bias Current			0.1		µA
V_{DDB}	Boost Converter Supply Range		2.7		17	V
D_{MAX}	Maximum Duty Cycle		85	92		%
$I(LX)_{MAX}$	Peak Internal FET Current			1.75		A
R_{DS-ON}	Switch On Resistance	at V_{BOOST} = 10V, I(LX) total = 350mA		0.22		Ω
$I_{LEAK-SWITCH}$	Switch Leakage Current	I(LX) total			1	µA
V_{BOOST}	Output Range	$V_{BOOST} > V_{IN} + V_{DIODE}$	5		17	V
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	2.7V < V_{IN} < 13.2V, V_{BOOST} = 15V		0.1		%
$\Delta V_{BOOST}/\Delta I_{O1}$	Load Regulation	50mA < I_{O1} < 250mA		0.5		%
$F_{OSC-RANGE}$	Frequency Range	R_{OSC} range = 240kΩ to 60kΩ	200		1000	kHz
F_{OSC1}	Switching Frequency	R_{OSC} = 100kΩ	620	680	750	kHz
POSITIVE REGULATED CHARGE PUMP (V_{ON}) Most positive V_{ON} output depends on the magnitude of the V_{DDP} input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)						
V_{DDP}	Supply Input for Positive Charge Pump	Usually connected to V_{BOOST} output	5		17	V
$IQ1(V_{DDP})$	Quiescent Current - Shut-down	ENP = 0V		11.5	20	µA
$IQ2(V_{DDP})$	Quiescent Current - Switching	ENBN = ENP = V_{DDB}		2.3	5	mA
V(FBP)	Feedback Reference Voltage		1.245	1.310	1.375	V
I(FBP)	Feedback Input Bias Current			0.1		µA
I(DRVP)	RMS DRVP Output Current	V_{DDP} = 12V		60		mA
		V_{DDP} = 6V	15			mA
ILR_V_{ON}	Load Regulation	5mA < I_L < 15mA	-0.5	0.03	0.5	%/mA
F_{PUMP}	Charge Pump Frequency	Frequency set by R_{OSC} - see boost section	0.5*F_{OSC}			

Electrical Specifications V_{IN} = 3.3V, V_{BOOST} = 12V, R_{OSC} = 100kΩ, T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
NEGATIVE REGULATED CHARGE PUMP (V_{OFF}) Most negative V_{OFF} output depends on the magnitude of the V_{DDN} input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)						
V_{DDN}	Supply Input for Negative Charge Pump	Usually connected to V_{BOOST} output	5		17	V
IQ1(V_{DDN})	Quiescent Current - Shut-down	ENBN = 0V		1.2	10	µA
IQ2(V_{DDN})	Quiescent Current - Switching	ENBN = V_{DDB}		2.3	5	mA
V(FBN)	Feedback Reference Voltage		-80	0	+80	mV
I(FBN)	Feedback Input Bias Current	Magnitude of input bias		0.1		µA
I(DRVN)	RMS DRVN Output Current	V_{DDN} = 12V		60		mA
		V_{DDN} = 6V	15			mA
ILR_V_{OFF}	Load Regulation	-15mA < I_L < -5mA	-0.5	0.03	0.5	%/mA
F_{PUMP}	Charge Pump Frequency	Frequency set by R_{OSC} - see boost section		0.5*F_{OSC}		
ENABLE CONTROL LOGIC						
V_{HI-ENX}	Enable Input High Threshold	x = “BN”, “P”	1.6			V
V_{LO-ENX}	Enable Input Low Threshold	x = “BN”, “P”			0.8	V
IL(EN”X”)	Logic Low Bias Current	X = “BN”, “P” = 0V		0.1		µA
IL(ENBN)	Logic High Bias Current	ENBN = 5V		7.5	15	µA
IL(ENP)	Logic High Bias Current	ENP = 5V		3.3	7.5	µA
OVER-TEMPERATURE PROTECTION						
T_{OT}	Over-temperature Threshold			130		°C
T_{HYS}	Over-temperature Hysteresis			40		°C

Pin Descriptions I = Input, O = Output, S = Supply

PIN NUMBER	PIN NAME	PIN TYPE	PIN FUNCTION
1	VSSB	S	Ground for DC/DC boost and reference circuits; chip substrate
2	SS	I	Soft-start input; the capacitor connected to this pin sets the current limited start time
3	FBB	I	Voltage feedback input for boost circuit; determines boost output voltage, V_{BOOST}
4	VDDB	S	Positive supply input for DC/DC boost circuits
5	LX	O	Boost regulator inductor drive connected to drain of internal NFET
6	LX	O	Boost regulator inductor drive connected to drain of internal NFET
7	LX	O	Boost regulator inductor drive connected to drain of internal NFET
8	DRVN	O	Driver output for the external generation of negative charge pump voltage, V_{OFF}
9	VDDN	S	Positive supply for input for V_{OFF} generator
10	FBN	I	Voltage feedback input to determine negative charge pump output, V_{OFF}
11	VSSP	S	Negative supply pin for both the positive and negative charge pumps
12	FBP	I	Voltage feedback to determine positive charge pump output, V_{ON}
13	VDDP	S	Positive supply input for V_{ON} generator
14	DRVP	O	Voltage driver output for the external generation of positive charge pump, V_{ON}
15	PGND	O	Power ground, connected to source of internal NFET
16	PGND	O	Power ground, connected to source of internal NFET
17	VREF	I	Voltage reference for charge pump circuits; decouple to ground
18	ENBN	I	Enable pin for boost (V_{BOOST} generation) and negative charge pump (V_{OFF} generation); active high
19	ENP	I	Enable for DRVP (V_{ON} generation); active high
20	ROSC	I	Connected to an external resistor to ground; sets the switching frequency of the DC/DC boost

Typical Performance Curves

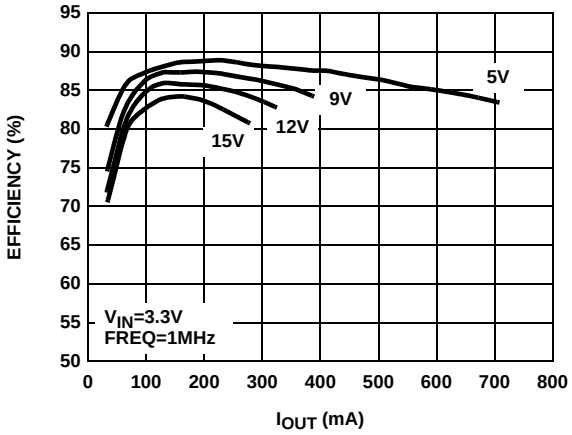


FIGURE 1. EFFICIENCY vs I_{OUT}

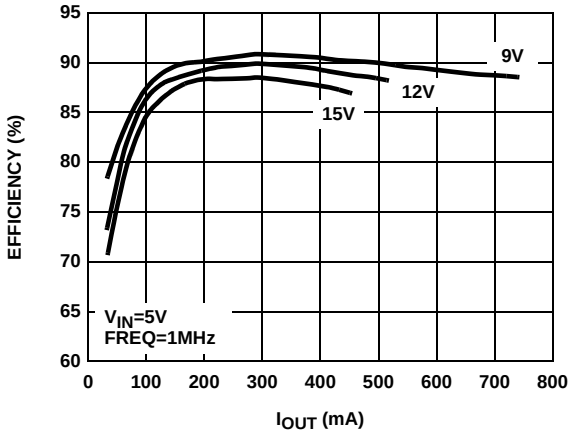


FIGURE 2. EFFICIENCY vs I_{OUT}

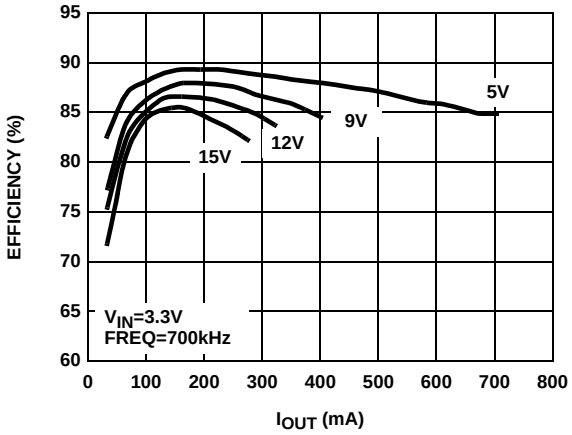


FIGURE 3. EFFICIENCY vs I_{OUT}

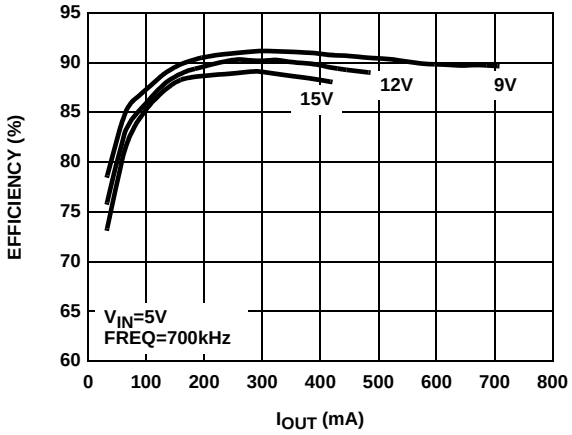


FIGURE 4. EFFICIENCY vs I_{OUT}

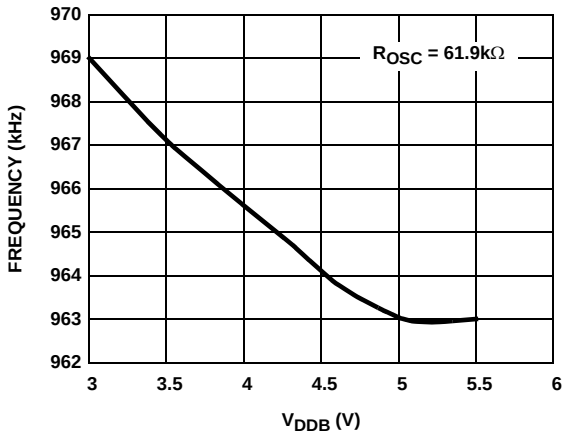


FIGURE 5. F_S vs V_{DDB}

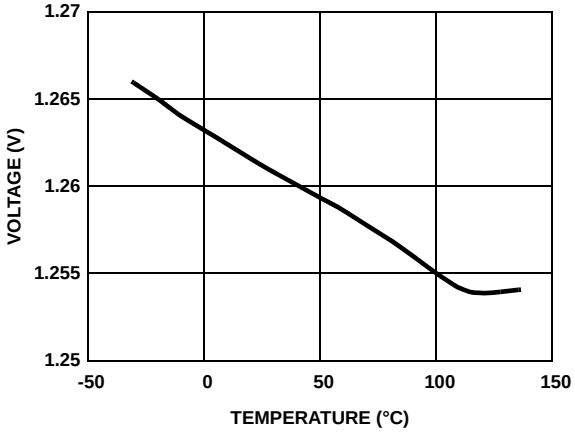


FIGURE 6. V_{REF} vs TEMPERATURE

Typical Performance Curves (Continued)

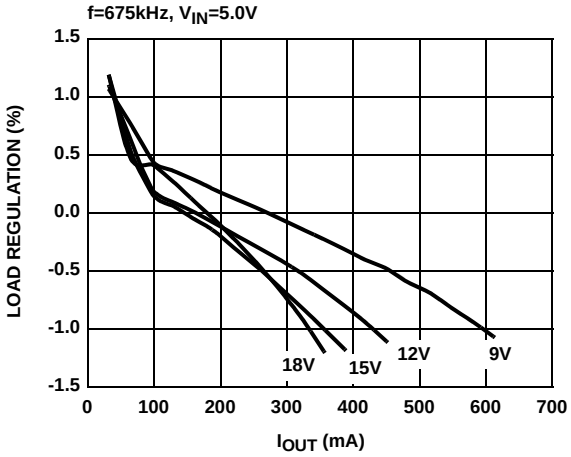


FIGURE 7. LOAD REGULATION vs I_{OUT}

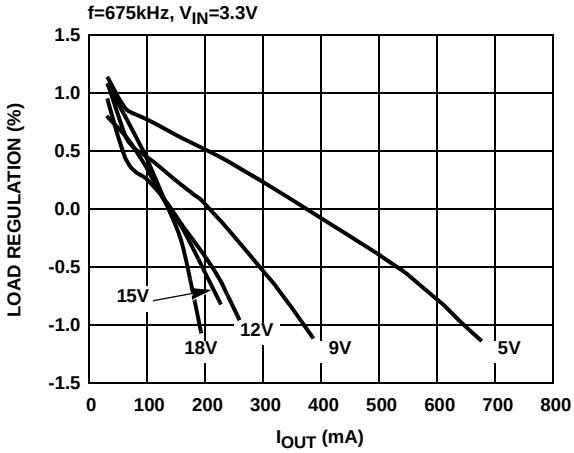


FIGURE 8. LOAD REGULATION vs I_{OUT}

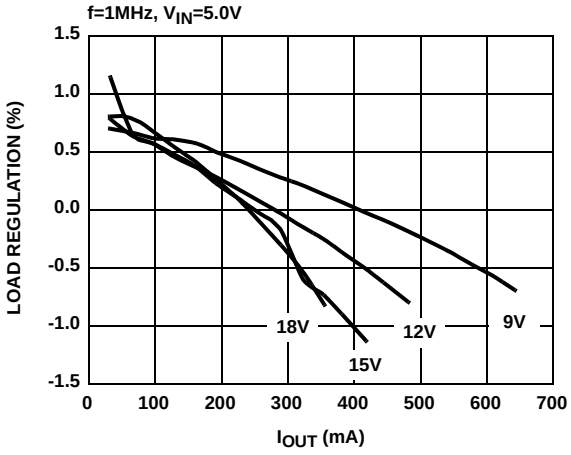


FIGURE 9. LOAD REGULATION vs I_{OUT}

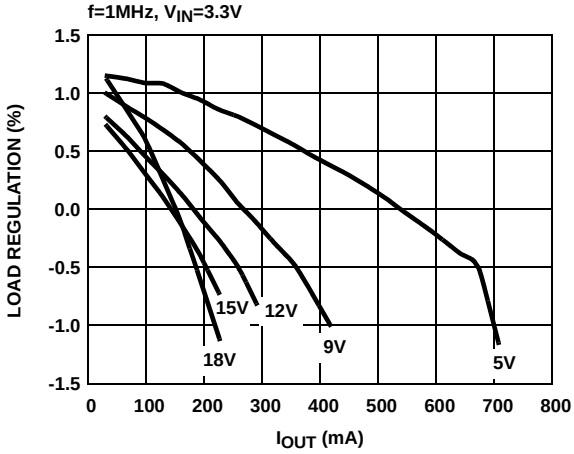


FIGURE 10. LOAD REGULATION vs I_{OUT}

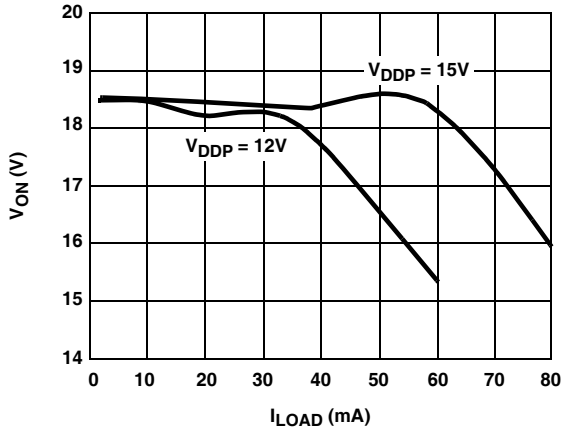


FIGURE 11. V_{ON} vs I_{ON}

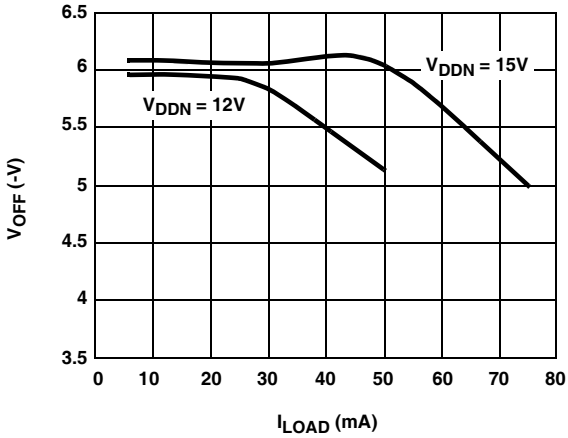


FIGURE 12. V_{OFF} vs I_{OFF}

Typical Performance Curves (Continued)

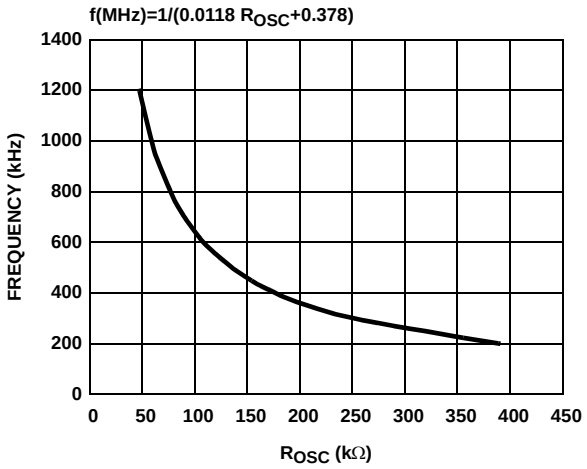


FIGURE 13. F_S vs R_{OSC}

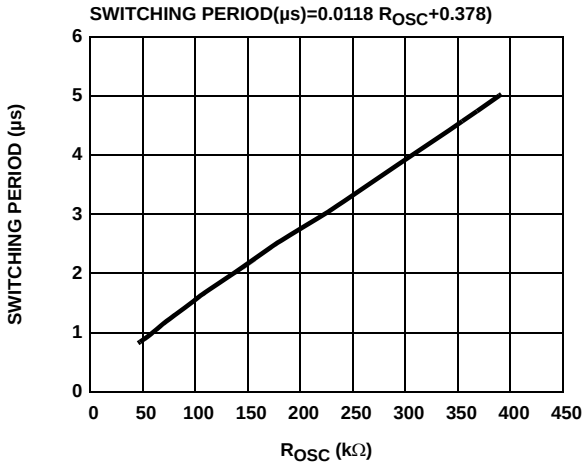


FIGURE 14. F_S vs R_{OSC}

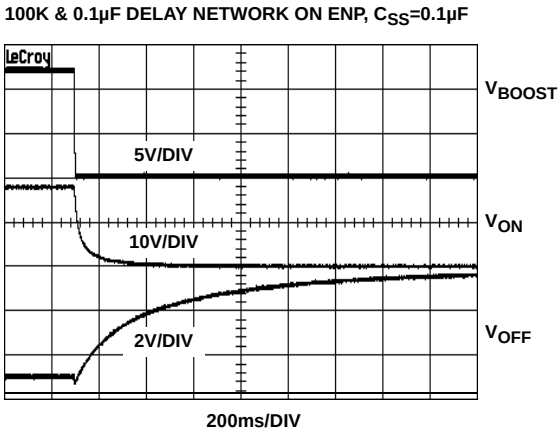


FIGURE 15. POWER-DOWN

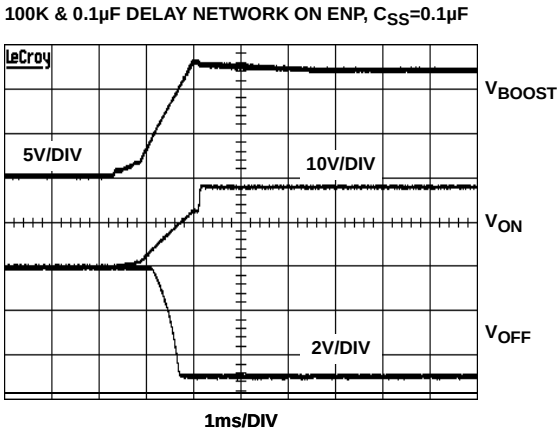


FIGURE 16. POWER-UP

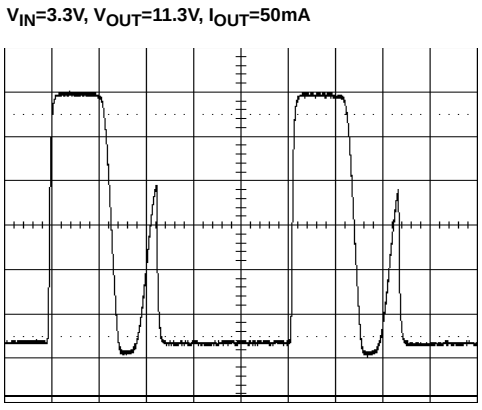


FIGURE 17. LX WAVEFORM - DISCONTINUOUS MODE

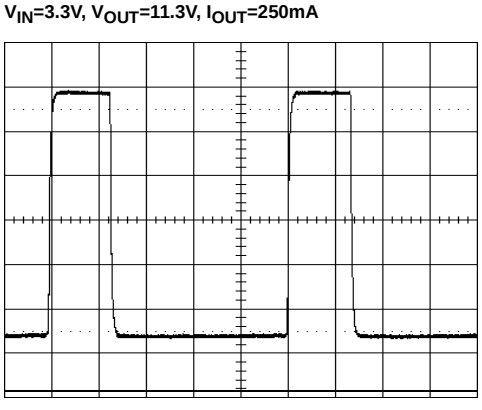


FIGURE 18. LX WAVEFORM - CONTINUOUS MODE

Typical Performance Curves (Continued)

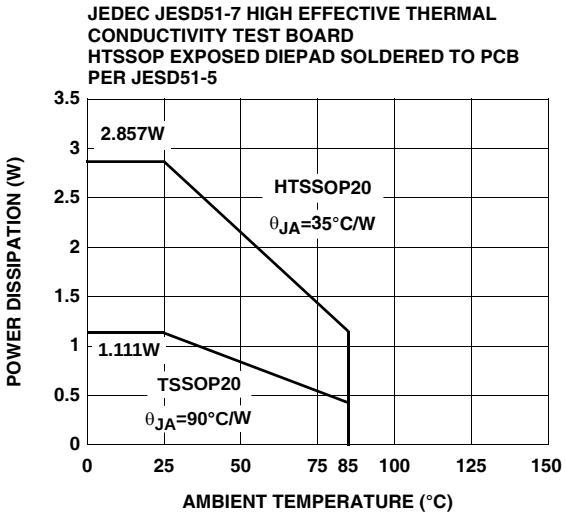


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

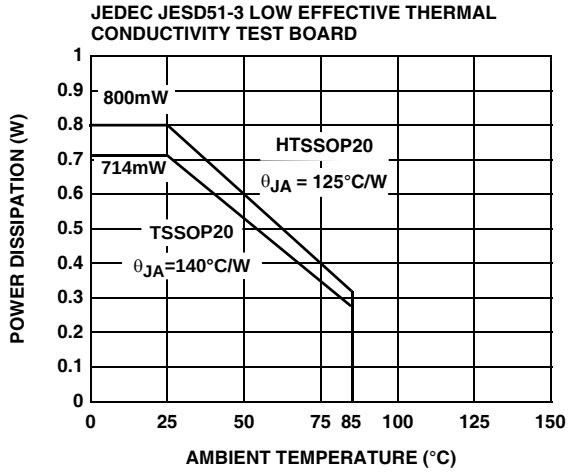
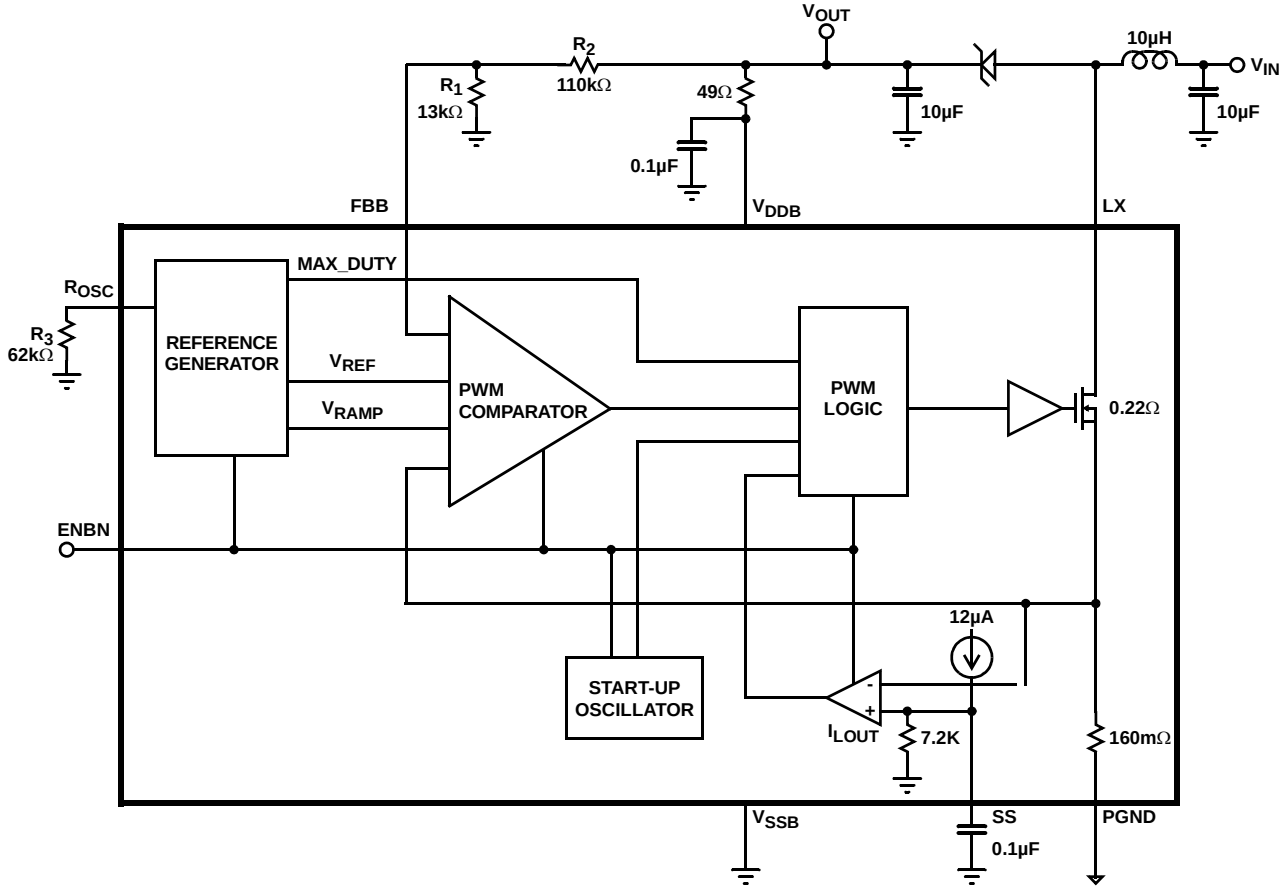


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Functional Block Diagram



Applications Information

The EL7583 is high efficiency multiple output power solution designed specifically for thin-film transistor (TFT) liquid crystal display (LCD) applications. The device contains one high current boost converter and two low power charge pumps (V_{ON} and V_{OFF}).

The boost converter contains an integrated N-channel MOSFET to minimize the number of external components. The converter output voltage can be set from 5V to 18V with external resistors. The V_{ON} and V_{OFF} charge pumps are independently regulated to positive and negative voltages using external resistors. Output voltages as high as 40V can be achieved with additional capacitors and diodes.

Boost Converter

The boost converter operates in constant frequency pulse-width-modulation (PWM) mode. Quiescent current for the EL7583 is only 5mA when enabled, and since only the low side MOSFET is used, switch drive current is minimized. 90% efficiency is achieved in most common application operating conditions.

A functional block diagram with typical circuit configuration is shown on previous page. Regulation is performed by the PWM comparator which regulates the output voltage by comparing a divided output voltage with an internal reference voltage. The PWM comparator outputs its result to the PWM logic. The PWM logic switches the MOSFET on and off through the gate drive circuit. Its switching frequency is external adjustable with a resistor from timing control pin (R_{OSC}) to ground. The boost converter has 200kHz to 1.2MHz operating frequency range.

Start-Up

After V_{DDB} reaches a threshold of about 2V, the power MOSFET is controlled by the start-up oscillator, which generates fixed duty-ratio of 0.5 - 0.7 at a frequency of several hundred kilohertz. This will boost the output voltage, providing the initial output current load is not too great (<250mA).

When V_{DDB} reaches about 3.7V, the PWM comparator takes over the control. The duty ratio will be decided by the multiple-input direct summing comparator, Max_Duty signal (about 90% duty-ratio), and the Current Limit Comparator, whichever is the smallest.

The soft-start is provided by the current limit comparator. As the internal 12µA current source charges the external soft-start capacitor, the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of output voltage.

The regulator goes through the start-up sequence as well after the ENBN signal is pulled to HI.

Steady-State Operation

When the output reaches the preset voltage, the regulator operates at steady state. Depending on the input/output condition and component, the inductor operates at either continuous-conduction mode or discontinuous-conduction mode.

In the continuous-conduction mode, the inductor current is a triangular waveform and LX voltage a pulse waveform. In the discontinuous-conduction mode, the inductor current is completely ‘dried-out’ before the MOSFET is turned on again. The input voltage source, the inductor, and the MOSFET and output diode parasitic capacitors forms a resonant circuit. Oscillation will occur in this period. This oscillation is normal and will not affect the regulation.

At very low load, the MOSFET will skip pulse sometimes. This is normal.

Current Limit

The MOSFET current limit is nominal I_{LMT} = 1.75. This restricts the maximum output current I_{OMAX} based on the following formula:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O}$$

where:

- ΔI_L is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{F_S}$$

- D is the MOSFET turn-on radio and is decided by:

$$D = \frac{V_O - V_{IN}}{V_O}$$

- F_S is the switching frequency.

The following table gives typical values:
(Margins are considered 10%, 3%, 20%, 10%, and 15% on V_{IN}, V_O, L, F_S, and I_{LMT}, respectively)

TABLE 1. MAXIMUM CONTINUOUS OUTPUT CURRENT

V_{IN} (V)	V_O (V)	L (µH)	F_S (kHz)	I_{OMAX} (mA)
3.3	9	10	1000	430
3.3	12	10	1000	320
3.3	15	10	1000	250
5	9	10	1000	650
5	12	10	1000	470
5	15	10	1000	370
12	18	10	1000	830

Component Considerations

Input Capacitor

It is recommended that C_{IN} is larger than 10µF. Theoretically, the input capacitor has ripple current of ΔI_L. Due to high-frequency noise in the circuit, the input current ripple may exceed the theoretical value. Larger capacitor will reduce the ripple further.

Boost Inductor

The inductor has peak and average current decided by:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_O}{1 - D}$$

The inductor should be chosen to be able to handle this current. Furthermore, due to the fixed internal compensation, it is recommended that maximum inductance of 10µH and 15µH to be used in the 5V and 12V or higher output voltage, respectively.

The output diode has average current of I_O, and peak current the same as the inductor's peak current. Schottky diode is recommended and it should be able to handle those currents.

Feedback Resistor Network

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 200kΩ is recommended. The boost converter output voltage is determined by the following relationship:

$$V_{BOOST} = \frac{R_1 + R_2}{R_1} \times V_{FBB}$$

where V_{FBB} is 1.300V.

A 1nF compensation capacitor across the feedback resistor to ground is recommended to keep the converter in stable operation at low output current and high frequency conditions.

Schottky Diode

Speed, forward voltage drop, and reverse current are the three most critical specifications for selecting the Schottky diode. The entire output current flows through the diode, so the diode average current is the same as the average load current and the peak current is the same as the inductor peak current. When selecting the diode, one must consider the forward voltage drop at the peak diode current. On the Elantec demo board, MBRM120 is selected. Its forward voltage drop is 450mV at 1A forward current.

Output Capacitor

The EL7583 is specially compensated to be stable with capacitors which have a worst-case minimum value of 10µF at the particular V_{OUT} being set. Output ripple voltage requirements also determine the minimum value and the type of capacitors. Output ripple voltage consists of two components - the voltage drop caused by the switching current though the ESR of the output capacitor and the charging and discharging of the output capacitor:

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{I_{OUT}}{C_{OUT} \times FS}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging/discharging of the output capacitor.

In addition to the voltage rating, the output capacitor should also be able to handle the RMS current is given by:

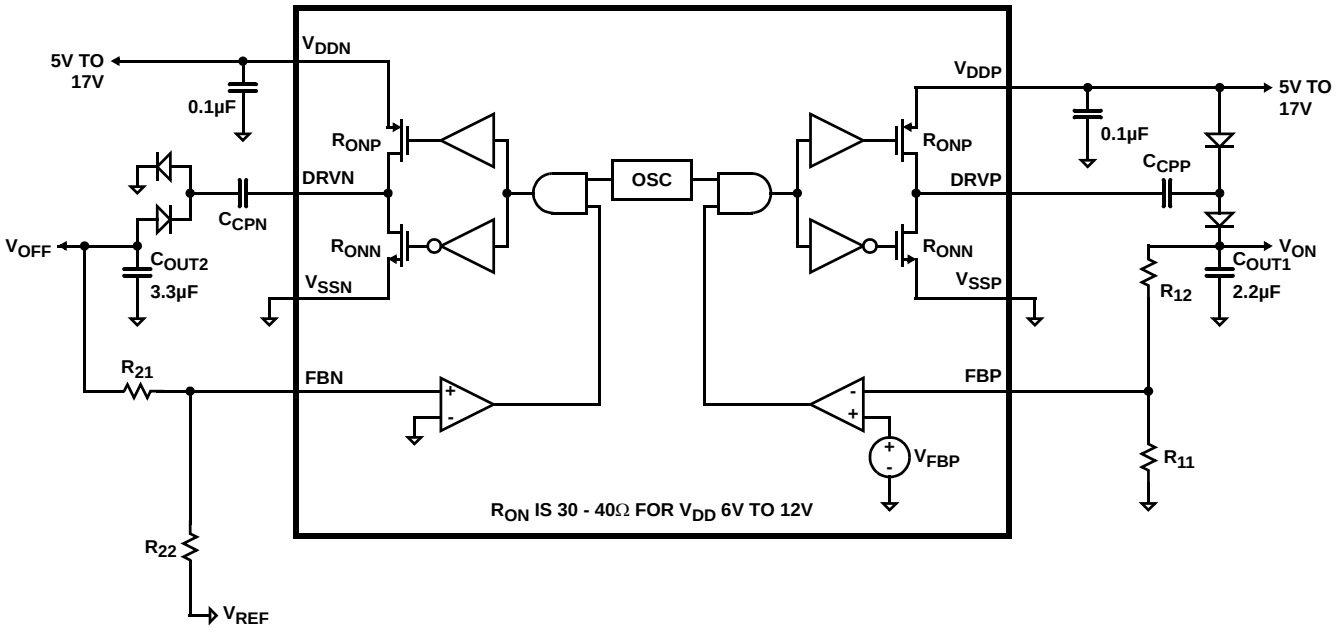
$$I_{CORMS} = \sqrt{(1 - D) \times \left(D + \frac{\Delta I_L^{\,2}}{I_{LAVG}^{\,2}} \times \frac{1}{12} \right)} \times I_{LAVG}$$

Positive and Negative Charge Pump (V_{ON} and V_{OFF})

The EL7583 contains two independent charge pumps (see charge pump block and connection diagram.) The negative charge pump inverts the V_{DDN} supply voltage and provides a regulated negative output voltage. The positive charge pump doubles the V_{DDP} supply voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by the internal comparator that senses the output voltage and compares it with and internal reference. The switching frequency of the charge pump is set to ½ the boost converter switching frequency.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps are short-circuit protected to 180mA at 12V supply and can provide 15mA to 60mA for 6V to 12V supply.

Single Stage Charge Pump



Positive Charge Pump Design Considerations

A single stage charge pump is shown above. The maximum V_{ON} output voltage is determined by the following equation:

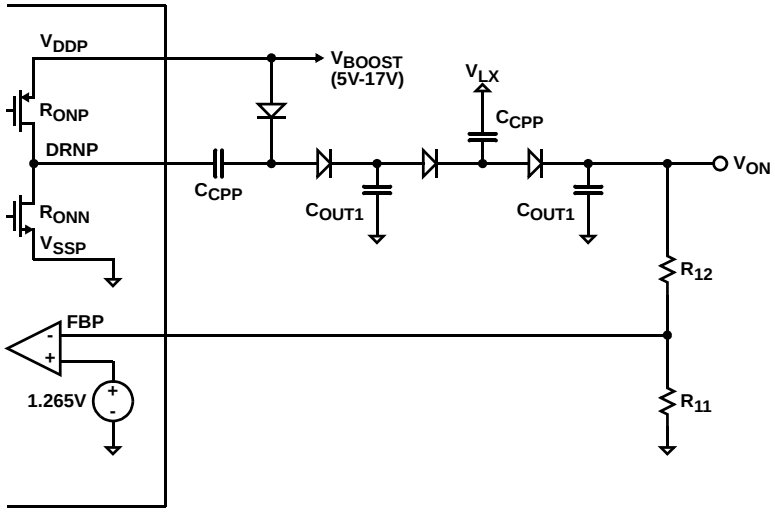
$$V_{ON(max)} \leq 2 \times V_{DDCPP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}}$$

where:

- R_{ONN} and R_{ONP} resistance values depend on the V_{DDP} voltage levels. For 12V supply, R_{ON} is typically 33Ω. For 6V supply, R_{ON} is typically 45Ω.

If additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The drive impedance at the LX switching is typically 220mΩ. The figure below illustrates an implementation for two-stage positive charge pump circuit.

Two-Stage Positive Charge Pump Circuit



The maximum V_{ON} output voltage for N+1 stage charge pump is:

$$V_{ON}(max) \leq 2 \times V_{DDP} - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}} + N \times V_{LX}(max) - N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPP}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT1}}\right)$$

R_{11} and R_{12} set the V_{ON} output voltage:

$$V_{ON} = V_{FBP} \times \frac{R_{11} + R_{12}}{R_{11}}$$

where V_{FBP} is 1.310V.

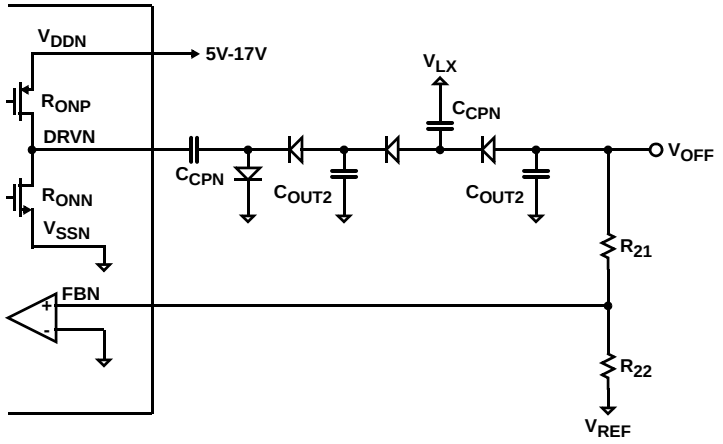
Negative Charge Pump Design Considerations

The criteria for the negative charge pump is similar to the positive charge pump. For a single stage charge pump, the maximum V_{OFF} output voltage is:

$$V_{OFF}(max) \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} - V_{DDN}$$

Similar to positive charge pump, if additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The figure on the next page shows a two stage negative charge pump circuit.

Two-Stage Negative Charge Pump Circuit



The maximum V_{OFF} output voltage for N+1 stage charge pump is:

$$V_{OFF(max)} \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}} -$$
$$V_{DDN} - N \times V_{LX(max)} + N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{CPN}} + I_{OUT} \times \frac{1}{0.5 \times F_S \times C_{OUT2}}\right)$$

R_{21} and R_{22} determine V_{OFF} output voltage:

$$V_{OFF} = -V_{REF} \times \frac{R_{21}}{R_{22}}$$

where V_{REF} is 1.310V.

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that die temperature exceeds the thermal trip point, the device will shut down and disable itself. The upper and lower trip points are typically set to 130°C and 90°C respectively.

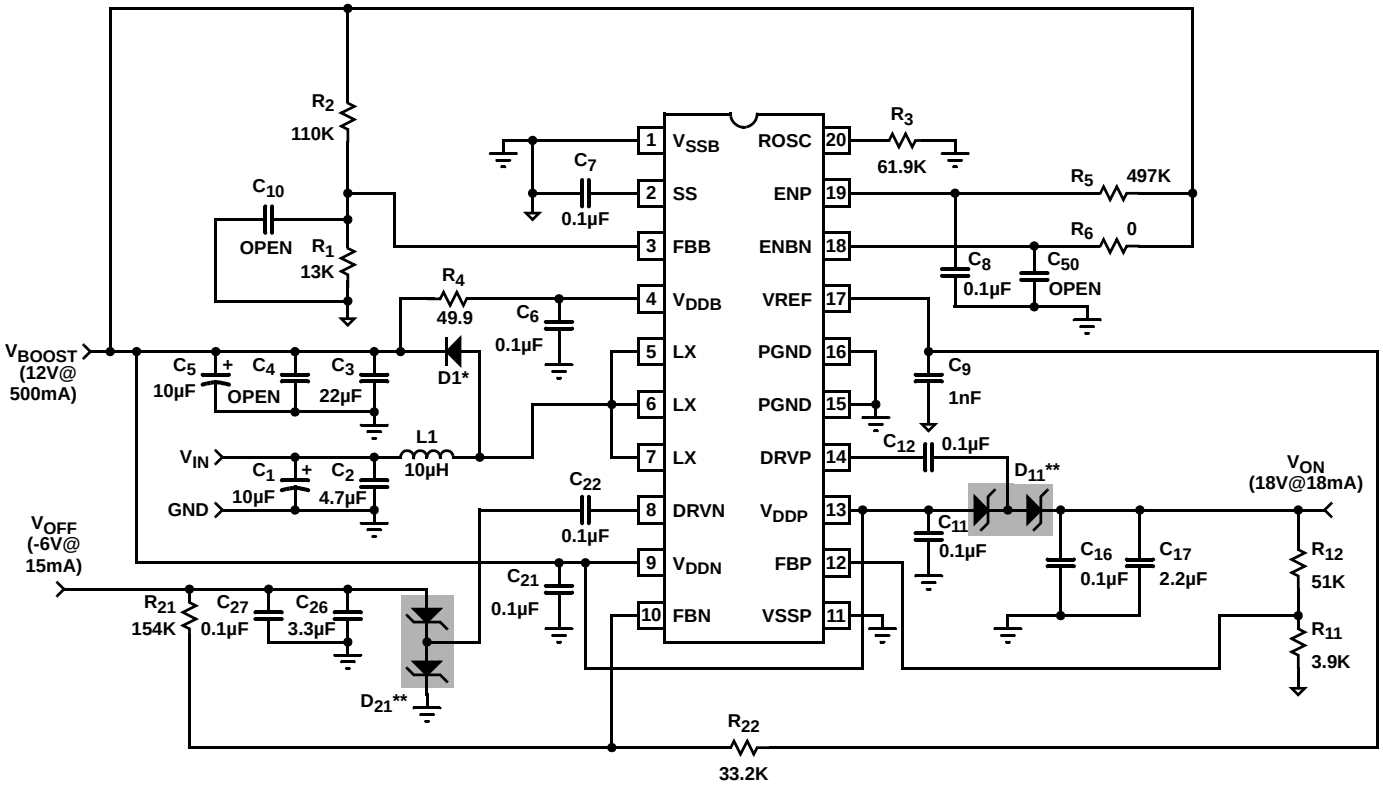
PCB Layout Guidelines

Careful layout is critical in the successful operation of the application. The following layout guidelines are recommended to achieve optimum performance.

- V_{REF} and V_{DDB} bypass capacitors should be placed next to the pins.
- Place the boost converter diode and inductor close to the LX pins.
- Place the boost converter output capacitor close to the PGND pins.
- Locate feedback dividers close to their respected feedback pins to avoid switching noise coupling into the high impedance node.
- Switching output PCB traces should not cross, or be laid out adjacent to, feedback traces without using a grounded shielding trace or layer. This is to prevent undesirable switching interactions coupling into the feedback inputs.
- Place the charge pump feedback resistor network after the diode and output capacitor node to avoid switching noise.
- All low-side feedback resistors should be connected directly to V_{SSB}. V_{SSB} should be connected to the power ground close at one point only.

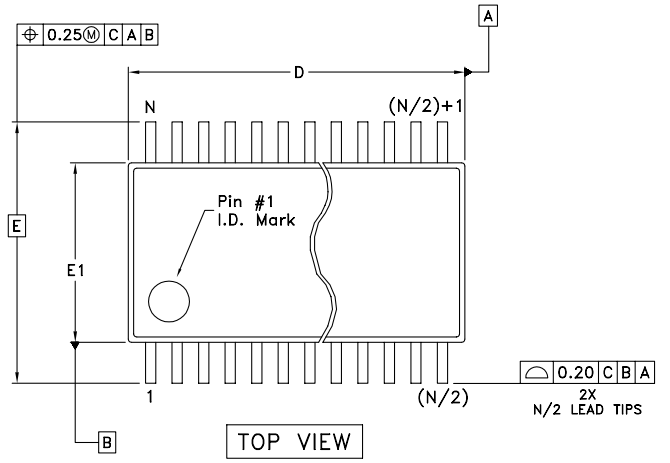
A demo board is available to illustrate the proper layout implementation.

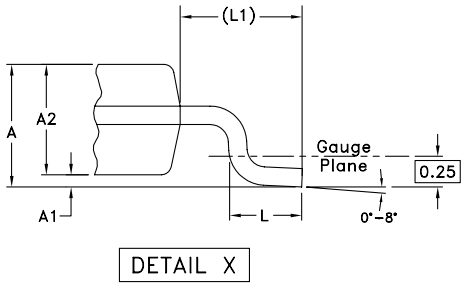
Typical Application Circuit

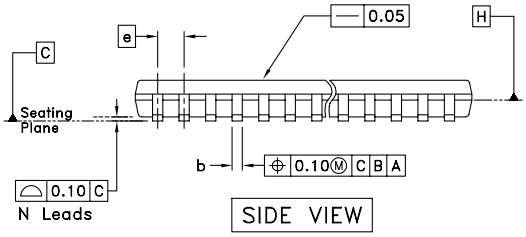


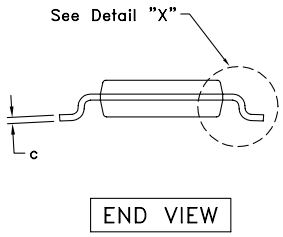
* MBRM120LT3
** BAT54S

TSSOP Package Outline Drawing







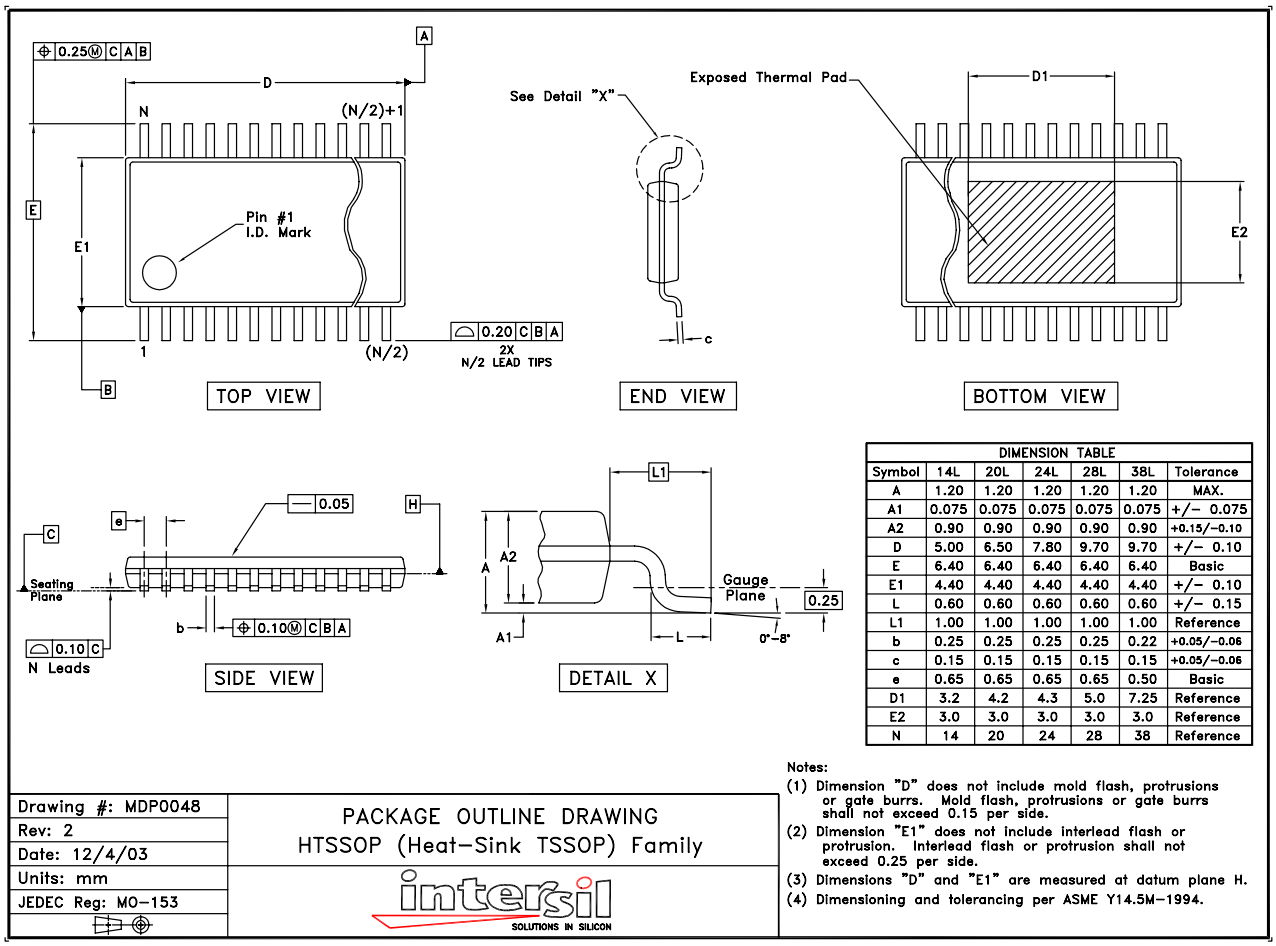


DIMENSION TABLE						
Symbol	14 Lead	16 Lead	20 Lead	24 Lead	28 Lead	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.10	0.10	0.10	0.10	0.10	+/− 0.05
A2	0.90	0.90	0.90	0.90	0.90	+/− 0.05
D	5.00	5.00	6.50	7.80	9.70	+/− 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/− 0.10
L	0.60	0.60	0.60	0.60	0.60	+/− 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.25	+0.05/−0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/−0.06
e	0.65	0.65	0.65	0.65	0.65	Basic

Drawing #: MDP0044	PACKAGE OUTLINE DRAWING TSSOP (Thin−Shrink Small Outline Package) Family
Rev: E	
Date: 12/11/02	
Units: mm	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO−153	

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

HTSSOP Package Outline Drawing



DIMENSION TABLE						
Symbol	14L	20L	24L	28L	38L	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	0.075	0.075	+/- 0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
D	5.00	6.50	7.80	9.70	9.70	+/- 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	0.65	0.50	Basic
D1	3.2	4.2	4.3	5.0	7.25	Reference
E2	3.0	3.0	3.0	3.0	3.0	Reference
N	14	20	24	28	38	Reference

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

Drawing #: MDP0048	PACKAGE OUTLINE DRAWING HTSSOP (Heat-Sink TSSOP) Family
Rev: 2	
Date: 12/4/03	
Units: mm	
JEDEC Reg: MO-153	intersil SOLUTIONS IN SILICON

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