



## **Absolute Maximum Ratings**

### **Supply Voltages**

Between GNDs ..... -0.3V to +0.3V  
Between VCCs ..... -0.3V to +0.3V  
VCCs to GND ..... 0V to +3.8V

### **RF Input Voltages**

CLKIP, CLKIN to GND ..... 0V to VCC

### **HS Digital Input Voltages**

DI<0:11> ..... 0V to VCC

### **Output Termination Voltages**

DOUTP, DOUTN to GND ..... 0V to VCC

### **Temperature**

Operating Temperature..... -30 to +100 °C  
Case Temperature..... -15 to +85 °C  
Junction Temperature..... +120 °C  
Lead, Soldering (10 Seconds) ..... +220 °C  
Storage..... -40 to 125 °C

## Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
<b>ACCURACY</b>							
Differential Nonlinearity	DNL		2	±2			LSB
Integral Nonlinearity	INL		2	±2.5			LSB
<b>DYNAMIC PERFORMANCE</b>							
Spurious Free Dynamic Range	SFDR1	$F_{clk} = 800\text{MHz}$ , $F_{out} = 267\text{MHz}$	1	56			dBc
	SFDR2	$F_{clk} = 1000\text{MHz}$ , $F_{out} = 333\text{MHz}$	1	53			dBc
	SFDR3	$F_{clk} = 1300\text{MHz}$ , $F_{out} = 400\text{MHz}$	1	50			dBc
Signal Noise Ratio	SNDR						dB
Clock Feedthrough	FD						dB
<b>ANALOG SIGNAL OUTPUT (OUTP, OUTN)</b>							
Full-scale Output Range	$V_{FSS}$	Single Ended, 50Ω Termination to Ground	2	570	600	630	mV <sub>p-p</sub>
Full-scale Output Range	$V_{FSRS}$	Single Ended, 50Ω Termination to Ground (MIN=000h, MAX=FFFh)		-650	0		mV
Full-scale output swing	$V_{FSD}$	Differential with 50Ω Termination to Ground on each output	2	1140	1200	1260	mV <sub>p-p</sub>
Output current	$I_{OUT}$		3	12			mA
Rise Time	$T_{R,OUT}$	20%-80% with FSR output					ps
Fall Time	$T_{F,OUT}$	20%-80% with FSR output					ps
Settling Time	$T_{SETTL}$						ps
<b>CORE CLOCK INPUT (HCLKIP, HCLKIN)</b>							
Amplitude	$V_{CPP,HCLKI}$	Differential ECL	1	400	600	800	mVpp
Common Mode Voltage	$V_{CM,HCLKI}$		1	-0.8	-1.5	-2.0	V
Input Resistance	$R_{HCLKI}$		3	45	50	55	Ω
Input Capacitance	$C_{HCLKI}$						fF
Maximum Frequency	$F_{MAX,HCLKI}$		3	1300			MHz
Minimum Frequency	$F_{MIN,HCLKI}$		3	1			MHz
<b>CLOCK INPUT (LCLKIP, LCLKIN)</b>							
Amplitude	$V_{CPP,LCLKI}$	Differential LVDS	2	250	350	450	mVpp
Common Mode Voltage	$V_{CM,LCLKI}$		2	0.9	1.2	1.5	mV
Input Resistance	$R_{LCLKI}$		3	100			Ω
Maximum Frequency	$F_{MAX,LCLKI}$		3	325			MHz
Minimum Frequency	$F_{MIN,LCLKI}$		3	0.25			MHz
<b>CLOCK OUPUT (LCLKOP, LCLKON)</b>							
Amplitude	$V_{CPP,LCLKO}$		2	250	350	450	mVpp
Common Mode Voltage	$V_{CM,LCLKO}$		2	0.9	1.2	1.5	mV
Maximum Frequency	$F_{MAX,LCLKO}$		3	325			MHz
Minimum Frequency	$F_{MIN,LCLKO}$		3	0.25			MHz
<b>DIGITAL INPUTS (A&lt;0:11&gt;, B&lt;0:11&gt;, C&lt;0:11&gt;, D&lt;0:11&gt;)</b>							
Input High Voltage	$V_{IH}$		2	0.9			VCC
Input Low Voltage	$V_{IL}$		2	-0.4			0.4
Input Resistance	$R_{DIN}$						Ω
Setup Time	$t_{ST,DTHCK}$	From data input to LCLKO	3	300			ps
Hold Time	$t_{HL,DTHCK}$	From LCLKO to data input	3	-50			ps

## Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
<b>TERMINATION (VTT)</b>							
HCLKI Termination Voltage	VTT				-2.0		V
<b>REFERENCE (VREFA, VREFD)</b>							
Analog Reference	VREFA	Internally generated	3	-1.9	-2.0	-2.1	V
Digital Reference	VREFD	Internally generated	3	-1.9	-2.0	-2.1	V
Input Resistance	R <sub>VREF</sub>	For externally driven VREFA, VREFD	3	500	560	620	Ω
<b>POWER SUPPLY</b>							
Positive Supply	VCC			3.1	3.3	3.5	V
Negative Supply, Analog	VEEA			-5.4	-5.2	-5.0	V
Negative Supply, Digital	VEED			-5.4	-5.2	-5.0	V
Power Dissipation	P	Total dissipation			3300		mW
Power Dissipation	P <sub>VCC</sub>	Positive supply			500		mW
Power Dissipation	P <sub>VEEA</sub>	Negative supply, analog			500		mW
Power Dissipation	P <sub>VEED</sub>	Negative supply, digital			2300		mW
<b>OPERATING RANGE</b>							
Ambient Temperature	T <sub>A</sub>						°C
Junction Temperature	T <sub>J</sub>				120		°C

## Test Levels

TEST LEVEL	TEST PROCEDURE
1	100% production tested at T <sub>A</sub> = 25C <sup>1,2</sup>
2	Sample tested at T <sub>A</sub> = 25C unless other temperature is specified <sup>1</sup>
3	Guaranteed by design and/or characterization testing

<sup>1</sup> All tests are continuous, not pulsed. Therefore, T<sub>J</sub> (junction temperature) > T<sub>C</sub> (case temperature) > T<sub>A</sub> (ambient temperature). This is the normal operating condition and is more stressful than a pulsed test condition.

<sup>2</sup> The tests are conducted with the power set to VCC<sub>MIN</sub> and to VCC<sub>MAX</sub>.



### Pad Layout

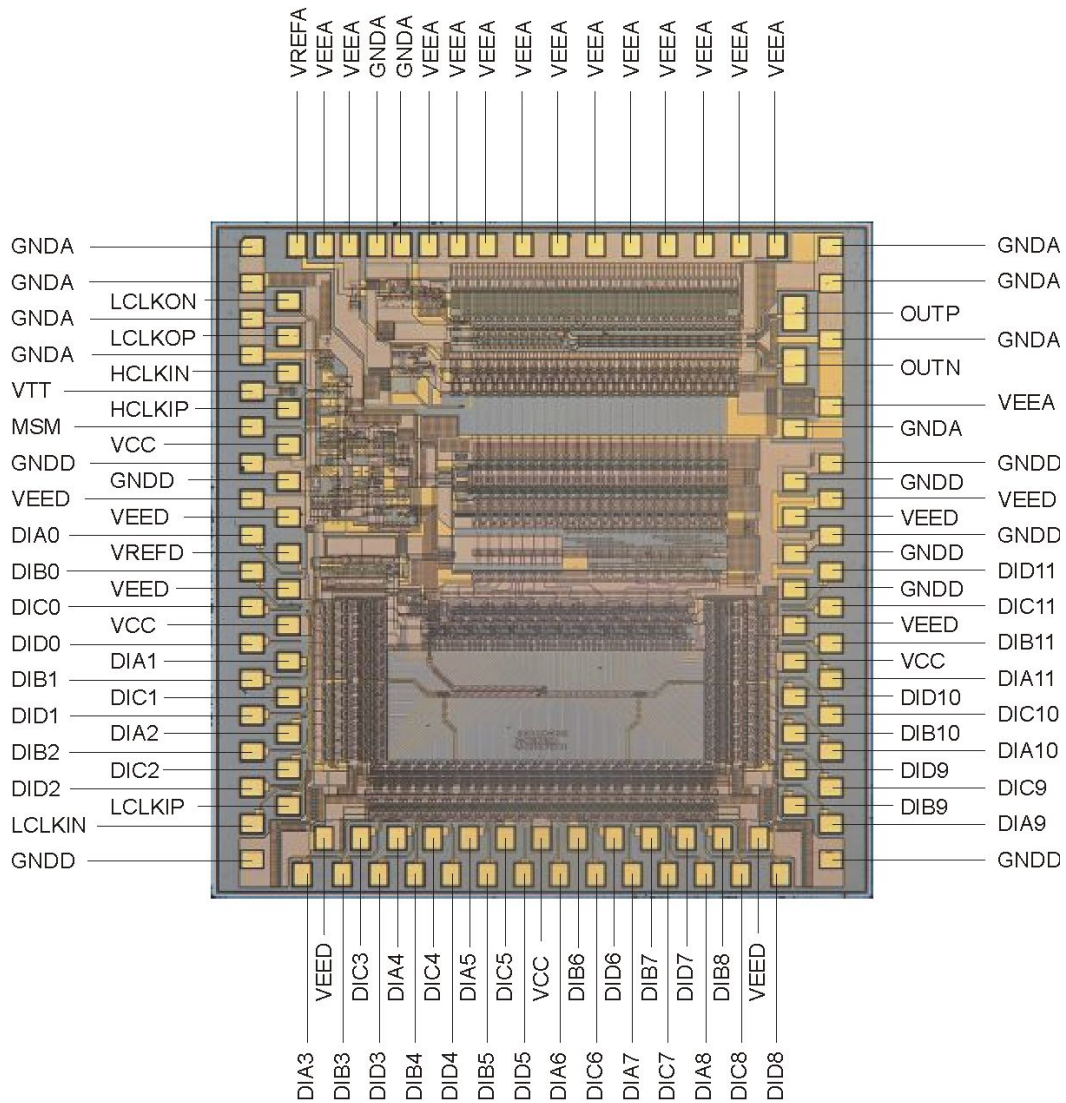


Figure 3 - RDA012M4MS pad layout.

## Theory of Operation

For best dynamic and static performance, the DAC employs 6-bit segmentation. The 3.3V NMOS compatible 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce the data skew. The four-channel data are combined together by the 48:12 MUX and latched again. The 6 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 6 LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master slave flip-flop to reduce the switching glitch. The decoded 6 MSB data drive 63 identical current switches, and the 6 LSB data drive 6 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output.

The DAC output full-scale voltage follows the relationship  $V_{FS} = 0.3xV_{REF}$ . An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience. The reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate,

temperature-compensated external voltage reference.

The timing diagram is shown in figure 3. The 1.3GHz external clock (HCLK) is divided by 2 and 4 resulting in the MUX internal selection signals S0 and S1. A low-speed clock (LCLK) is provided to drive the external digital. The four-channel data input are latched with an internal clock that is synchronized with the LCLK. Controlled by S0 and S1, input data are fed to the 1.3GS/s DAC in the order shown.

For applications requiring two MUXDACs, such as quadrature modulation, the RDA012M4MS offers master and slave mode operation. This provides synchronization between the two MUXDACs in a straightforward manner. Figure 4 illustrates two MUXDACs in an I-Q configuration and 1 GS/s conversion rate. The I-MUXDAC is in master mode and the Q-MUXDAC is in slave mode. The master MUXDAC generates an LVDS compatible 250MHz clock signal that is input to the slave MUXDAC where it is used to synchronize the generation of the select signal for the input muxes. The slave device then feeds this clock to the FPGA clock driver. For proper synchronization, the delay associated with the LVDS clock signal from master to slave MUXDAC must not exceed one clock period of the high-speed clock.

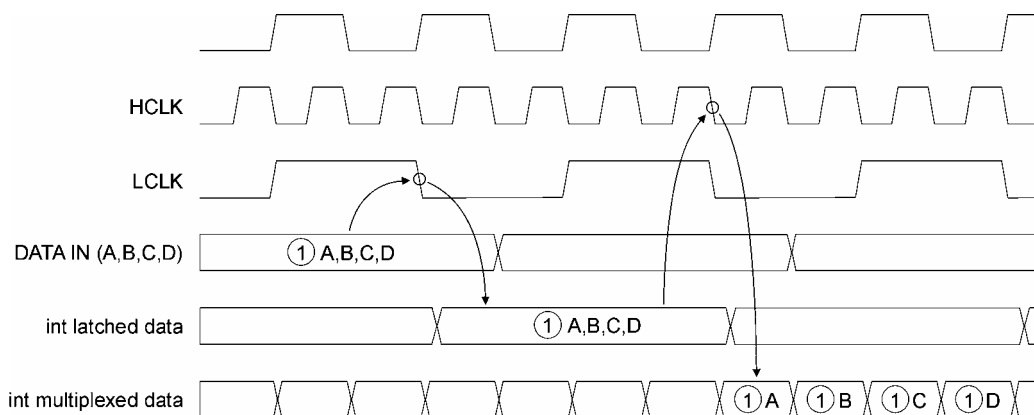


Figure 4 - Input Timing Diagram.



## Signal Description

### HIGH SPEED INPUT CLOCK.

The RDA012M4MS high-speed clock input is differential and can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used. The HCLKIP and HCLKIN inputs, are internally terminated with  $50\ \Omega$  to VTT which should be connected to a well decoupled  $-2.0$  volt supply. Since the MUXDAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter ( $\sim 100$ fs). A 500MHz MUXDAC output demands a white noise induced clock jitter of less than 250fs for a 10-bit equivalent, 62dB SNDR.

### DATA INPUT.

The data inputs are 3.3V NMOS-compatible. The data is interleaved according to significant bit. For example, consecutive data pins will occur as A0, B0, C0, D0, A1, B1, etc.

### OUTPUT CLOCK.

Output clock LCLKOP and LCLKON are supplied for the DSP/FPGA/ASIC in slave mode, or connected to another MUXDAC if in master mode. They are LVDS compliant and needs to be terminated with a  $100\ \Omega$  resistor in front of the clock driver for the ASIC/DSP.

For application convenience, the data input's setup and hold time is specified with respect to the LCLKO. It should be noted that LCLKOP and LCLKON are driven by the MUXDAC and the waveforms of these signals are better defined at the receiver end; that is, near the ASIC/DSP chip that provides the input data for the MUXDAC. The system designer should consider the delay associated with the signal routing in the system's timing budget.

In figure 6, the setup and hold time of the LCLK to data transition are defined at the MUXDAC side. Data transitions of the data input have to occur during the "Valid Data Transition Window." The timing margin seen from the MUXDAC is  $T_P - T_S$  where  $T_P$  is the LCLKO period and  $T_S$  is the setup time, assuming that the ASIC chip takes LCLKO as the clock input and its outputs are latched at the falling edge of the clock.

From the ASIC/DSP end, however, the timing margin is decreased by the amount equal to the sum of the data delay and clock delay between the two chips, as noted in the lower part of the diagram.

### ANALOG OUTPUT.

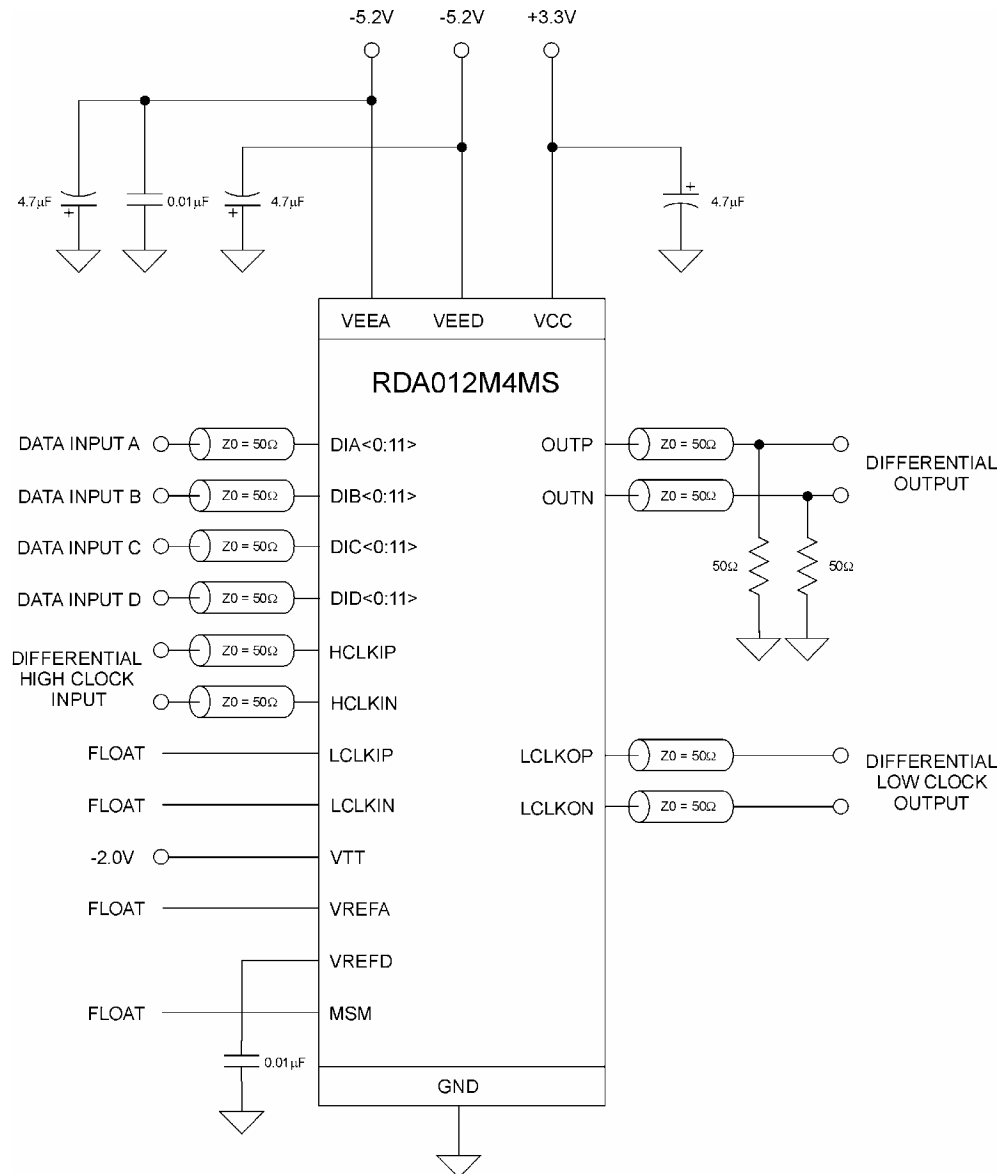
The outputs DACOUTP and DACOUTN should both be connected though a  $50\ \Omega$  resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage. The device is optimized to perform best when connected to a voltage between 0 and 1 volt, however. For reliable operation, the output termination voltage should not exceed 3 volts.

### REFERENCE.

VREFA is provided for added control of the full-scale amplitude output. The internal reference circuit is designed to provide  $-2.0$  volts, which can change up to  $\pm 5\%$  as the supply voltage and/or operating temperature changes. If the user prefers accurate absolute full-scale, use an external voltage reference with low output impedance to override the internal reference. The output full-scale voltage follows the relationship  $V_{FS} = 0.3 \times V_{REF}$ . Note that the MUXDAC is optimized to have the best performance with a reference voltage of  $-2.0$  volts. The output resistance of the reference node is  $560\ \Omega \pm 10\%$ . VREFD allows adjusting of the digital circuitry bias point for varying input voltage swings. In most cases, VREFD should be bypassed to GND.



### Typical Operating Circuit



**Figure 5 - RDA012M4MS typical operating circuit using the internal voltage reference.**

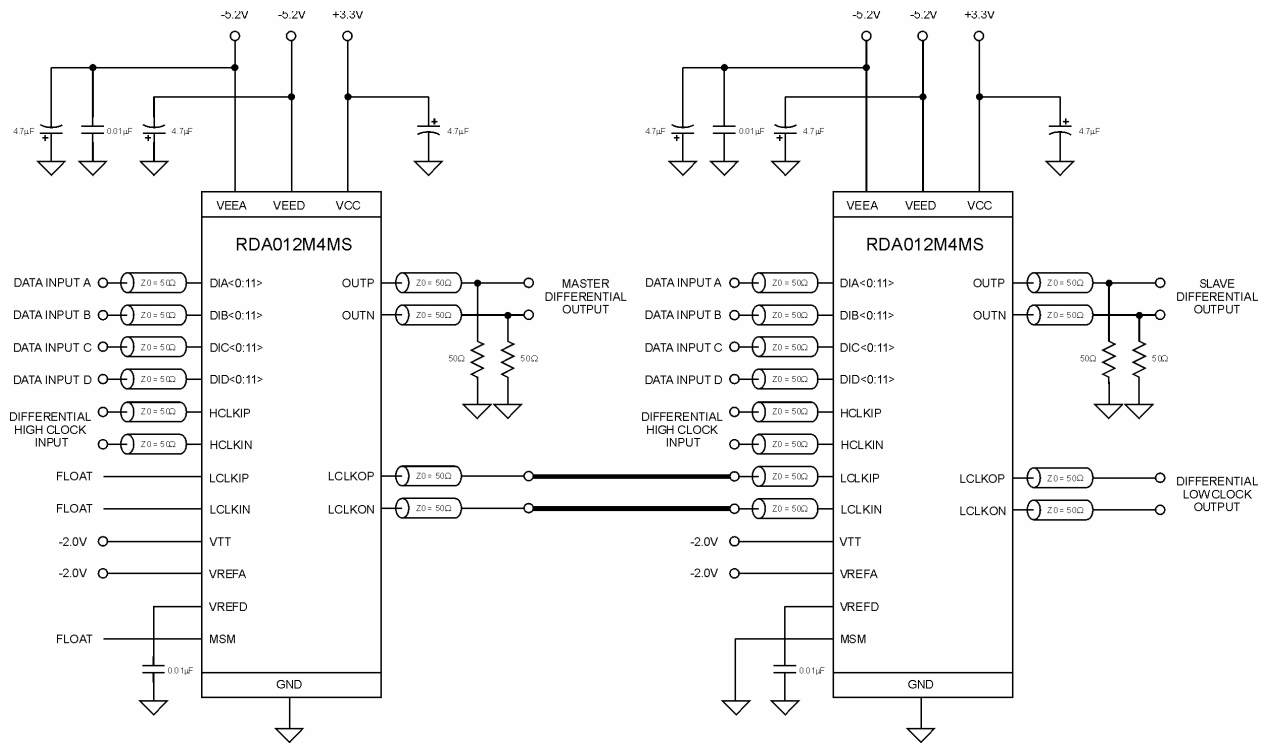


Figure 6 - RDA012M4MS typical operating circuit in master-slave mode using external voltage reference.

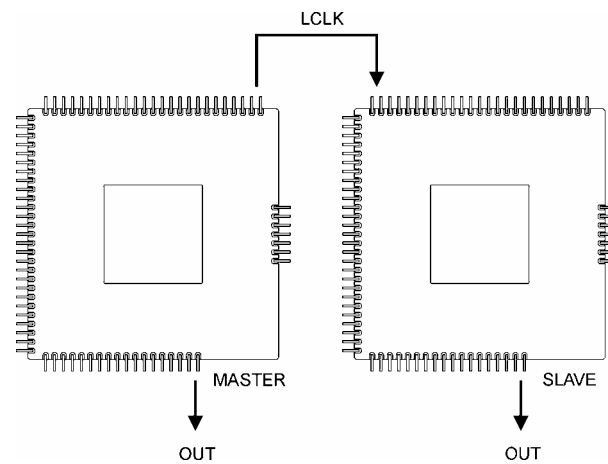


Figure 7 - RDA012M4MS recommended placement in master-slave mode to minimize LCLK routing.

## Typical Performance

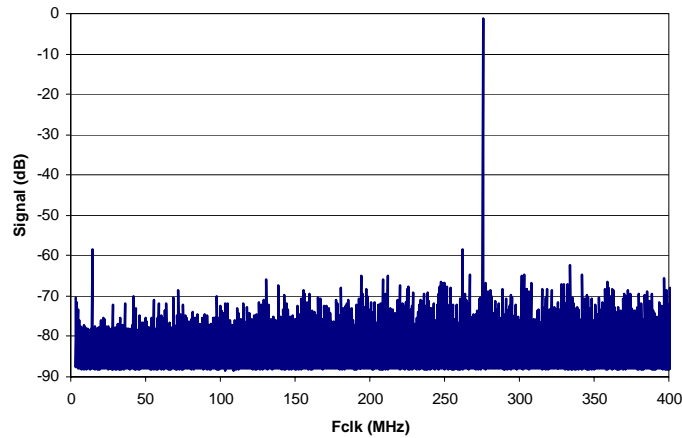


Figure 8 - Output spectrum at Fclk=800MHz, Fout=270MHz

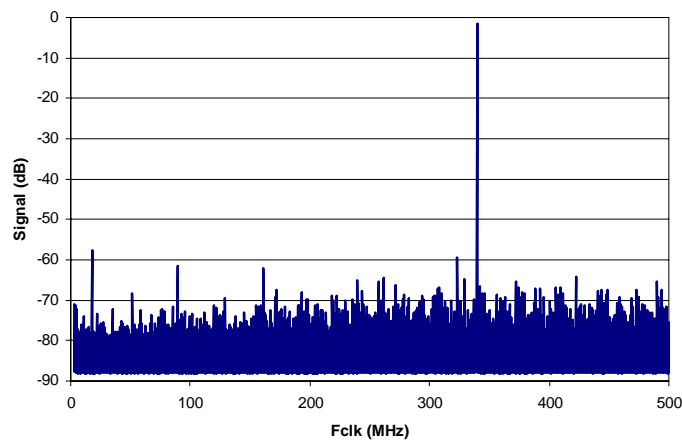


Figure 9 - Output spectrum at Fclk=1000MHz, Fout=340MHz

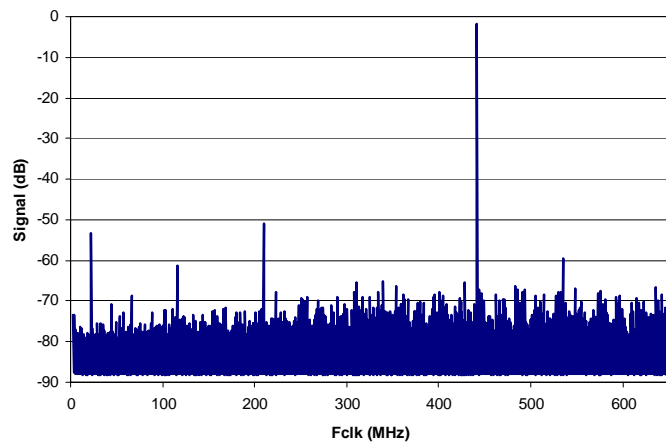
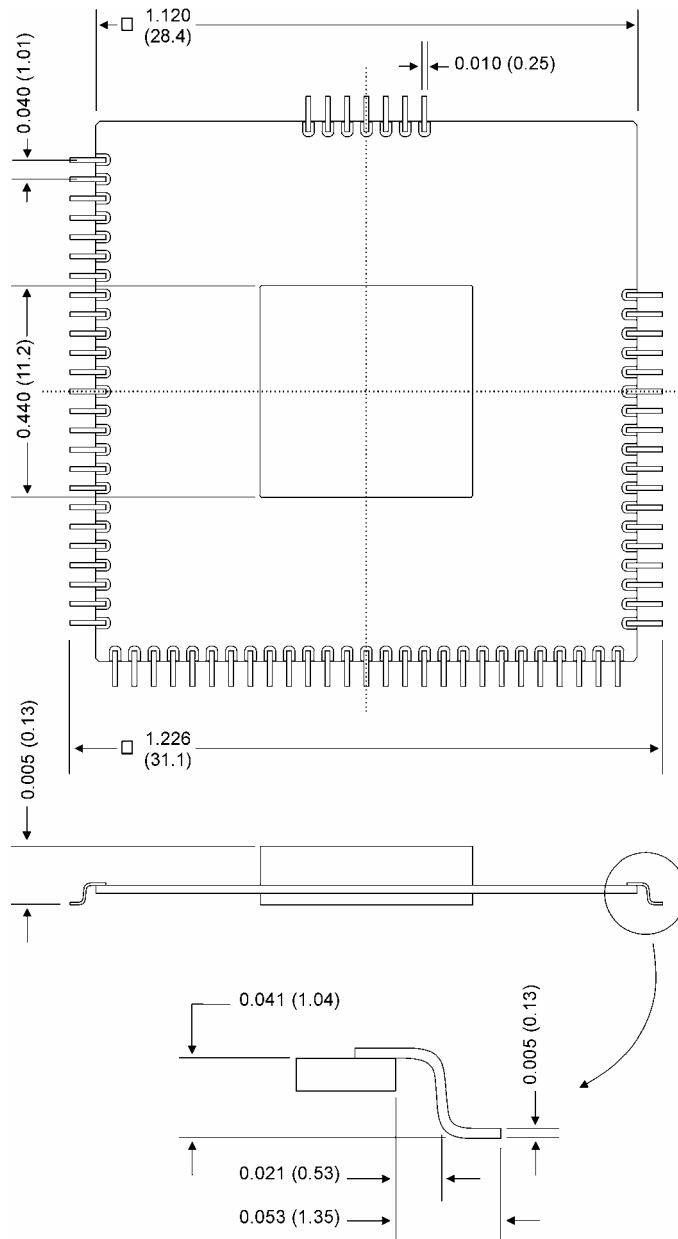


Figure 10 - Output spectrum at Fclk=1300MHz, Fout=340MHz

### Package Information

The package is a 77 pin HSD with a heat sink slug on the package's bottom. The leads are gull-winged

formed and trimmed to 0.053 inch (1.35 mm) in length.



**Figure 11 - RDA012M4MS-HD package, dimensions shown in inches (mm).**

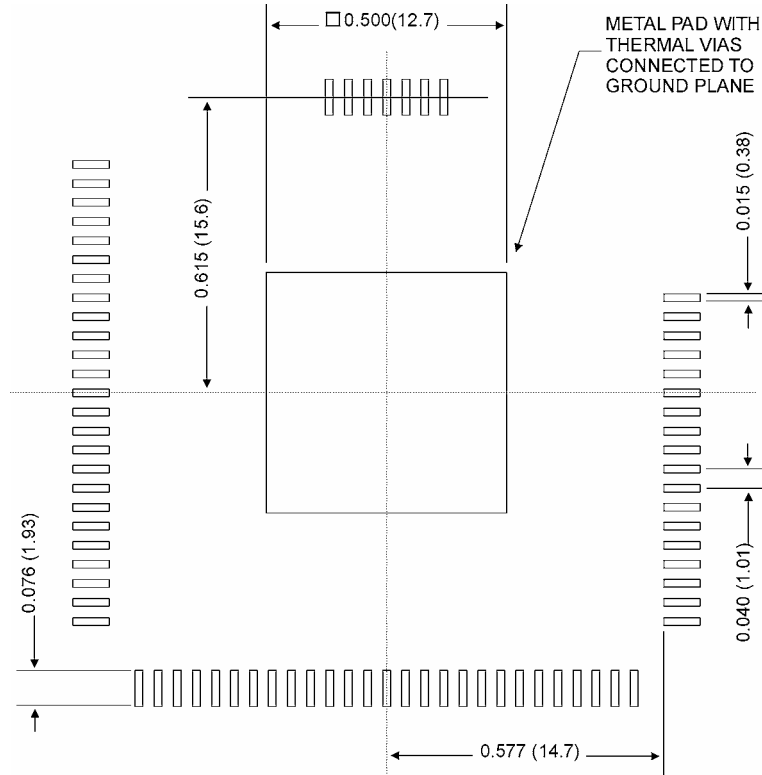


Figure 12 - RDA012M4MS-HD footprint, dimensions shown in inches (mm).