

FAN7380 Half-Bridge Gate Driver

Features

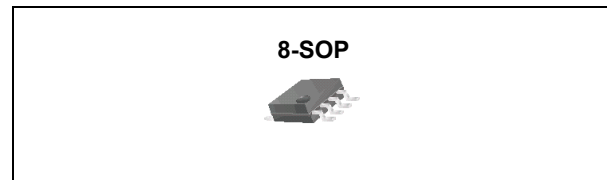
- Floating Channel Designed for Bootstrapping Operation to +600V
- Typically 90mA/180mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at $V_{CC}=V_{BS}=15V$
- V_{CC} & V_{BS} Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL-Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50ns
- Built-in 100ns Dead-Time Control Function
- Output in Phase with Input Signal

Typical Applications

- Fluorescent Lamp Ballast
- Compact Fluorescent Lamp Ballast

Description

The FAN7380 is a monolithic half-bridge gate drive IC for MOSFETs and IGBTs, which operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling technique give stable operation of high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S=-9.8V$ (typical) for $V_{BS}=15V$. The input logic level is compatible with standard TTL-series logic gates. The internal shoot-through protection circuit provides 100ns dead-time to prevent output switching devices from both conduction during transition periods. UVLO circuits for both channels prevent malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Output drivers typically source/sink at 90mA/180mA, respectively, which is suitable for fluorescent / compact fluorescent lamp ballast applications and the systems that require low di/dt noise.



Ordering Information

| Device | Package | Pb-Free | Operating Temperature | Packing |
|--------------------------|---------|---------|-----------------------|-------------|
| FAN7380M ⁽¹⁾ | 8-SOP | Yes | -40°C ~ +125°C | Tube |
| FAN7380MX ⁽¹⁾ | | | | Tape & Reel |

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Circuit

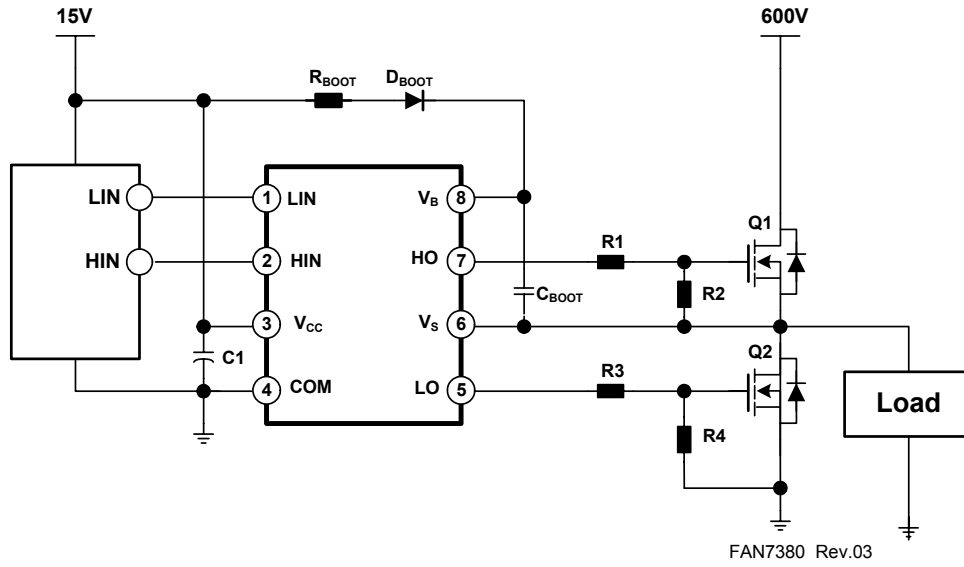


Figure 1. Application Circuit for Fluorescent Lamp Ballast

Internal Block Diagram

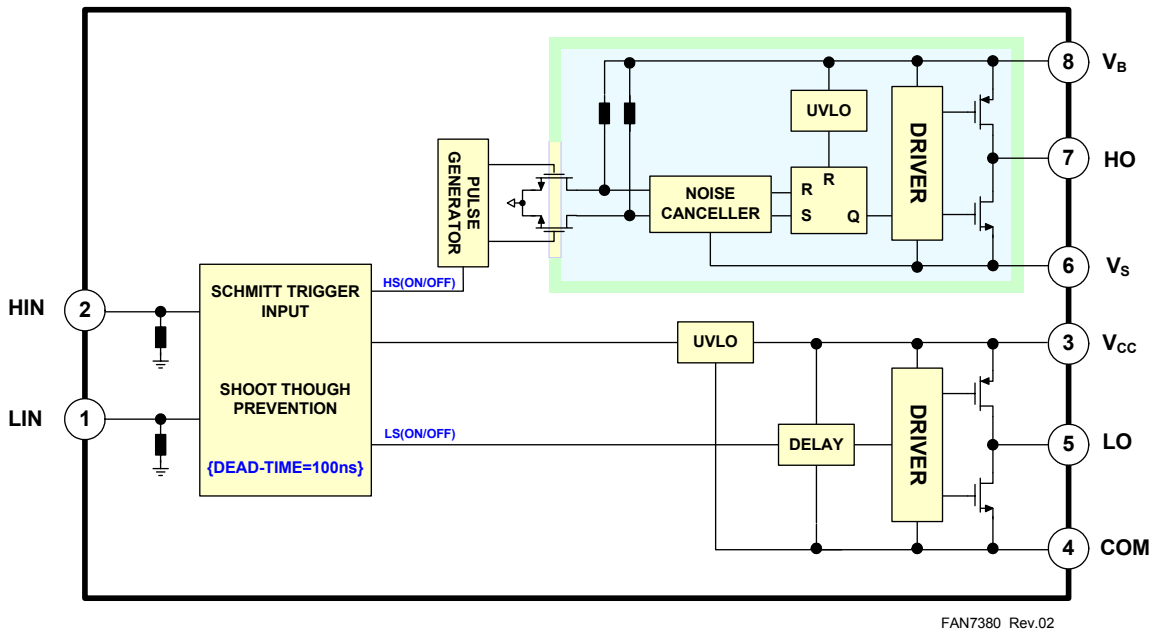


Figure 2. Functional Block Diagram of FAN7380

Pin Configuration

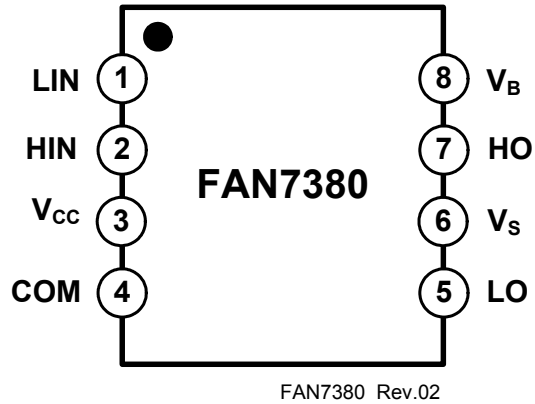


Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | I/O | Description |
|-------|-----------------|-----|--|
| 1 | LIN | I | Logic Input for Low-Side Gate Driver Output |
| 2 | HIN | I | Logic Input for High-Side Gate Driver Output |
| 3 | V _{CC} | I | Low-Side Supply Voltage |
| 4 | COM | | Logic Ground and Low-Side Driver Return |
| 5 | LO | O | Low-Side Driver Output |
| 6 | V _S | I | High-Voltage Floating Supply Return |
| 7 | HO | O | High-Side Driver Output |
| 8 | V _B | I | High-Side Floating Supply |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|---|-------------|--------------|-----------------------------|
| V_S | High-side offset voltage | V_B-25 | $V_B+0.3$ | V |
| V_B | High-side floating supply voltage | -0.3 | 625 | |
| V_{HO} | High-side floating output voltage HO | $V_S-0.3$ | $V_B+0.3$ | |
| V_{CC} | Low-side and logic-fixed supply voltage | -0.3 | 25 | |
| V_{LO} | Low-side output voltage LO | -0.3 | $V_{CC}+0.3$ | |
| V_{IN} | Logic input voltage (HIN, LIN) | -0.3 | $V_{CC}+0.3$ | |
| COM | Logic ground | $V_{CC}-25$ | $V_{CC}+0.3$ | |
| dV_S/dt | Allowable offset voltage slew rate | | 50 | V/ns |
| $P_D^{(2)(3)(4)}$ | Power dissipation | | 0.625 | W |
| θ_{JA} | Thermal resistance, junction-to-ambient | | 200 | $^{\circ}\text{C}/\text{W}$ |
| T_J | Junction temperature | | 150 | $^{\circ}\text{C}$ |
| T_S | Storage temperature | -50 | 150 | $^{\circ}\text{C}$ |

Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
 - JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
 - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed P_D under any circumstances.

Recommended Operating Ratings

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|----------|--|------------|----------|--------------------|
| V_B | High-side floating supply voltage | V_S+10 | V_S+20 | V |
| V_S | High-side floating supply offset voltage | $6-V_{CC}$ | 600 | |
| V_{HO} | High-side (HO) output voltage | V_S | V_B | |
| V_{LO} | Low-side (LO) output voltage | COM | V_{CC} | |
| V_{IN} | Logic input voltage (HIN, LIN) | COM | V_{CC} | |
| V_{CC} | Low-side supply voltage | 10 | 20 | |
| T_A | Ambient temperature | -40 | 125 | $^{\circ}\text{C}$ |

Static Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}) = 15.0V$, $T_A = 25^\circ C$, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------------------|---|---|------|------|------|---------|
| V_{CCUV+} V_{BSUV+} | V_{CC} & V_{BS} supply under-voltage positive going threshold | | 8.2 | 9.2 | 10.0 | V |
| V_{CCUV-} V_{BSUV-} | V_{CC} & V_{BS} supply under-voltage negative going threshold | | 7.6 | 8.7 | 9.6 | |
| V_{CCUVH} V_{BSUVH} | V_{CC} supply under-voltage lockout hysteresis | | | 0.5 | | |
| I_{LK} | Offset supply leakage current | $V_B = V_S = 600V$ | | | 50 | μA |
| I_{QBS} | Quiescent V_{BS} supply current | $V_{IN} = 0V$ or $5V$ | | 44 | 100 | |
| I_{QCC} | Quiescent V_{CC} supply current | $V_{IN} = 0V$ or $5V$ | | 70 | 180 | |
| I_{PBS} | Operating V_{BS} supply current | $f_{IN} = 20kHz$, rms value | | | 600 | μA |
| I_{PCC} | Operating V_{CC} supply current | $f_{IN} = 20kHz$, rms value | | | 610 | |
| V_{IH} | Logic "1" input voltage | | 2.5 | | | V |
| V_{IL} | Logic "0" input voltage | | | | 0.8 | |
| V_{OH} | High-level output voltage, $V_{BIAS} - V_O$ | $I_O = 20mA$ | | | 2.8 | V |
| V_{OL} | Low-level output voltage, V_O | | | | 1.2 | |
| I_{IN+} | Logic "1" input bias current | $V_{IN} = 5V$ | | 5 | 40 | μA |
| I_{IN-} | Logic "0" input bias current | $V_{IN} = 0V$ | | 1.0 | 2.0 | |
| I_{O+} | Output HIGH short-circuit pulse current | $V_O = 0V, V_{IN} = 5V$ with $PW \leq 10\mu s$ | 60 | 90 | | mA |
| I_{O-} | Output LOW short-circuit pulsed current | $V_O = 15V, V_{IN} = 0V$ with $PW \leq 10\mu s$ | 130 | 180 | | |
| V_S | Allowable negative V_S pin voltage for HIN signal propagation to HO | | | -9.8 | -7.0 | V |

Dynamic Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}) = 15.0V$, $V_S = COM$, $C_L = 1000pF$ and $T_A = 25^\circ C$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------|-------------------------------------|----------------------------|------|------|------|------|
| t_{on} | Turn-on propagation delay | $V_S = 0V$ | 70 | 135 | 200 | ns |
| t_{off} | Turn-off propagation delay | $V_S = 0V$ or $600V^{(5)}$ | 60 | 130 | 190 | |
| t_r | Turn-on rise time | | 160 | 230 | 290 | |
| t_f | Turn-off fall time | | 20 | 90 | 160 | |
| DT | Dead-time | | 80 | 120 | 190 | |
| MT | Delay matching, HS & LS turn-on/off | | | | 50 | |

Note:

5. This parameter guaranteed by design.

Typical Performance Characteristics

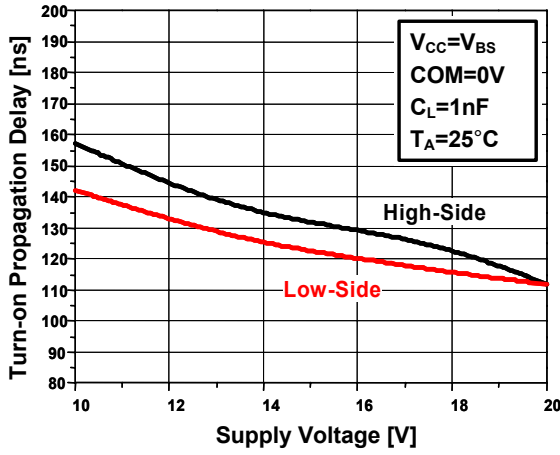


Figure 4. Turn-On Propagation Delay vs. Supply Voltage

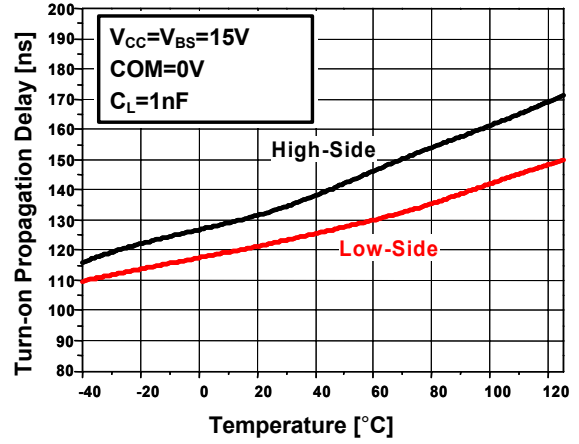


Figure 5. Turn-On Propagation Delay vs. Temp.

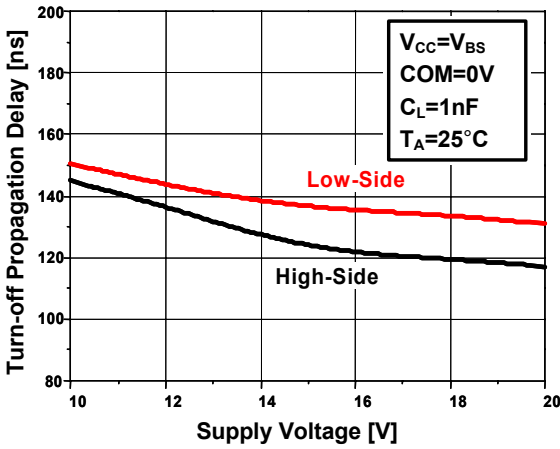


Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

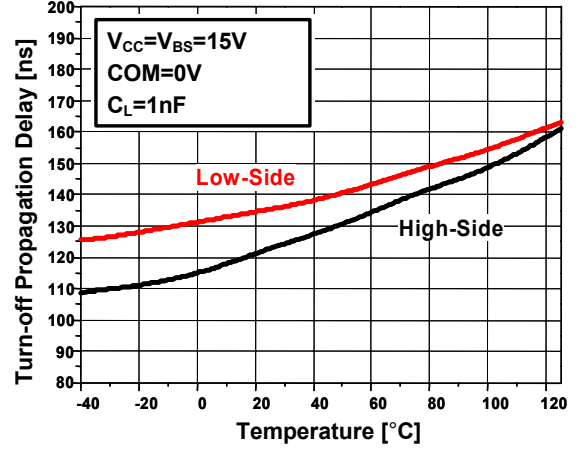


Figure 7. Turn-Off Propagation Delay vs. Temp.

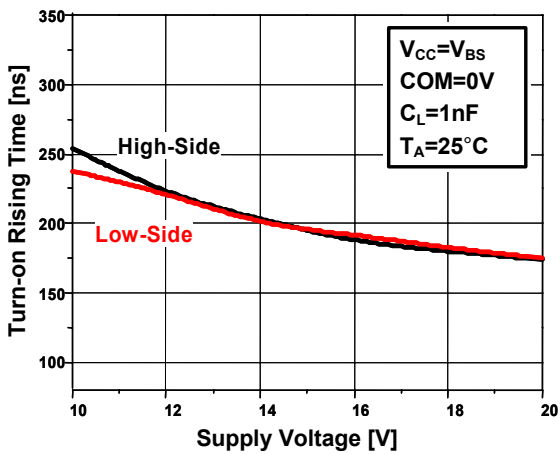


Figure 8. Turn-On Rising Time vs. Supply Voltage

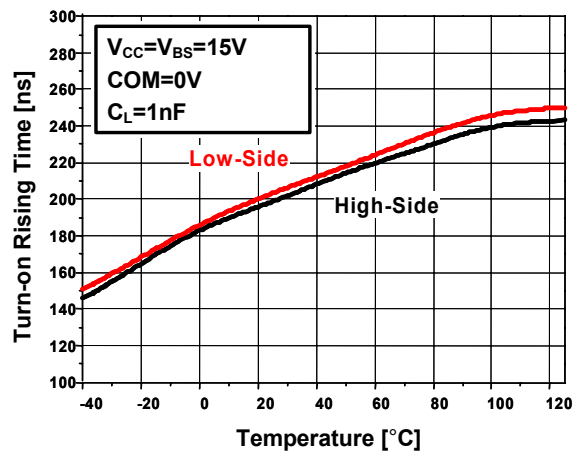


Figure 9. Turn-On Rising Time vs. Temp.

Typical Performance Characteristics (Continued)

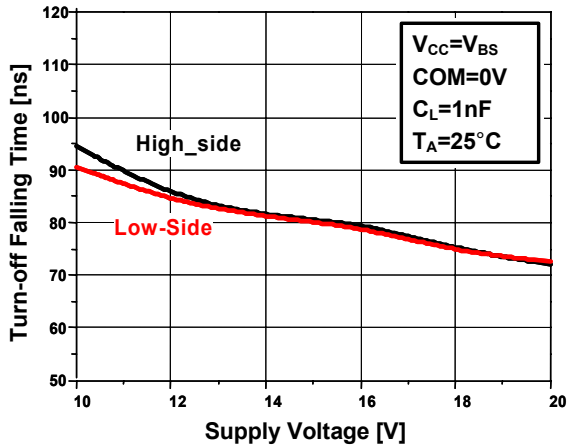


Figure 10. Turn-Off Falling Time vs. Supply Voltage

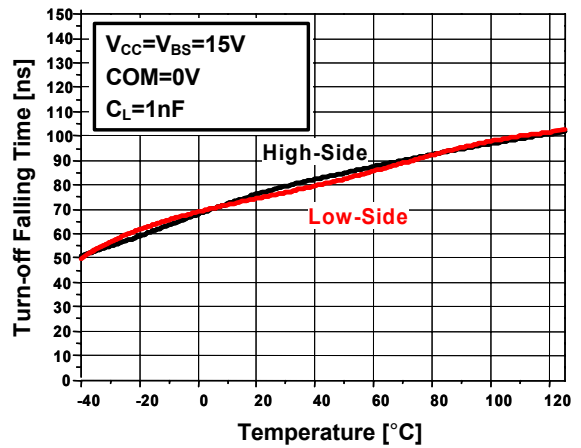


Figure 11. Turn-Off Falling Time vs. Temp.

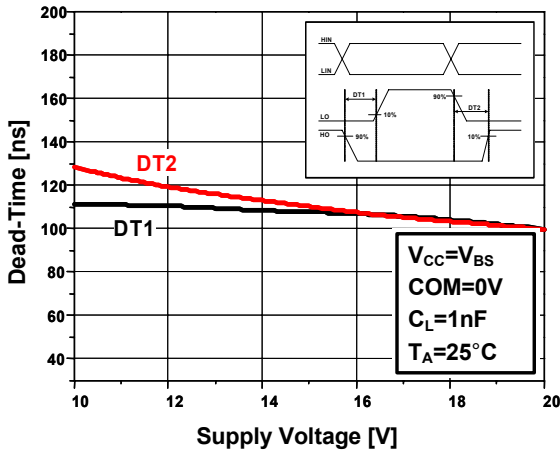


Figure 12. Dead-Time vs. Supply Voltage

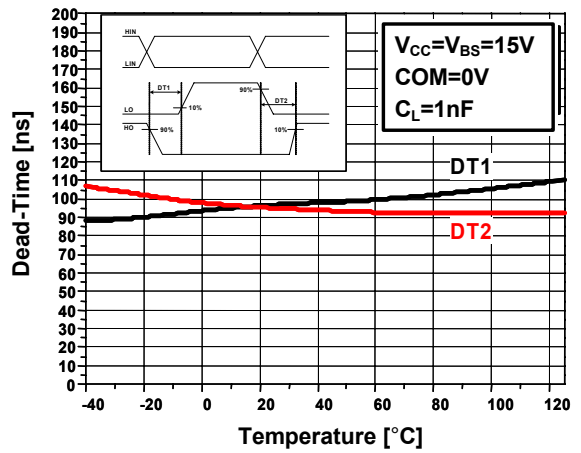


Figure 13. Dead-Time vs. Temp.

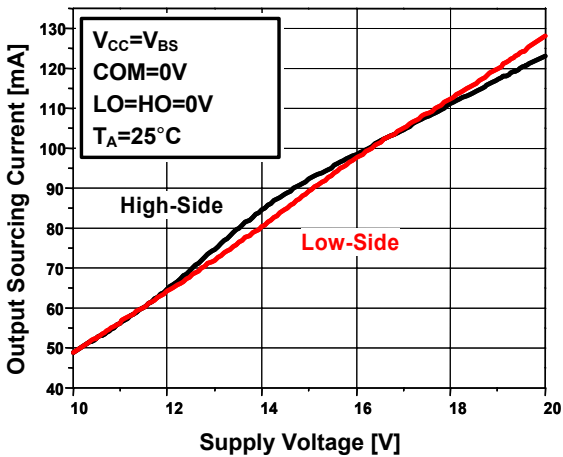


Figure 14. Output Sourcing Current vs. Supply Voltage

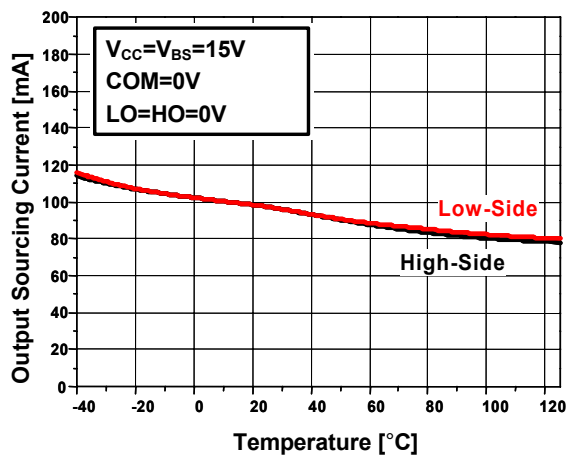


Figure 15. Output Sourcing Current vs. Temp.

Typical Performance Characteristics (Continued)

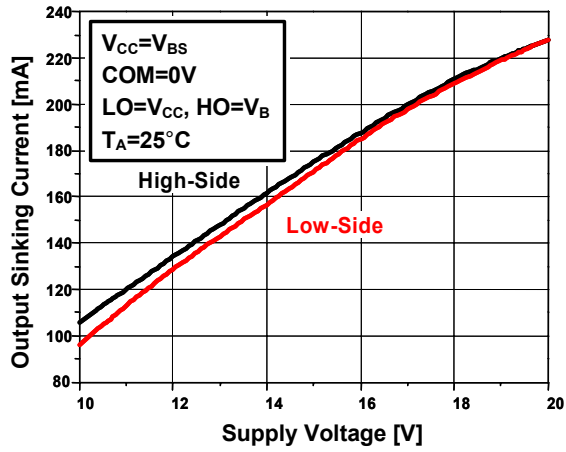


Figure 16. Output Sinking Current vs. Supply Voltage

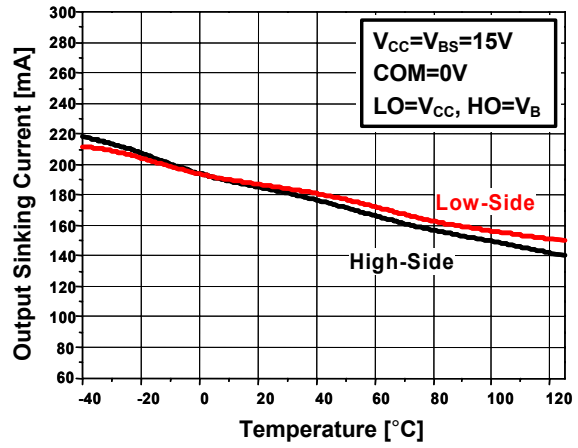


Figure 17. Output Sinking Current vs. Temp.

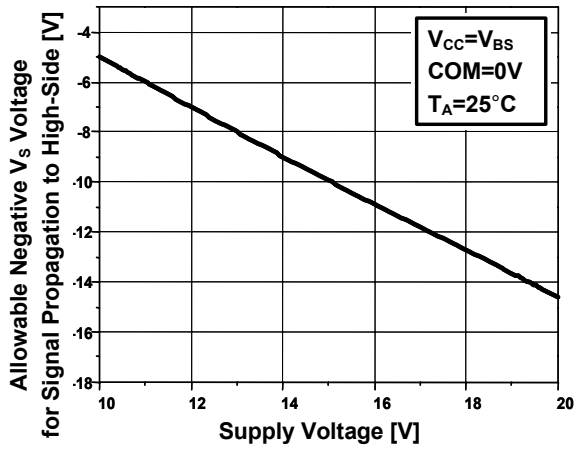


Figure 18. Allowable Negative V_S Voltage for Signal Propagation to High-Side vs. Supply Voltage

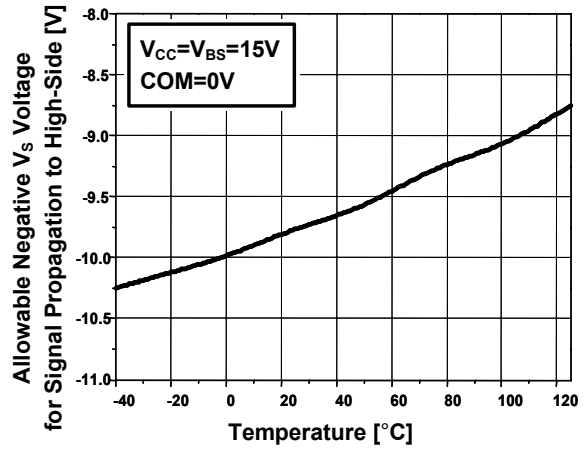


Figure 19. Allowable Negative V_S Voltage for Signal Propagation to High-Side vs. Temp.

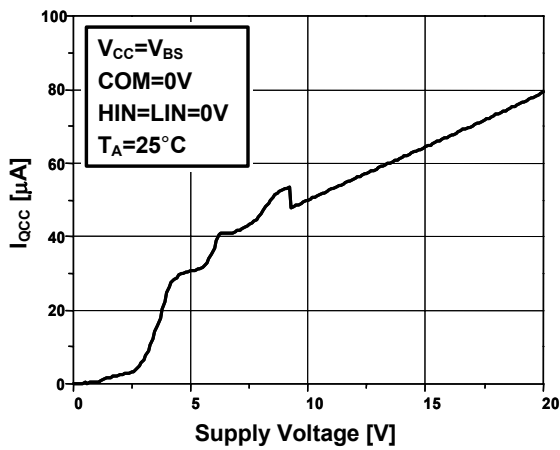


Figure 20. I_{QCC} vs. Supply Voltage

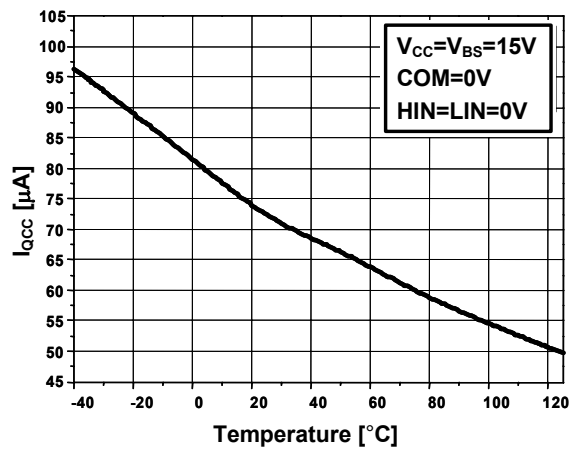


Figure 21. I_{QCC} vs. Temp.

Typical Performance Characteristics (Continued)

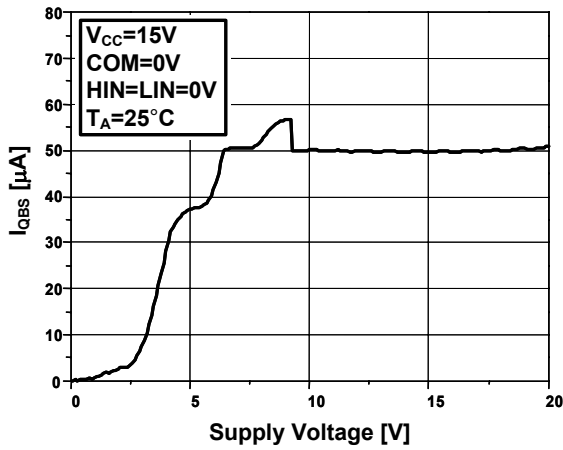


Figure 22. I_{QBS} vs. Supply Voltage

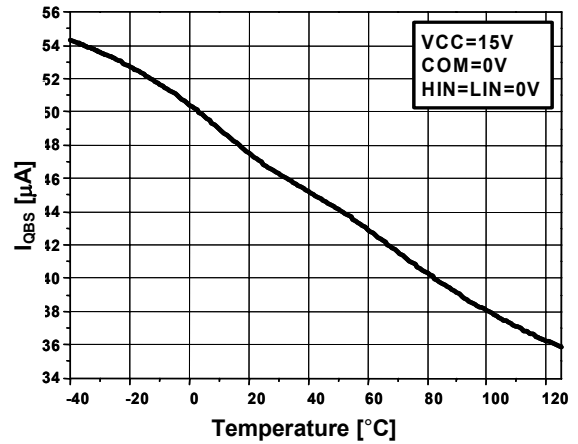


Figure 23. I_{QBS} vs. Temp.

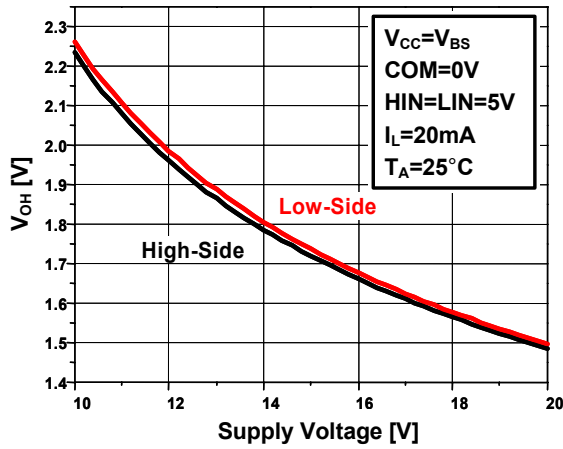


Figure 24. High-Level Output Voltage vs. Supply Voltage

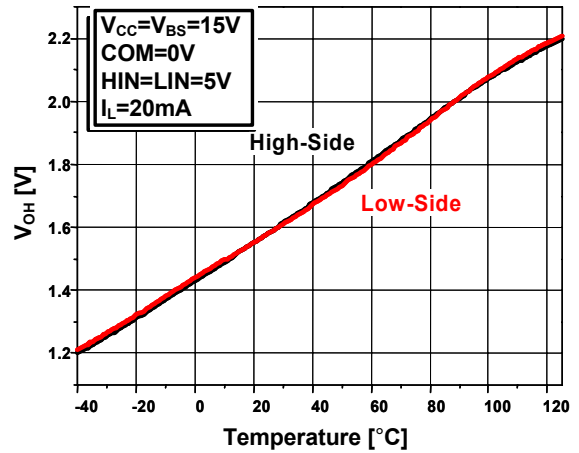


Figure 25. High-Level Output Voltage vs. Temp.

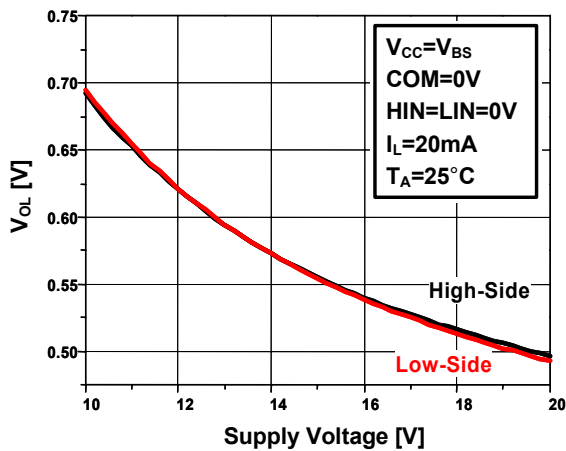


Figure 26. Low-Level Output Voltage vs. Supply Voltage

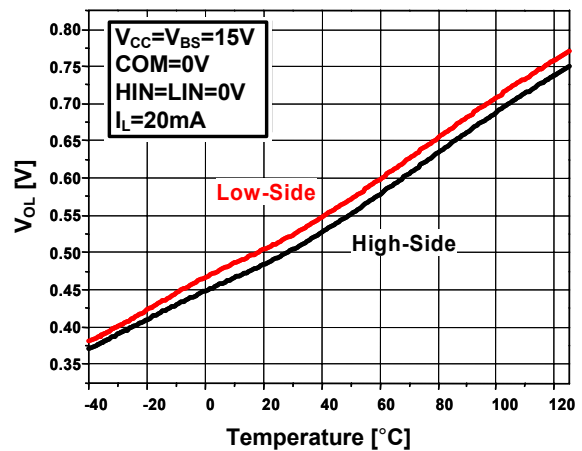


Figure 27. Low-Level Output Voltage vs. Temp.

Typical Performance Characteristics (Continued)

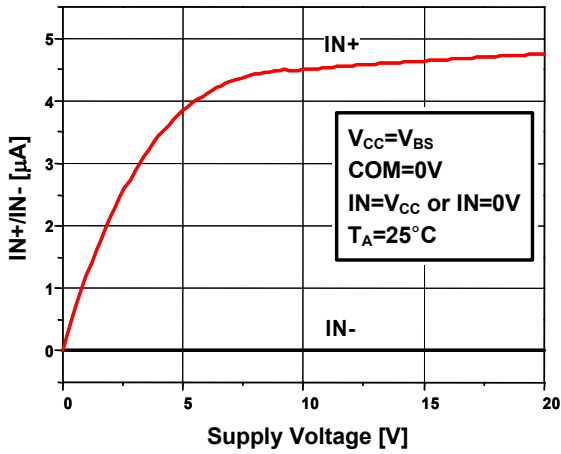


Figure 28. Input Bias Current vs. Supply Voltage

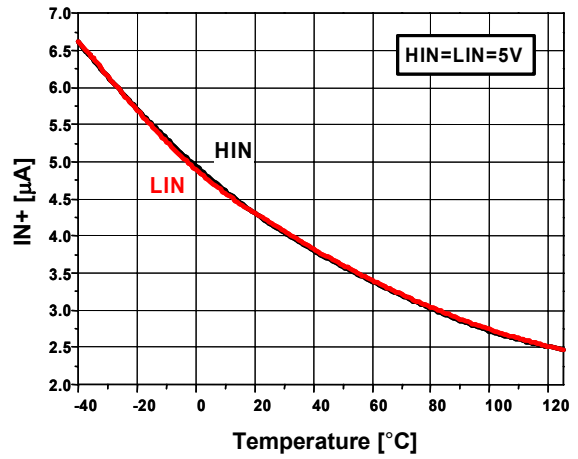


Figure 29. Input Bias Current vs. Temp.

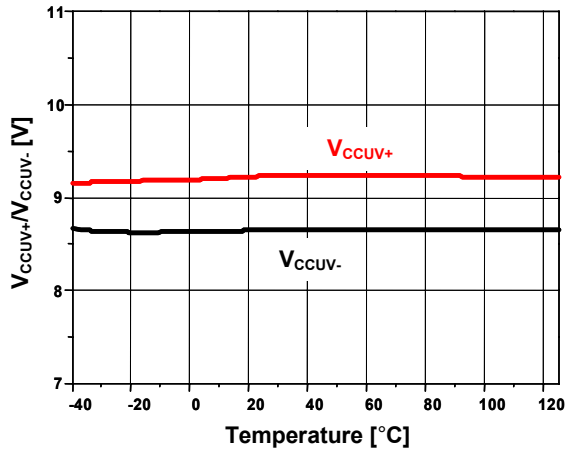


Figure 30. V_{CC} UVLO Threshold Voltage vs. Temp

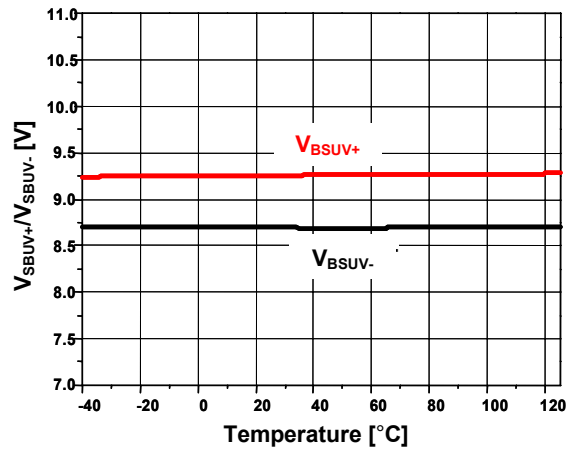


Figure 31. V_{BS} UVLO Threshold Voltage vs. Temp.

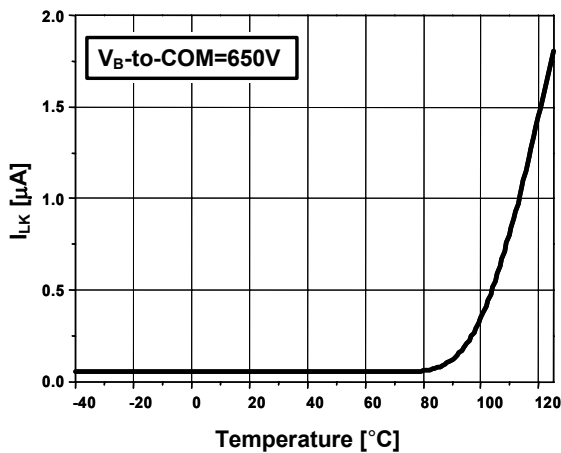


Figure 32. VB to COM Leakage Current vs. Temp.

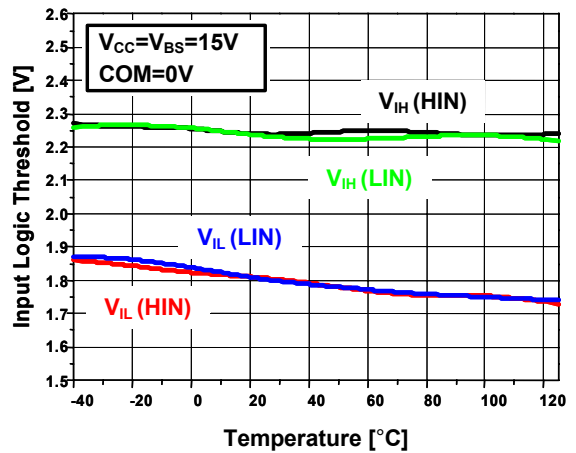


Figure 33. Input Logic Threshold vs. Temp.

Switching Time Definitions

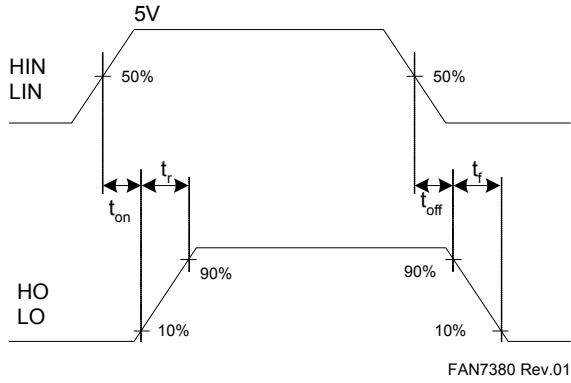


Figure 34. Switching Time Waveforms

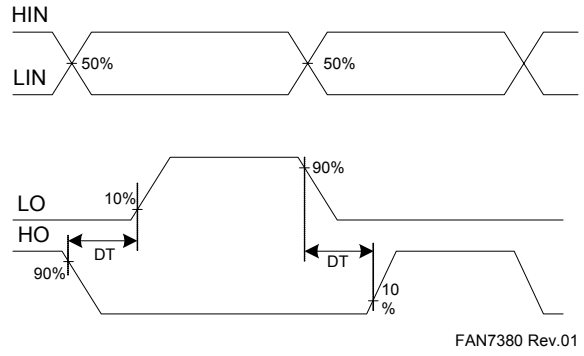



Figure 35. Internal Dead-Time Timing



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