

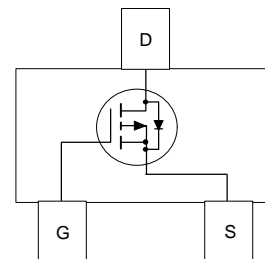
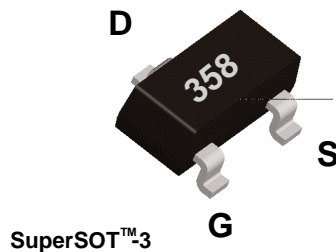
## FDN358P P-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

SuperSOT™-3 P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- -1.5 A, -30 V,  $R_{DS(ON)} = 0.125 \Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 0.20 \Omega @ V_{GS} = -4.5 \text{ V}$ .
- High power version of industry SOT-23 package: identical pin out to SOT-23; 30% higher power handling capability.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDN358P	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain/Output Current - Continuous - Pulsed	-1.5	A
		-5	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

## Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-28		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
			$T_J = 55\text{ }^\circ\text{C}$			-10
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}$ , $V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	-1	-1.5	-2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -1.5\text{ A}$		0.11	0.125	$\Omega$
			$T_J = 125\text{ }^\circ\text{C}$	0.15	0.21	
			$V_{GS} = -4.5\text{ V}$ , $I_D = -1.2\text{ A}$	0.175	0.2	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}$ , $V_{DS} = -5\text{ V}$	-5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}$ , $I_D = -1.5\text{ A}$		7		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		270		pF
$C_{oss}$	Output Capacitance			150		pF
$C_{rss}$	Reverse Transfer Capacitance			45		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -15\text{ V}$ , $I_D = -1\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		8	16	ns
$t_r$	Turn - On Rise Time			7	14	ns
$t_{D(off)}$	Turn - Off Delay Time			17	27	ns
$t_f$	Turn - Off Fall Time			10	1.8	ns
$Q_g$	Total Gate Charge		$V_{DS} = -5\text{ V}$ , $I_D = -1.5\text{ A}$ , $V_{GS} = -10\text{ V}$		6.5	9.1
$Q_{gs}$	Gate-Source Charge			1		nC
$Q_{gd}$	Gate-Drain Charge			1.1		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -0.42\text{ A}$ (Note 2)		-0.74	-1.2	V

Note:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

Typical  $R_{\theta JA}$  using the board layouts shown below on FR-4 PCB in a still air environment:



a.  $250\text{ }^\circ\text{C/W}$  when mounted on  
a  $0.02\text{ in}^2$  pad of 2oz Cu.

a



b.  $270\text{ }^\circ\text{C/W}$  when mounted on  
a  $0.001\text{ in}^2$  pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

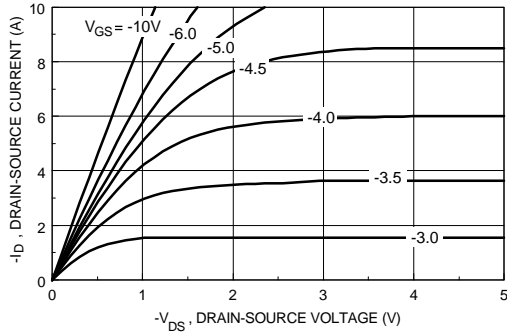


Figure 1. On-Region Characteristics.

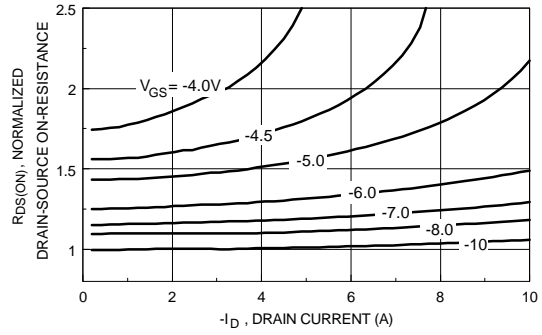


Figure 2. On-Resistance Variation with Drain Current and Gate

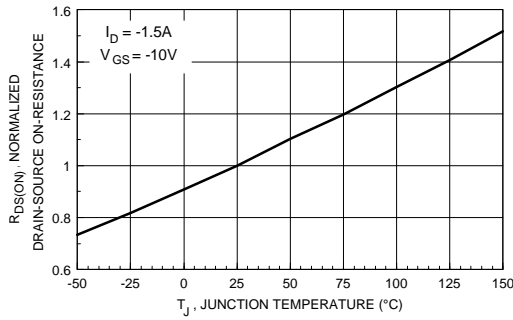


Figure 3. On-Resistance Variation with Temperature.

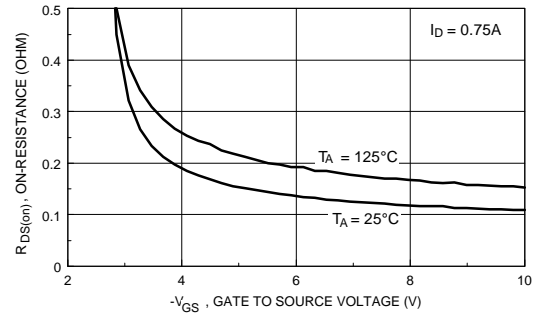


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

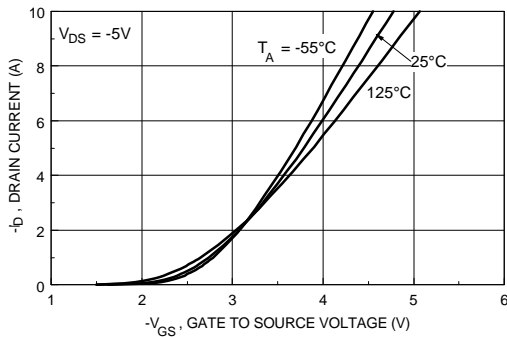


Figure 5. Transfer Characteristics.

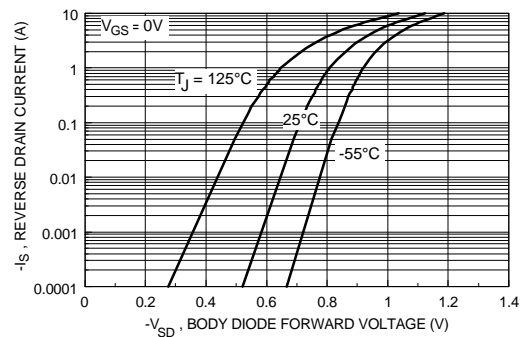


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics

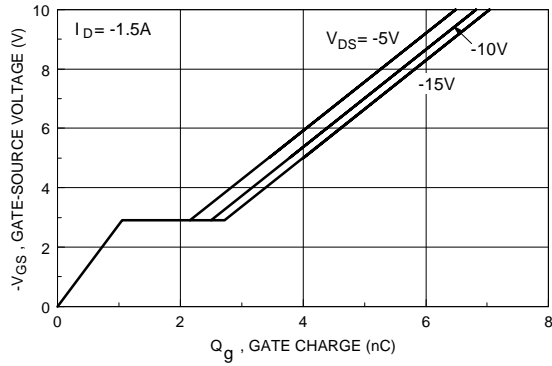


Figure 7. Gate Charge Characteristics.

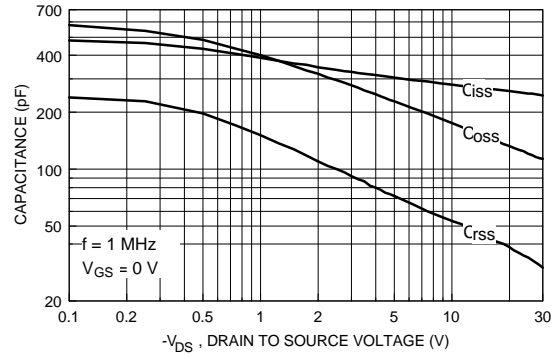


Figure 8. Capacitance Characteristics.

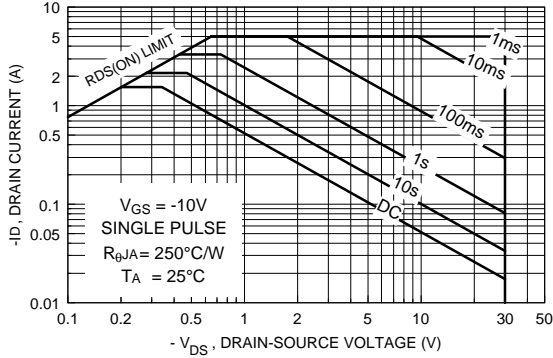


Figure 9. Maximum Safe Operating Area.

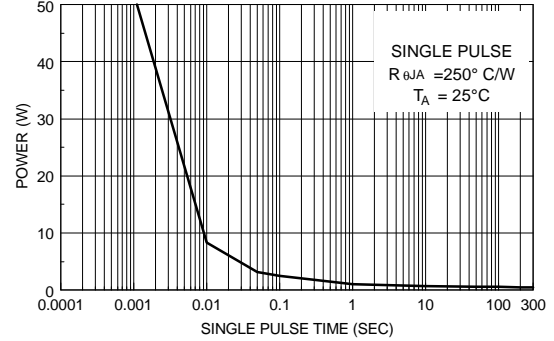


Figure 10. Single Pulse Maximum Power Dissipation.

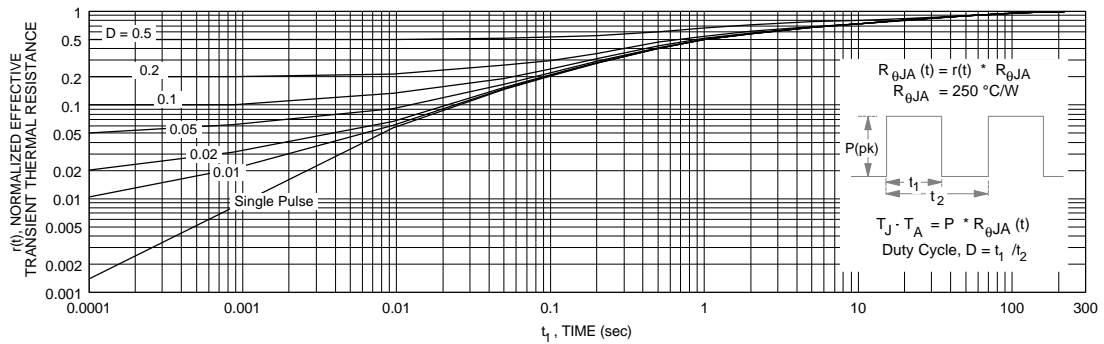


Figure 11. Transient Thermal Response Curve.