FAIRCHILD SEMICONDUCTOR®

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FIN12AC
µSerDes™ Low-Voltage 12-Bit Bi-Directional Serializer/Deserializer with Multiple Frequency Ranges

Features

- Low power consumption
- Fairchild proprietary low-power CTL interface
- LVCMOS parallel I/O interface:
  – 2mA source / sink current
  – Over-voltage tolerant control signals
- Parallel I/O power supply (V_{DDP}) range between 1.65V and 3.6V
- Analog power supply range of 2.5V to 3.05V
- Multi-mode operation allows for a single device to operate as Serializer or Deserializer
- Internal PLL with no external components
- Standby power-down mode support
- Small footprint packaging:
  – 32-terminal MLP and 42-ball BGA
- Built-in differential termination
- Supports external CKREF frequencies; 5MHz to 40MHz
- Serialized data rate up to 560Mb/s
- Voltage translation from 1.65V to 3.6V

Applications

- Microcontroller or pixel interfaces
- Image sensors
- Small displays: LCD, cell phone, digital camera, portable gaming, printer, PDA, video camera, automotive

Description

The FIN12AC is a 12-bit serializer capable of running a parallel frequency range between 5MHz and 40MHz. The frequency range is selected by the S1 and S2 control signals. The bi-directional data flow is controlled through use of a direction (DIRI) control pin. The devices can be configured to operate in a unidirectional mode only by hardwiring the DIRI pin. An internal Phase-Locked Loop (PLL) generates the required bit clock frequency for transfer across the serial link. Options exist for dual or single PLL operation, dependent upon system operational parameters. The device has been designed for low power operation and utilizes Fairchild proprietary low-power control Current Transistor Logic (CTL) interface. The device also supports an ultra low power power-down mode for conserving power in battery-operated applications.

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FIN12ACGFX	42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide	Yes	-30°C to +70°C	Tape and Reel
FIN12ACMLX	32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square	Yes	-30°C to +70°C	Tape and Reel

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Functional Block Diagram

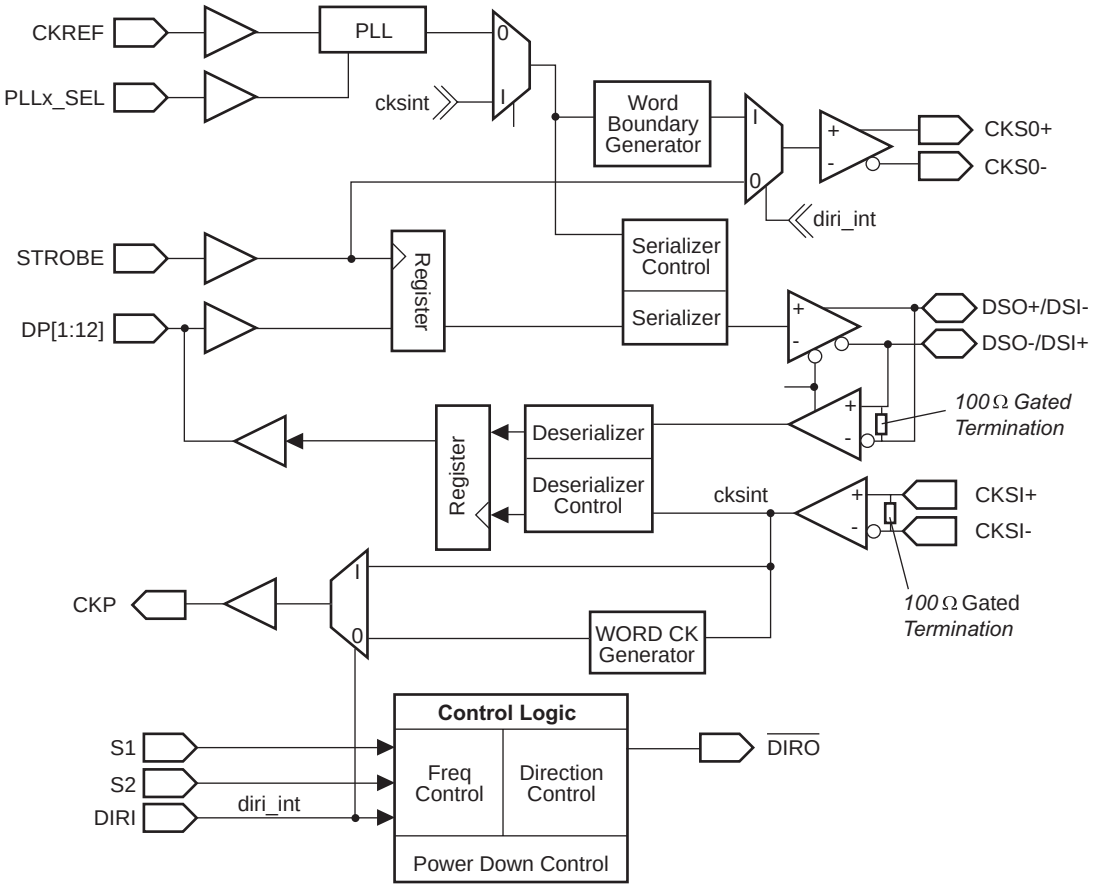
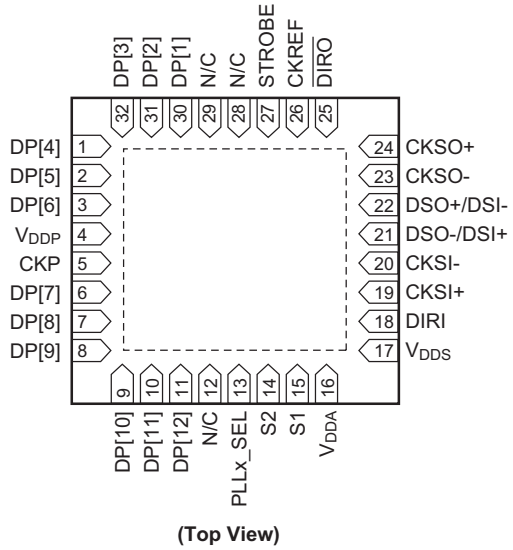


Figure 1. FIN12AC Block Diagram

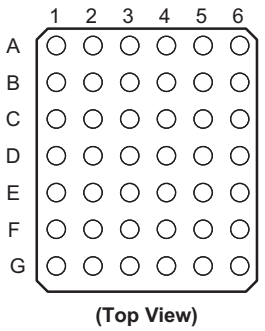
Connection Diagrams

Terminal Assignments for MLP



(Top View)

Pin Assignments for BGA



(Top View)

Figure 2. Terminal and Pin Assignments

Terminal Descriptions for MLP

Pin Name	I/O Type	Number of Terminals	Description of Signals
DP[1:12]	I/O	12	LVCMOS parallel I/O, Direction controlled by DIRI pin
CKREF	IN	1	LVCMOS clock input and PLL reference
STROBE	IN	1	LVCMOS strobe signal for latching data into the serializer
CKP	OUT	1	LVCMOS word clock output. This signal is the regenerated STROBE signal
DSO+ / DSI- DSO- / DSI+	DIFF-I/O	2	CTL differential serial I/O data signals(1) DSO: Refers to output signal pair DSI: Refers to input signal pair DSO(I)+: Positive signal of DSO(I) pair DSO(I)-: Negative signal of DSO(I) pair
CKSI+ / CKSI-	DIFF-IN	2	CTL differential deserializer input bit clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI-: Negative signal of CKSI pair
CKSO+ / CKSO-	DIFF-OUT	2	CTL differential deserializer output bit clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO-: Negative signal of CKSO pair
S1	IN	1	Used to define frequency range for the RefClock, CKREF.
S2	IN	1	
PLLx_SEL	IN	1	Used to define PLL multiplication mode. PLLX_SEL = 0 multiplication factor 7-1/3x PLLX_SEL = 1 multiplication factor 7x
DIRI	IN	1	LVCMOS control input. Used to control direction of data flow: DIRI = “1” Serializer DIRI = “0” Deserializer
$\overline{\text{DIRO}}$	OUT	1	LVCMOS output, inversion of DIRI
V_{DDP}	Supply	1	Power supply for parallel I/O and translation circuitry
V_{DDS}	Supply	1	Power supply for core and serial I/O
V_{DDA}	Supply	1	Power supply for analog PLL circuitry
GND	Supply	0	Use bottom ground plane for ground signals

Notes:

1. The DSO/DSI serial port pins have been arranged such that if one device is rotated 180° with respect to the other device, the serial connections properly aligns without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.

Pin Assignments for BGA Pin Assignments

	1	2	3	4	5	6
A	DP4	DP2	N/C	N/C	N/C	CKREF
B	DP6	DP5	DP1	N/C	STROBE	$\overline{\text{DIRO}}$
C	CKP	N/C	DP3	N/C	CKSO+	CKSO-
D	N/C	DP7	V_{DDP}	GND	DSO-/DSI+	DSO+/DSI-
E	DP8	DP9	GND	V_{DDS}	CKSI+	CKSI-
F	DP10	DP11	N/C	V_{DDA}	N/C	DIRI
G	DP12	N/C	N/C	PLLx_SEL	S2	S1

N/C = No Connect

Control Logic Circuitry

The FIN12AC has the ability to be used as a 12-bit serializer or a 12-bit deserializer. Terminals S1 and S2 must be set to accommodate the clock reference input frequency range of the serializer. Table 1 shows the terminal programming of these options based on the S1 and S2 control terminals. The DIRI terminal controls whether the device is the serializer or a deserializer. When DIRI is asserted LOW, the device is configured as a deserializer. When the DIRI terminal is asserted HIGH, the device is configured as a serializer. Changing the state on the DIRI signal reverses the direction of the I/O signals and generates the opposite state signal on $\overline{\text{DIRO}}$. For unidirectional operation, the DIRI terminal should be hardwired to the HIGH or LOW state and the $\overline{\text{DIRO}}$ terminal should be left floating. For bi-directional operation, the DIRI of the master device is driven by the system and the $\overline{\text{DIRO}}$ signal of the master is used to drive the DIRI of the slave device.

PLL Multiplier

The multiply select pin PLLx_SEL determines whether the PLL multiplication factor is 7 times the CKREF frequency or 7-1/3 times the CKREF frequency. Overclocking the PLL increases the range of spread spectrum on the CKREF input clock that can be tolerated.

Both of the PLL multiplier modes can work with a non-spread spectrum clock. When operating with the standard 7x multiplier and operating in a CKREF = STROBE mode, the serialized word is 14 data bits long. Each deserializer output period has the same period of the STROBE signal.

When operating in the overclocking mode, the average deserializer period is the same as the STROBE signal. The individual periods vary between 14 and 16 data bits long. The pattern repeats every three cycles with two 14-bit cycles, followed by a third 16-bit cycle. The last two bits in the 16-bit cycle are zero. The deserializer output clock period has the same variation as the serializer outputs.

Turn-Around Functionality

The device passes and inverts the DIRI signal through the device asynchronously to the $\overline{\text{DIRO}}$ signal. Care must be taken by the system designer to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be put into a HIGH-impedance state prior to the DIRI signal being asserted.

When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned into a deserializer and the values are overwritten.

Power-Down Mode

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state, the PLL and references are disabled, differential input buffers are shut off, differential output buffers are placed into a HIGH-impedance state, LVCMOS outputs are placed into a HIGH-impedance state, LVCMOS inputs are driven to a valid level internally, and all internal circuitry are reset. The loss of CKREF state is also enabled to ensure that the PLL only powers up if there is a valid CKREF signal.

In a typical application mode, signals of the device do not change other than between the desired frequency range and the power-down mode. This allows for system-level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a “logic 0” should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a “logic 1” should be connected to a system-level power-down signal.

Table 1. Control Logic Circuitry

Mode Number	PLLx_SEL	S2	S1	DIRI	Description
0	X	0	0	X	Power-Down Mode
1	1	0	1	1	12-Bit Serializer, Standard Clocking, 20MHz to 40MHz CKREF
	0	0	1	1	12-Bit Serializer, Over-Clocked PLL, 19MHz to 38.2MHz CKREF
	X	0	1	0	12-Bit Deserializer
2	1	1	0	1	12-Bit Serializer, Standard Clocking, 5MHz to 14MHz CKREF
	0	1	0	1	12-Bit Serializer, Over-Clocked PLL, 4.7MHz to 13.3MHz CKREF
	X	1	0	0	12-Bit Deserializer
3	1	1	1	1	12-Bit Serializer, Standard Clocking, 8MHz to 28MHz CKREF
	0	1	1	1	12-Bit Serializer, Over-Clocked PLL, 9.5MHz to 26.7MHz CKREF
	X	1	1	0	12-Bit Deserializer

Serializer Operation Mode

The serializer configurations are described in the following sections. The basic serialization circuitry works similarly in these modes, but the actual data and clock streams differ, dependent on whether CKREF is the same as the STROBE signal. When it is stated that CKREF = STROBE, the CKREF and STROBE signals have an identical frequency of operation, but may or may not be phase aligned. When it is stated that CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: (Figure 3)
Modes 1, 2, 3
DIRI = 1,
CKREF = STROBE

The PLL must receive a stable CKREF signal to achieve lock prior to any valid data being sent. During the PLL phase, STROBE should not be connected to the CKREF signal.

Once the PLL is stable and locked, the device can begin to capture and serialize data. Data is captured on the rising edge of the STROBE signal and serialized. The serialized data stream is synchronized and sent source synchronously with a bit clock with an embedded word boundary. When operating in this mode, the internal deserializer circuitry is disabled, including the DS input buffer. The CKSI serial inputs remain active to allow the pass through of the CKSI signal to the CKP output. For more on this mode, please see the section on Passing a Word Clock. If this mode is not needed, the CKSI inputs can either be driven to valid levels or left to float. For lowest power operation, let the CKSI inputs float.

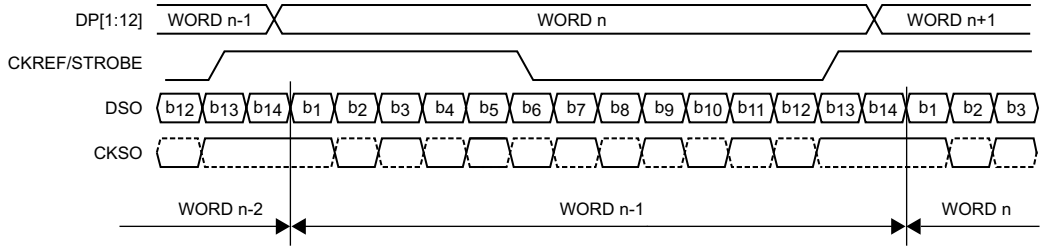


Figure 3. Serializer Timing Diagram (CKREF = STROBE)

Serializer Operation: (Figure 4)
DIRI = 1,
CKREF does not = STROBE

If the same signal is not used for CKREF and STROBE, the CKREF signal must be run at a higher frequency than the STROBE rate to serialize the data correctly. The actual serial transfer rate remains at 14 times the CKREF frequency. A data value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same.

The exact frequency that the reference clock needs is dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the minimum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly if the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

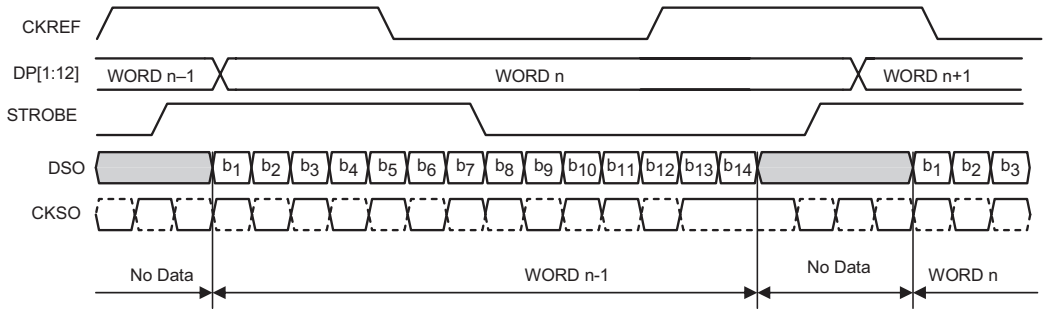


Figure 4. Serializer Timing Diagram (CKREF does not = STROBE)

Serializer Operation Mode (Continued)

Serializer Operation: (Figure 5)
DIRI = 1,
No CKREF

A third method of serialization uses a free-running bit clock on the CKSI signal. This mode is enabled by grounding the CKREF signal and driving the DIRI signal HIGH.

At power-up, the device is configured to accept a serialization clock from CKSI. If a CKREF is received, this device enables the CKREF serialization mode. The device remains in this mode even if CKREF is stopped. To re-enable this mode, the device must be powered down and powered back up with “logic 0” on CKREF.

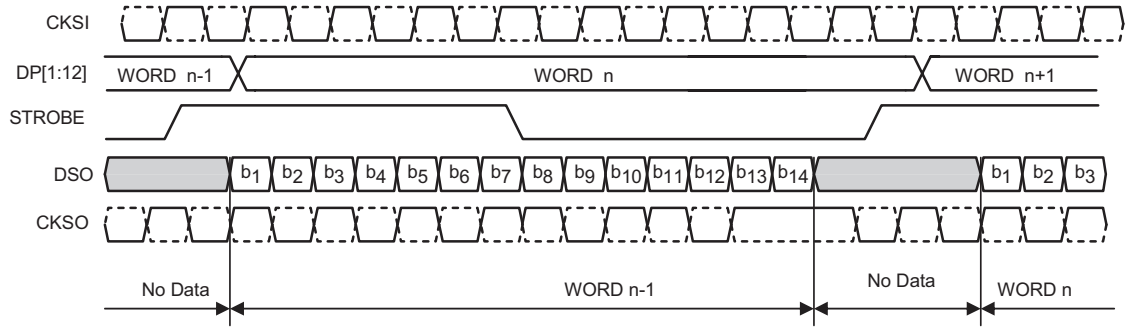


Figure 5. Serializer Timing Diagram Using Provided Bit Clock (No CKREF)

Deserializer Operation Mode

The operation of the deserializer is only dependent upon the data received on the DSI data signal pair and the CKSI clock signal pair. The following two sections describe the operation of the deserializer under two distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device used in generating the serial data and clock signals that are inputs to the deserializer.

When operating in this mode, the internal serializer circuitry is disabled, including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks. When S1 and S2 are asserted low, all CMOS outputs are driven low at the output of the deserializer.

Deserializer Operation: (Figure 6)
DIRI = 0
(Serializer Source: CKREF = STROBE)

When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserializer through use of the bit clock sent with the data. The word boundary is defined in the actual clock and data signal. Parallel data is generated at the time the word boundary is detected. The falling edge of CKP occurs coincident with the data transition. The rising edge of CKP is generated approximately seven bit times later. When no embedded word boundary occurs, no pulse on CKP is generated and CKP remains HIGH.

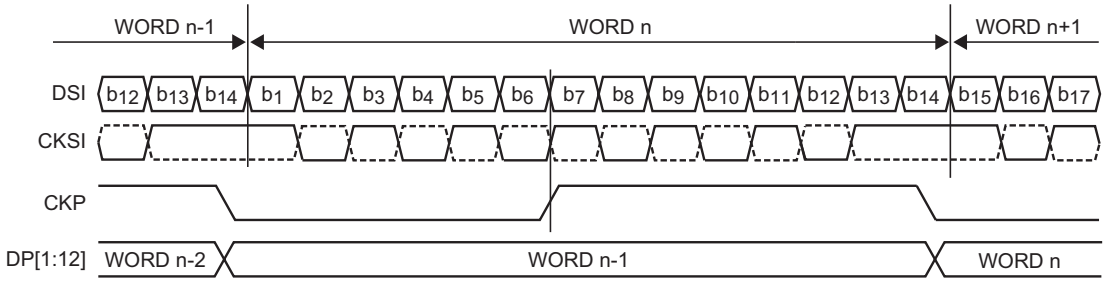


Figure 6. Deserializer Timing Diagram (Serializer Source: CKREF equals STROBE)

Deserializer Operation: (Figure 7)
PwrDwn = 1
DIRI = 0
(Serializer Source: CKREF does not = STROBE)

The logical operation of the deserializer remains the same if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer differs because it has non-valid data bits sent between words. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal is equal to the STROBE frequency. The falling edge of CKP is coincident with data transition. The LOW time of the CKP signal is equal to 1/2 (seven bit times) of the CKREF period. The CKP HIGH time is equal to STROBE period – half of the CKREF period. Figure 7 is representative of a waveform that could be seen when CKREF is not equal to STROBE. If CKREF is significantly faster, additional non-valid data bits occur between data words.

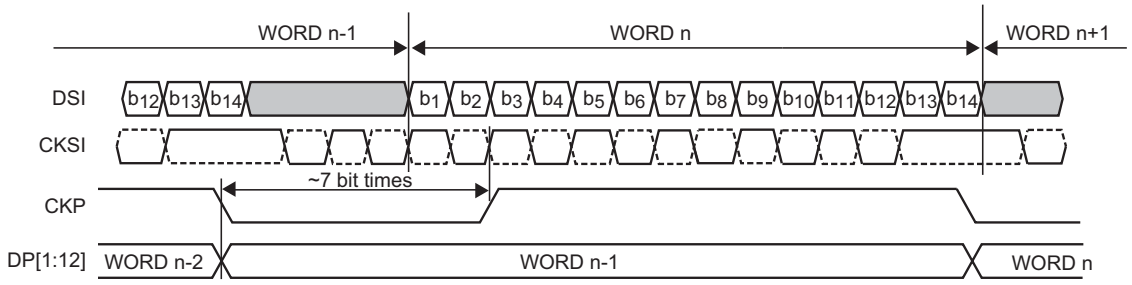


Figure 7. Deserializer Timing Diagram (Serializer Source: CKREF does not = STROBE)

Embedded Word Clock Operation

The FIN12AC sends and receives serial data source synchronously with a bit clock. The bit clock has been modified to create a word boundary at the end of each data word. The word boundary has been implemented by skipping a low clock pulse. This appears in the serial clock stream as three consecutive bit times where signal CKSO remains HIGH. To implement this scheme, two extra data bits are required. During the word boundary phase, the data toggles either HIGH-then-LOW or LOW-then-HIGH, dependent upon the last bit of the actual data word. Table 2 provides some examples showing the actual data word and the data word with the word boundary bits added. Note that a 12-bit word is extended to 14 bits during serial transmission. Bit 13 and Bit 14 are defined with respect to Bit 12. Bit 13 is always the inversion of Bit 12 and Bit 14 is the same as Bit 12. This ensures that a "0" → "1" and a "1" → "0" transition always occurs during the embedded-word phase, where CKSO is HIGH.

The serializer generates the word boundary data bits and the boundary clock condition and embeds them into the serial data stream. The deserializer looks for the end of the word boundary condition to capture and transfer the data to the parallel port. The deserializer only uses the embedded word boundary information to find and capture the data. These boundary bits are stripped prior to the word being sent out the parallel port.

LVCMOS Data I/O

The LVCMOS input buffers have a nominal threshold value equal to half V_{DDP}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer, the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source / sink current of 2mA at 1.8V. The outputs are active when the DIRI signal is asserted LOW. When the DIRI signal is asserted HIGH, the bi-directional LVCMOS I/Os are in HIGH-Z state. Under purely capacitive load conditions, the output swings between GND and V_{DDP}.

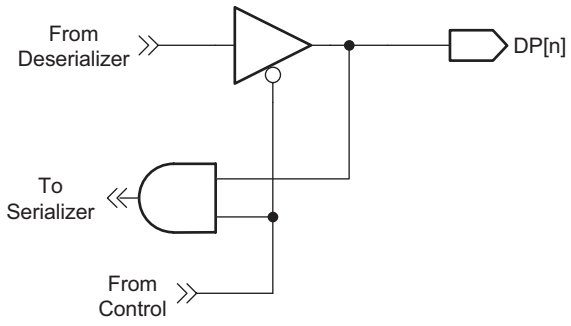


Figure 8. LVCMOS I/O

Differential I/O Circuitry

The FIN12AC employs FSC proprietary CTL I/O technology. CTL is a low-power, low-EMI differential swing I/O technology. The CTL output driver generates a constant output source and sink current. The CTL input receiver senses the current difference and direction from the corresponding output buffer to which it is connected. This differs from LVDS, which uses a constant current source output, but a voltage sense receiver. Like LVDS, an input source termination resistor is required to properly terminate the transmission line. The FIN12AC device incorporates an internal termination resistor on the CKSI receiver and a gated internal termination resistor on the DS input receiver. The gated termination resistor ensures proper termination regardless of direction of data flow. The relatively greater sensitivity of the current sense receiver of CTL allows it to work at much lower current drive and a much lower voltage.

During power-down mode, the differential inputs are disabled and powered down and the differential outputs are placed in a HIGH-Z state. CTL inputs have an inherent fail-safe capability that supports floating inputs. When the CKSI input pair of the serializer is unused, it can be left floating reliably. Alternately both of the inputs can be connected to ground. CTL inputs should never be connected to V_{DD}. When the CKSO output of the deserializer is unused, it should be allowed to float.

Table 2. Word Boundary Data Bits

12-bit Data Words		12-bit Data Word with Word Boundary	
Hex	**Binary**	**Hex**	**Binary**
FFFh	1111 1111 1111b	2FFFh	10 1111 1111 1111b
555h	0101 01010 0101b	1555h	01 0101 0101 0101b
xxxh	0xxx xxxx xxxxb	1xxxh	01 0xxx xxxx xxxxb
xxxh	1xxx xxxx xxxxb	2xxxh	10 1xxx xxxx xxxxb

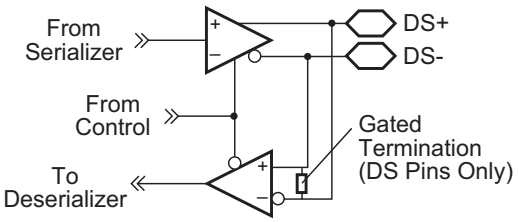


Figure 9. Bi-Directional Differential I/O Circuitry

Phase-Locked Loop (PLL) Circuitry

The CKREF input signal is used to provide a reference to the PLL. The PLL generates internal timing signals capable of transferring data at 14 times the incoming CKREF signal. The output of the PLL is a bit clock used to serialize the data. The bit clock is also sent source synchronously with the serial data stream.

There are two ways to disable the PLL. The PLL can be disabled by entering the Mode 0 state (S1 = S2 = 0). The PLL disables immediately upon detecting a LOW on both the S1 and S2 signals. When any of the other modes are entered by asserting S1 or S2 HIGH and by providing a CKREF signal, the PLL powers up and goes through a lock sequence. Wait a specified number of clock cycles prior to capturing valid data into the parallel port and applying CKREF to STROBE. When the µSerDes chipset transitions from a power-down state (S1, S2 = 0.0) to a powered state (example S1, S2 = 1, 1), CKP on the deserializer transitions LOW for a short duration and returns HIGH. Following this, the signal level of the deserializer at CKP corresponds to the serializer signal levels.

An alternate way of powering down the PLL is by stopping the CKREF signal either HIGH or LOW. Internal circuitry detects the lack of transitions and shuts the PLL and serial I/O down. Internal references are not disabled, allowing for the PLL to power-up and re-lock in fewer clock cycles than when exiting Mode 0. When a transition is seen on the CKREF signal, the PLL is reactivated.

Application Mode Diagrams Modes 1, 2, 3: Unidirectional Data Transfer

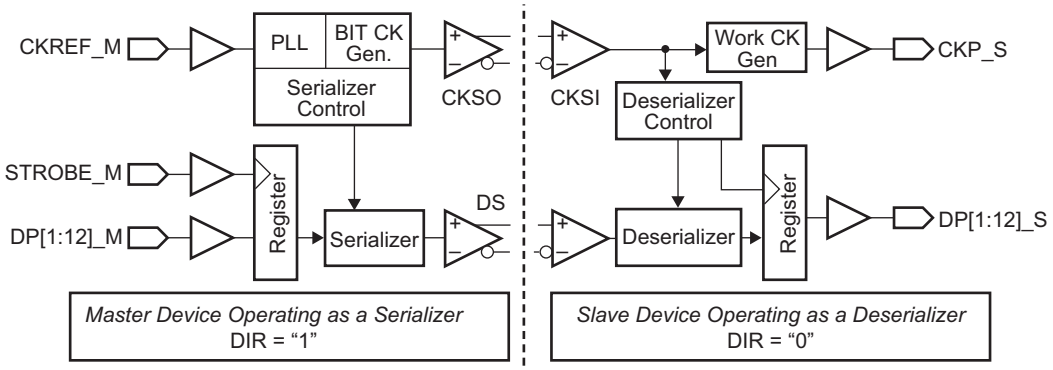


Figure 10. Simplified Block Diagram for Unidirectional Serializer and Deserializer

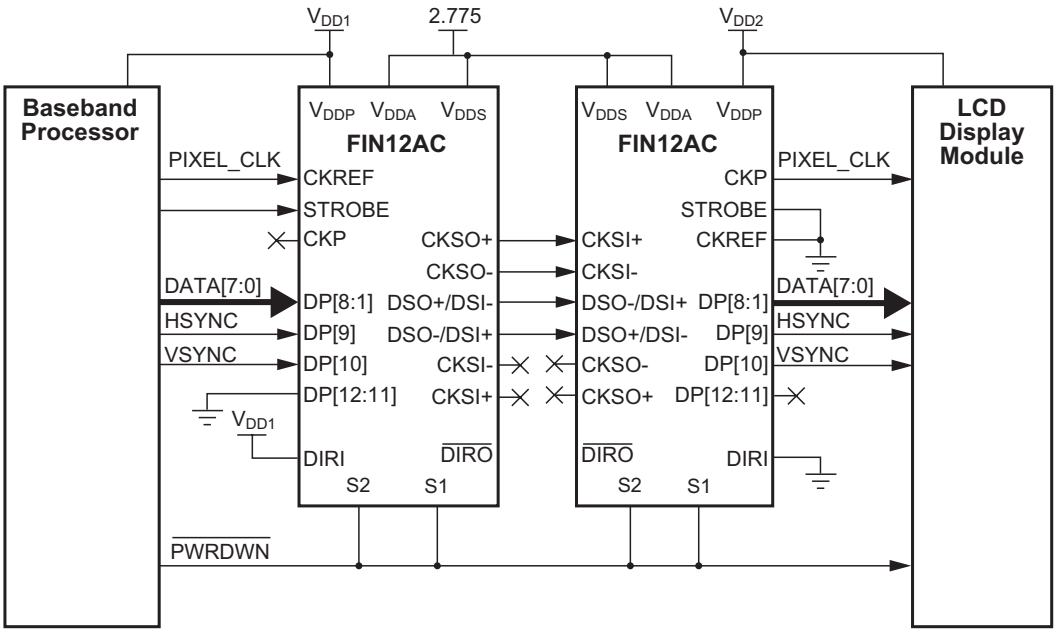
Figure 10 shows basic operation when a pair of µSerDes is configured in an unidirectional operation mode.

Master Operation:

1. During power-up, the device is configured as a serializer based on the value of the DIRI signal.
2. The device accepts CKREF_M word clock and generates a bit clock with embedded word boundary. This bit clock is sent to the slave device through the CKSO port.
3. The device receives parallel data on the rising edge of STROBE_M.
4. The device generates and transmits serialized data on the DS signals, which is source synchronous with CKSO.
5. The device generates an embedded word clock for each strobe signal.

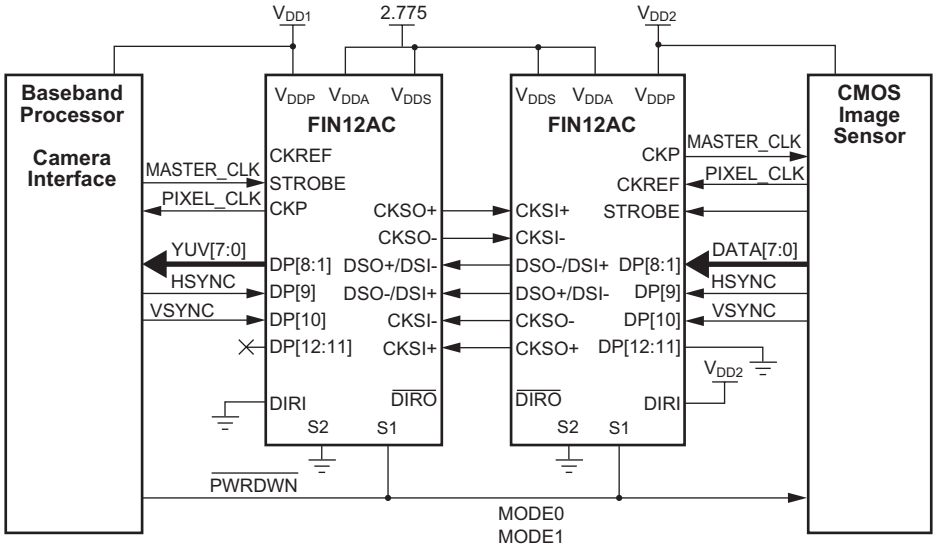
Slave Operation:

1. The device is configured as a deserializer at power-up based on the value of the DIRI signal.
2. The device accepts an embedded word boundary bit clock on CKSI.
3. The device deserializes the DS data stream using the CKSI input clock.
4. The device writes parallel data onto the DP_S port and generates the CKP_S only when a valid data word occurs.



Note:
V_{DD1} does not have to equal V_{DD2}.

Figure 11. Unidirectional 8-bit RGB Interface (10MHz to 40MHz Operation)



Note:
V_{DD1} does not have to equal V_{DD2}.

Figure 12. Unidirectional 8-bit YUV Sensor with Master Clock on Base (10MHz to 40MHz Operation)

STROBE Pass-Through Mode

For some applications, it is desirable to pass a word clock across a differential signal pair in the opposite direction of serialization. The FIN12AC supports this mode of operation. Figure 5 in the application section illustrates how to configure the devices for this mode. The following describes how to enable this functionality.

For the deserializer:

1. DIRI = LOW
2. CKREF = LOW
3. Word clock should be connected to the STROBE.

This passes the STROBE signal out the CKSO port.

For the serializer:

1. Connect CKSO of the deserializer to CKSI of the serializer.
2. CKSI passes the signal to CKP.

When PLL-bypass mode is used, the bit clock toggles on the CKP signal.

Table 3. Control I/O

Mode Number	DIRI	$\overline{\text{DIRO}}$	CKSO	CKP	Mode of Operation
0	x	Z	Z	Z	Power Down Mode: S2 = 0, S1 = 0
1, 2, 3	0	1	CKSO = STROBE	Deserializer Output STROBE	Deserializer: Any active mode
1, 2, 3	1	0	Serializer Output Bit Clock	CKSI	Serializer: Any active mode

Flex Circuit Design Guidelines

The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB:

- Keep all four differential wires the same length.
- Allow no noisy signals over or near differential serial wires. Example: No LVCMOS traces over differential wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+4.6	V
	All Input/Output Voltage	-0.5	+4.6	V
	LVDS Output Short-Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 4 seconds)		+260	°C
ESD	Rating Human Body Model, 1.5kΩ, 100pF			
	All Pins		>3	kV
	S1, S2, CKSO, CKSI, DSO, DSI, VDDA, VDDS, VDDP (as specified in IEC61000-4-2)		>15	kV

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	3.3	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature	-30	+70	°C
V_{DDA-PP}	Supply Noise Voltage		100	mVp-p

DC Electrical Characteristics

Over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.(2)	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = –2.0mA	V_{DDP} = 3.3 ±0.30	0.75 x V_{DDP}			V
			V_{DDP} = 2.5 ±0.20				
			V_{DDP} = 1.8 ±0.15				
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	V_{DDP} = 3.3 ±0.30			0.25 x V_{DDP}	V
			V_{DDP} = 2.5 ±0.20				
			V_{DDP} = 1.8 ±0.15				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		–5.0		5.0	µA
Differential I/O							
I_{ODH}	Output HIGH Source Current	V_{OS} = 1.0V, Figure 13			–1.75		mA
I_{ODL}	Output LOW Sink Current	V_{OS} = 1.0V, Figure 13			0.950		mA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS} S2 = S1 = 0V			±1.0	±5.0	µA
I_{IZ}	Disabled Input Leakage Current	CKSI, DSI = 0V to V_{DDS} S2 = S1 = 0V			±1.0	±5.0	µA
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ±5%			V_{GO} + 0.80		V
V_{GO}	Input Voltage Ground Off-set Relative to Driver(3)	see Figure 14			0		V
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0 $\lvert CKSI^+ - CKSI^- \rvert = V_{ID}$		80.0	100	120	Ω
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0 $\lvert DSI^+ - DSI^- \rvert = V_{ID}$		80.0	100	120	Ω

Notes:

2. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into the device
and negative values refer to current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified
(except ΔV_{OD} and V_{OD}).
3. V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

Symbol	Parameter	Test Conditions			Min.	Typ.(4)	Max.	Unit
I_{DDA1}	V_{DDA} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 1				437		µA
I_{DDA2}	V_{DDA} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 0				528		µA
I_{DDS1}	V_{DDS} Serializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 1				4.4		mA
I_{DDS2}	V_{DDS} Deserializer Static Supply Current	All DP and Control Inputs at 0V or V_{DD} NOCKREF, S2 = 0, S1 = 1, DIR = 0				5.5		mA
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD\_PD} = I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S2 = 0 All Inputs at GND or V_{DD}				1.0		µA
I_{DD_SER1}	14:1 Dynamic Serializer Power Supply Current(4) $I_{DD\_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = H See Figure 16	S2 = H S1 = L	5MHz		8.5		mA
				14MHz		15.0		
			S2 = H S1 = H	10MHz		9.5		
				28MHz		17.0		
			S2 = L S1 = H	20MHz		11.0		
				40MHz		17.0		
I_{DD_DES1}	14:1 Dynamic Deserializer Power Supply Current(4) $I_{DD\_DES1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = L See Figure 16	S2 = H S1 = L	5MHz		6.5		mA
				14MHz		7.5		
			S2 = H S1 = H	10MHz		7.0		
				28MHz		10.0		
			S2 = L S1 = H	20MHz		8.5		
				40MHz		11.5		

Notes:

4. The worst-case test pattern produces a maximum toggling of internal digital circuits, CTL I/O and LVCMOS I/O with the PLL operating at the reference frequency unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

AC Electrical Characteristics

Characteristics at recommended over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.[5]	Max.	Unit
Serializer Input Operating Conditions							
t_{TCP}	CKREF Clock Period (5MHz – 40MHz)	CKREF = STROBE See Figure 19	S2=1 S1=0 S2=1 S1=1 S2=0 S1=1	71.0 35.0 25.0	T	200 100 50.0	ns
f_{REF}	CKREF Frequency Relative to STROBE Frequency	CKREF does not = STROBE	S2=1 S1=0 S2=1 S1=0 S2=0 S1=1	1.1 x f_{STROBE}		40 14 28	MHz
t_{CPWH}	CKREF Clock High Time			0.2	0.5		T
t_{CPWL}	CKREF Clock Low Time			0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time	See Figure 19				90.0	ns
t_{SPWH}	STROBE Pulse Width HIGH/LOW	See Figure 19		(T x 4)/14		(T x 12)/14	ns
f_{MAX}	Maximum Serial Data Rate	CKREF x 14	S2=0 S1=1 S2=1 S1=0 S2=1 S1=1	280 70 140		540 196 392	Mb/s
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI = 1 See Figure 8 (f = 5MHz)		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE			2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	DIRI = 1, a=(1/f)/14 CKREF = STROBE, See Figure 22		23a+1.5		21a+6.5	ns
t_{SPOS}	CKSO Position Relative to DS	See Figure 25[6]		-200		200	ps
PLL AC Electrical Characteristics							
t_{TPLLS0}	Serializer Phase-Lock Loop Stabilization Time	See Figure 21				200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock	See Figure 26				30.0	µs
t_{TPLLD1}	PLL Power-Down Time	See Figure 27[7]				20.0	ns
Deserializer AC Electrical Characteristics							
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period	See Figure 20		17.8	T	200	ns
t_{RCOL}	CKP OUT Low Time	See Figure 20 (Rising Edge Strobe) Serializer source STROBE = CKREF where a = (1/f)/14[9]		7a–3		7a+3	ns
t_{RCOH}	CKP OUT High Time			7a–3		7a+3	ns
t_{PDV}	Data Valid to CKP LOW	See Figure 20 (Rising Edge Strobe) where a = (1/f)/14[9]		7a–3		7a+3	ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 5pF See Figure 17			3.5	7.0	ns
t_{ROHL}	Output Fall Time (80% to 20%)				3.5	7.0	ns

Notes:

5. Typical values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
6. Skew is measured from either the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.
7. The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW and the state of the
   S1/S2 mode pins. The specific number of clock cycles required for the PLL to be disabled varies dependent upon the operating mode of the device.
8. Signals are transmitted from the serializer source synchronously. Note that, in some cases, data is transmitted when the clock remains at a HIGH state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew would be a combination of output skew from the serializer, load variations, and ISI and jitter effects.
9. Rising edge of CKP appears approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP occurs approximately 8 bit times after a data transition or 6 bit times after the falling edge of CKSO. Variation of the data with respect to the CKP signal is due to internal propagation delay differences of the data and CKP path and propagation delay differences on the various data pins. Note that if the CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle.The low time of CKP remains 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			17.0	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			25.0	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			25.0	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 29			25.0	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 29(10)			2.0	µs
t_{PLZ}, t_{PHZ}	Serializer Disable Time S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW Figure 28			25.0	ns
t_{PZL}, t_{PZH}	Serializer Enable Time S0 or S1 to CKSO, DS	DIRI = 1, S1(2) and S2(1) = LOW-to-HIGH Figure 28			65.0	ns

Notes:

10. Serializer enable time includes the amount of time required for internal voltage and current references to stabilize. This time is significantly less than the PLL lock time and does not limit overall system startup time.

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = 0, S2=0, V_{DD} = 2.5V		2.0		pF
C_{IO}	Capacitance of Parallel Port Pins DP[1:12]	DIRI = 1, S1 = 0, S2=0, V_{DD} = 2.5V		2.0		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 1, S2=0, S1 = 0, V_{DD} = 2.5V		2.0		pF

AC Loading and Waveforms

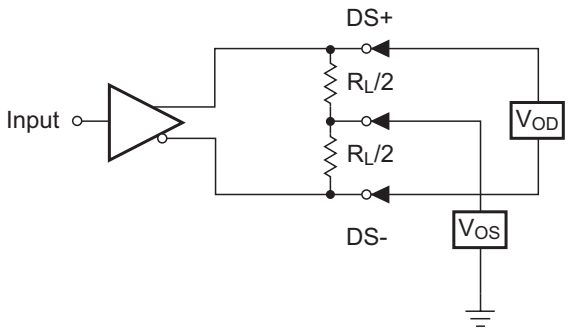


Figure 13. Differential CTL Output DC Test Circuit

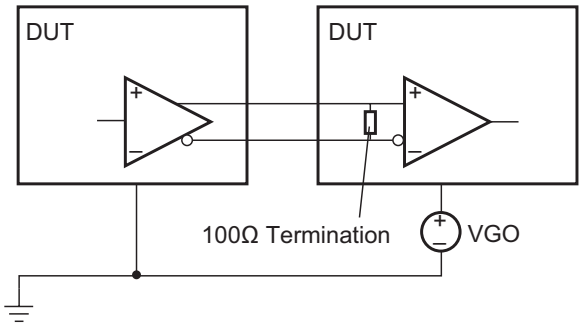
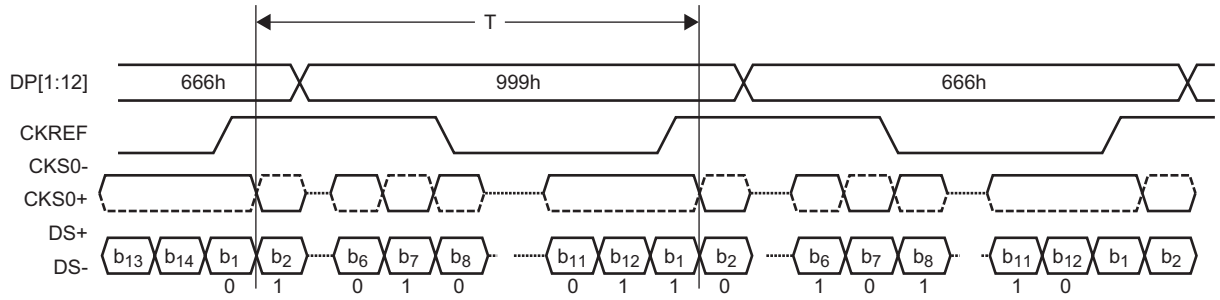


Figure 14. CTL Input Common Mode Test Circuit



Note:
The Worst Case test pattern produces a maximum toggling of internal digital circuits, CTL I/O and LVCMOS I/O with the PLL operating at the reference frequency unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

Figure 15. "Worst Case" Serializer Test Pattern

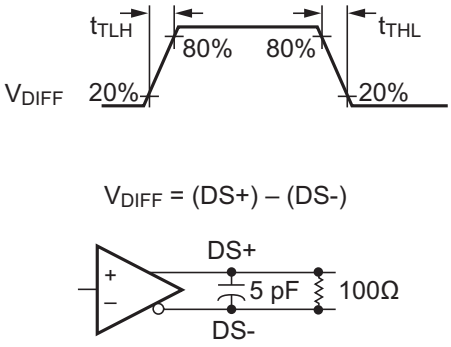


Figure 16. CTL Output Load and Transition Times

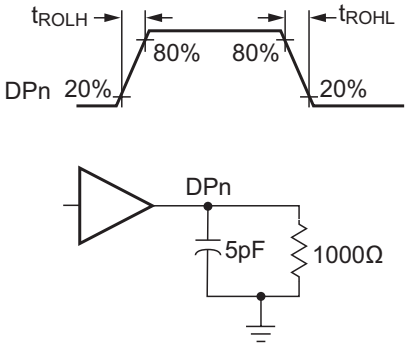
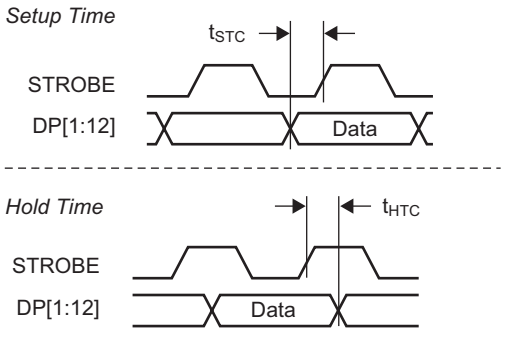


Figure 17. LVCMOS Output Load and Transition Times

AC Loading and Waveforms (Continued)



Setup: MODE0 = “0” or “1”, MODE1 = “1”, SER/$\overline{DES}$ = “1”

Figure 18. Serial Setup and Hold Time

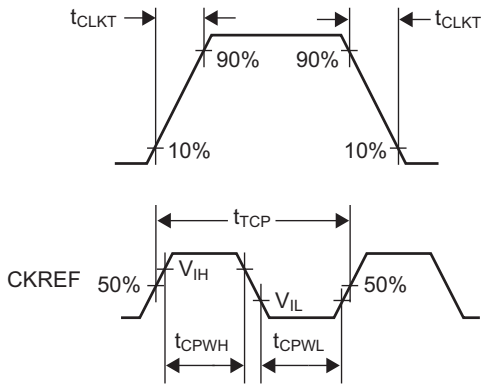
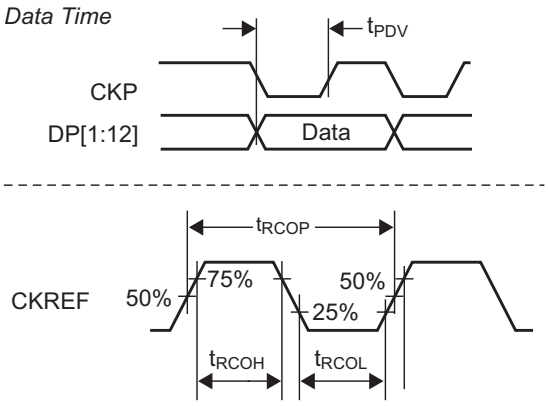
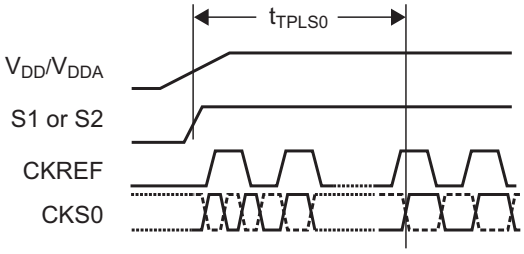


Figure 19. LVCMOS Clock Parameters



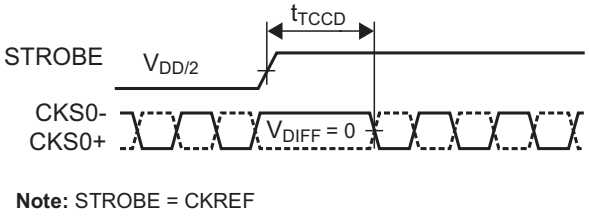
Setup: $\overline{DIRI}$ = “0”, CKSI and DS are valid signals.

Figure 20. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF Signal is free running.

Figure 21. Serializer PLL Lock Time



Note: STROBE = CKREF

Figure 22. Serializer Clock Propagation Delay

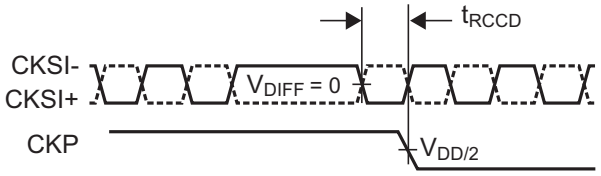


Figure 23. Deserializer Clock Propagation Delay

AC Loading and Waveforms (Continued)

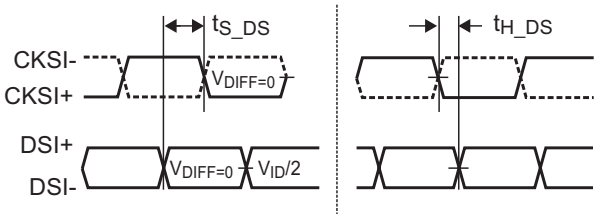


Figure 24. Differential Input Setup and Hold Times

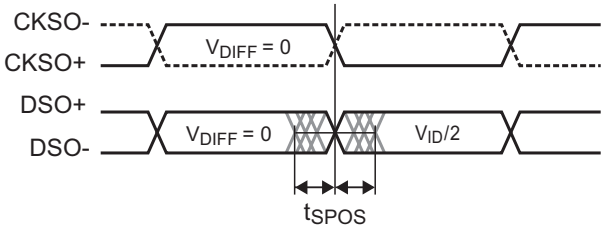
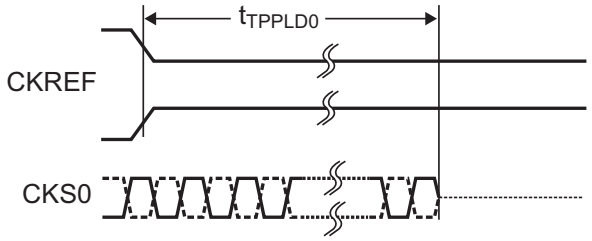


Figure 25. Differential Output Signal Skew



Note: CKREF Signal can be stopped either High or LOW.

Figure 26. PLL Loss of Clock Disable Time

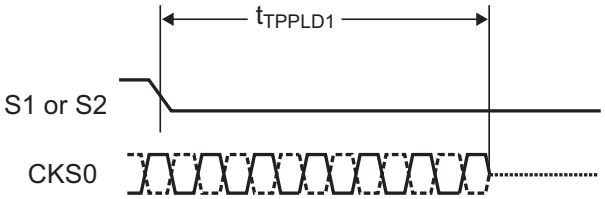
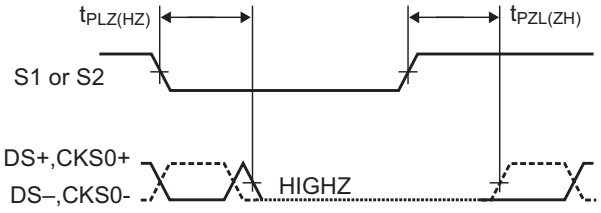
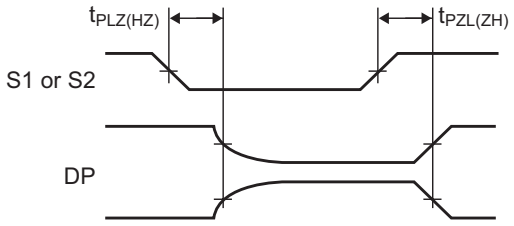


Figure 27. PLL Power-Down Time



Note: CKREF must be active and PLL must be stable.

Figure 28. Serializer Enable and Disable Time



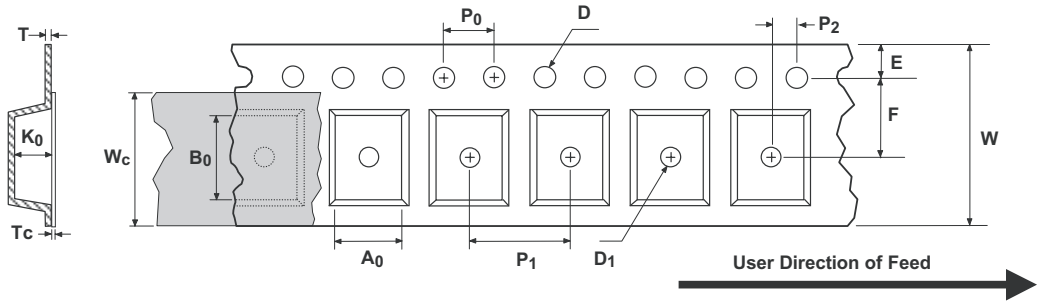
Note: If S1(2) transitioning, then S2(1) must = 0 for test to be valid.

Figure 29. Deserializer Enable and Disable Times

Tape and Reel Specification

BGA Embossed Tape Dimension

Dimensions are in millimeters.

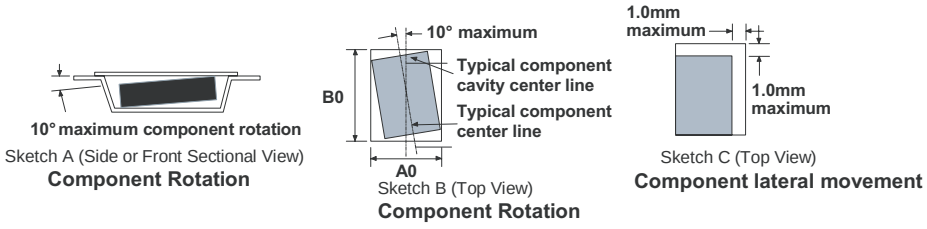


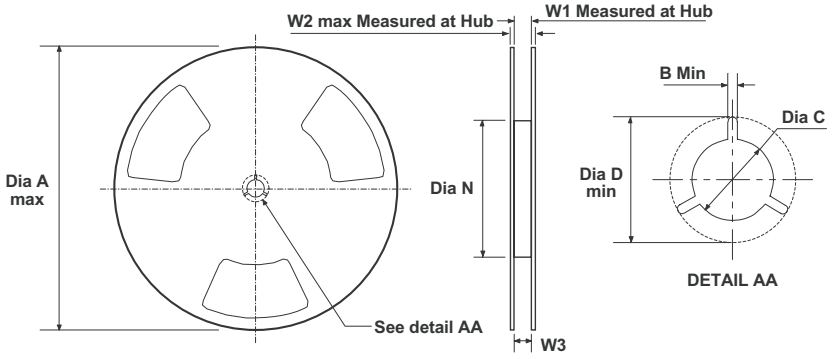
Package	A_0 ±0.1	B_0 ±0.1	D ±0.05	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0/05	T Typ.	T_C ±0.005	W ±0.3	W_C Typ.
3.5 x 4.5	TBD	TBD	1.55	1.5	1.75	5.5	1.1	8.0	4.0	2.0	0.3	0.07	12.0	9.3

Notes:
A0, B0, and K0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Shipping Reel Dimension

Dimensions are in millimeters.



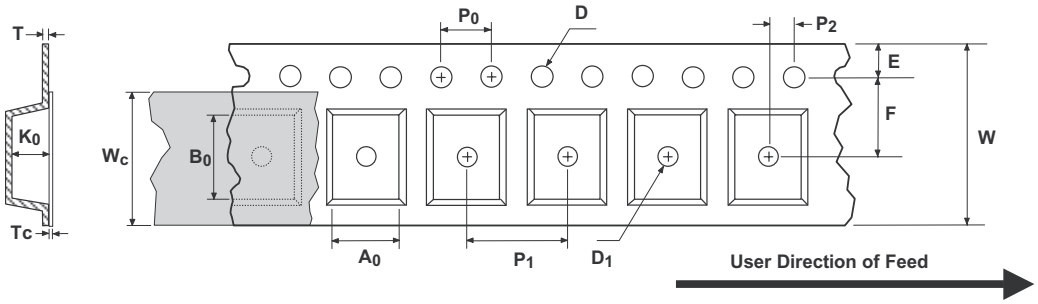


Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/–0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/–0	Dim W2 Max.	Dim W3 (LSL–USL)
8	330	1.5	13.0	20.2	178	8.4	14.4	7.9 ~ 10.4
12	330	1.5	13.0	20.2	178	12.4	18.4	11.9 ~ 15.4
16	330	1.5	13.0	20.2	178	16.4	22.4	15.9 ~ 19.4

Tape and Reel Specification (Continued)

MLP Embossed Tape Dimension

Dimensions are in millimeters.

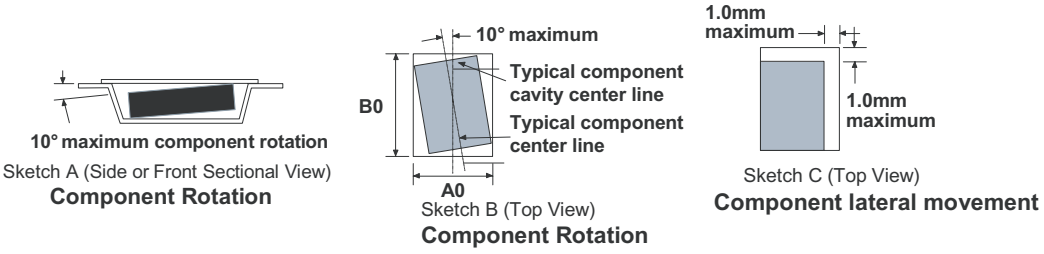


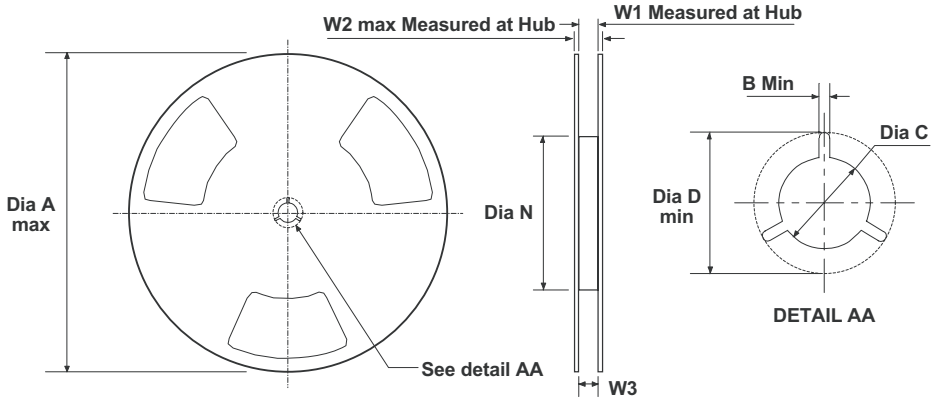
Package	A_0 ±0.1	B_0 ±0.1	D ±0.05	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0/05	T Typ.	T_C ±0.005	W ±0.3	W_C Typ.
5 x 5	5.35	5.35	1.55	1.5	1.75	5.5	1.4	8	4	2.0	0.3	0.07	12	9.3
6 x 6	6.30	6.30	1.55	1.5	1.75	5.5	1.4	8	4	2.0	0.3	0.07	12	9.3

Notes:
Ao, Bo, and Ko dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Shipping Reel Dimensions

Dimensions are in millimeters.

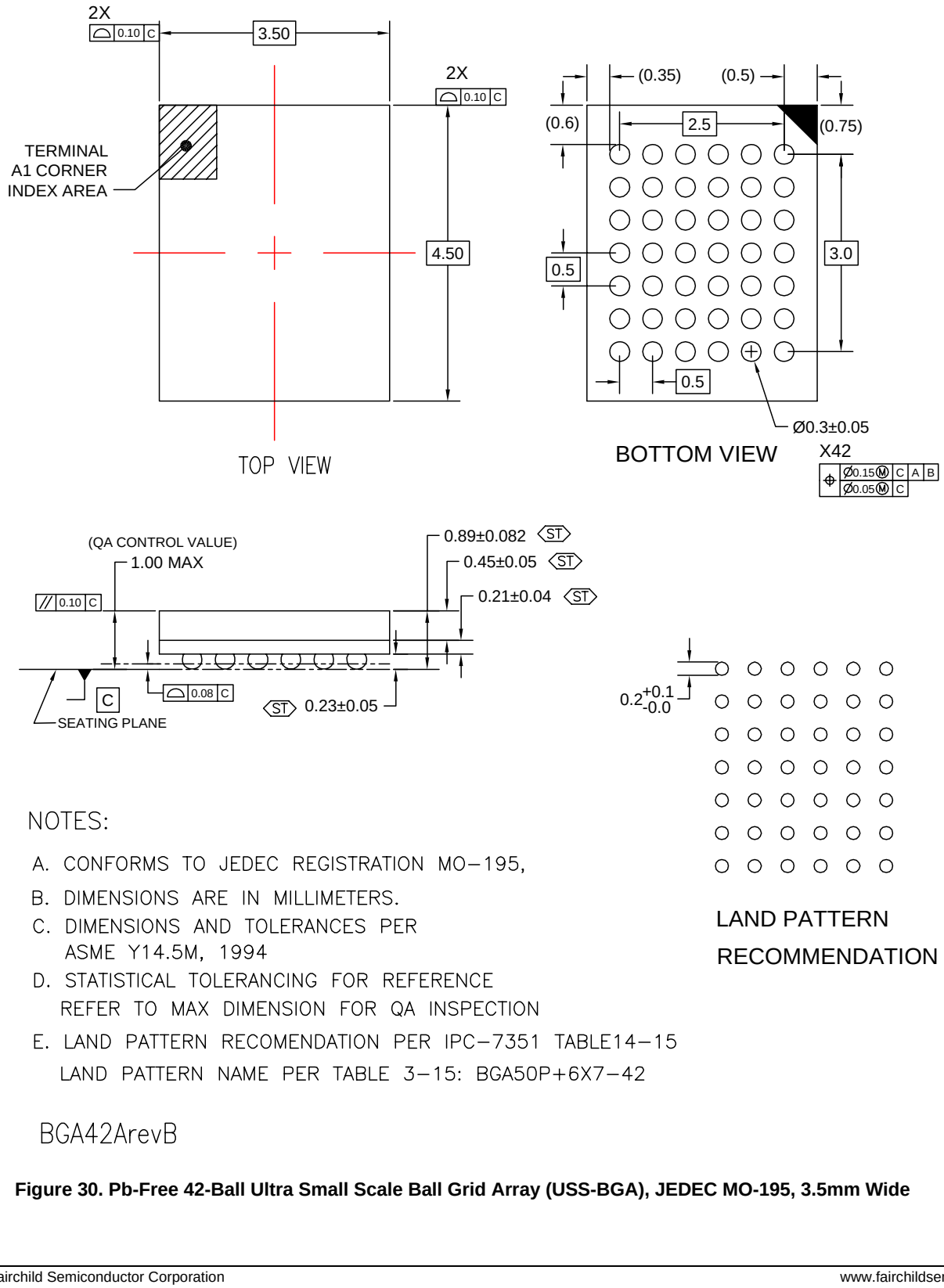




Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/–0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/–0	Dim W2 Max.	Dim W3 (LSL–USL)
8	330	1.5	13	20.2	178	8.4	14.4	7.9 ~ 10.4
12	330	1.5	13	20.2	178	12.4	18.4	11.9 ~ 15.4
16	330	1.5	13	20.2	178	16.4	22.4	15.9 ~ 19.4

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION

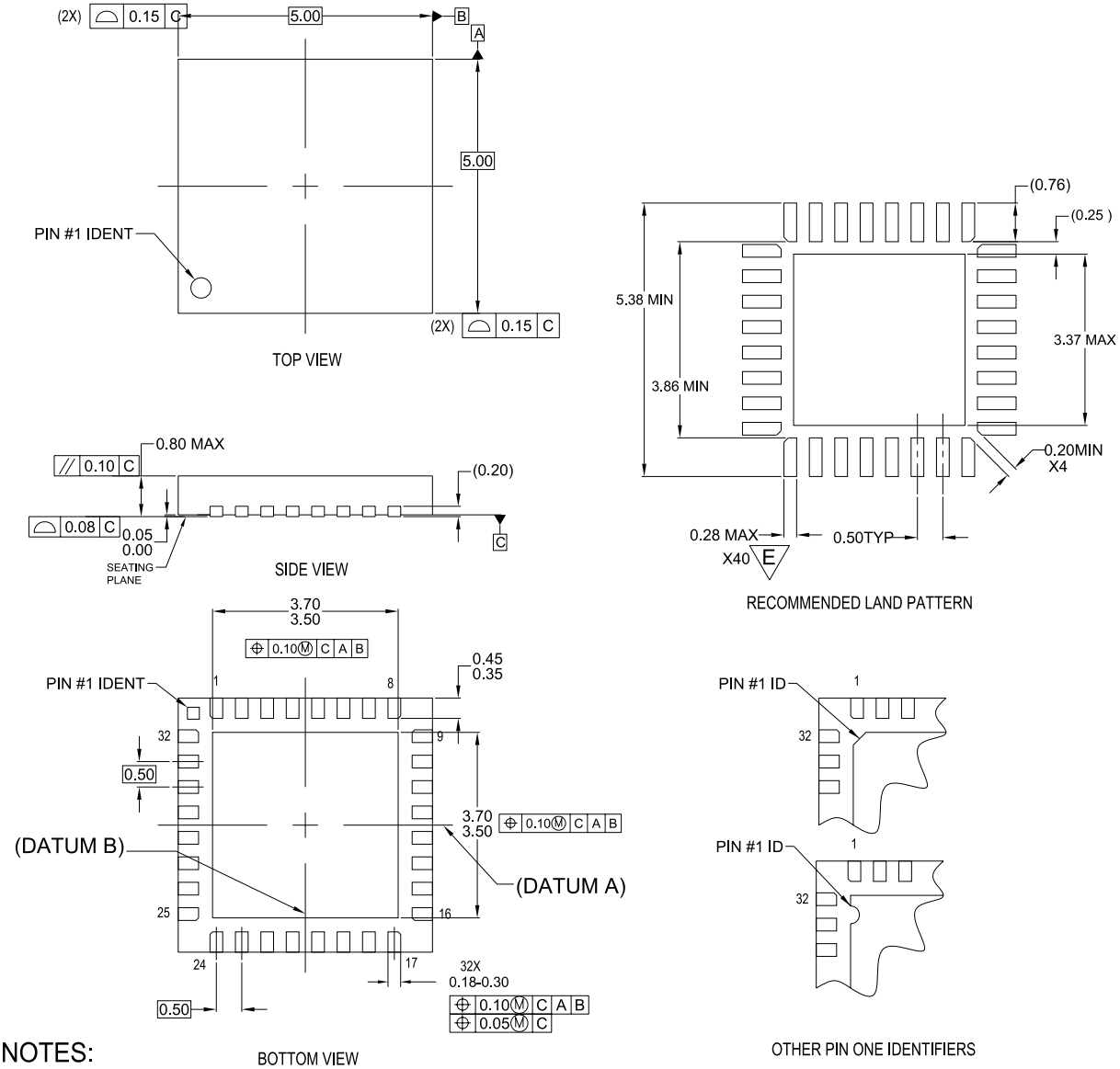
E. LAND PATTERN RECOMENDATION PER IPC−7351 TABLE14−15 LAND PATTERN NAME PER TABLE 3−15: BGA50P+6X7−42

BGA42ArevB

Figure 30. Pb-Free 42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4
THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS,
MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP032ArevB

Figure 31. Pb-Free 32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square

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CoolFET™	I^2C™	PACMAN™	SuperFET™	
CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
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EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
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	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
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Programmable Active Droop™				

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