FS8160 1.1 GHz/1.1 GHz Dual Phase-locked Loop IC

Description

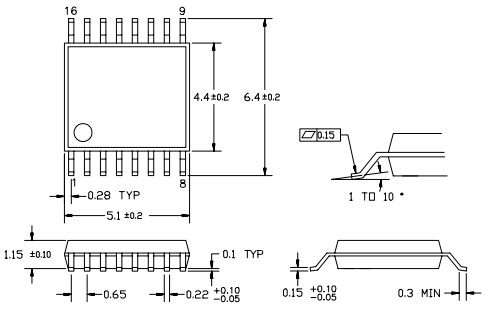
The FS8160 is a serial data input, fully programmable dual phase-locked loop IC for use in the local oscillator subsystem of radio transceivers. When combined with external VCOs, the FS8160 becomes the core of a very low power dual frequency synthesizer well-suited for mobile communication applications. **The FS8160 is pin-compatible with National Semiconductor's LMX1602 IC.**

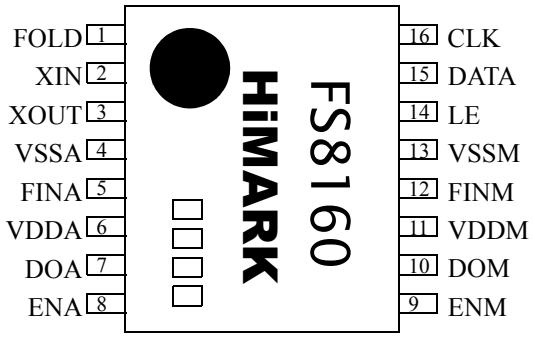
Features

- Supply voltage operating range: 2.7 to 3.6 V
- Maximum input frequency: 1.1 GHz/1.1 GHz (main/auxiliary)
- Low current consumption ($I_{DD,total}$ typically 5 mA at $V_{DD,main} = V_{DD,aux} = 3.0$ V and < 1 μA in power down mode)
- 16-bit programmable input (both main and auxiliary) frequency dividers (including a ÷ 16/17 prescaler) with divide ratio range from 240 to 65535
- 12-bit programmable reference (both main and auxiliary) frequency dividers with divide ratio range from 2 to 4095
- Programmable charge pump output
- Digital-filtered lock detect output
- 16 pin, plastic TSSOP (0.65 mm pitch)

Package and Pin Assignment

16 pin, plastic TSSOP (dimensions in mm)

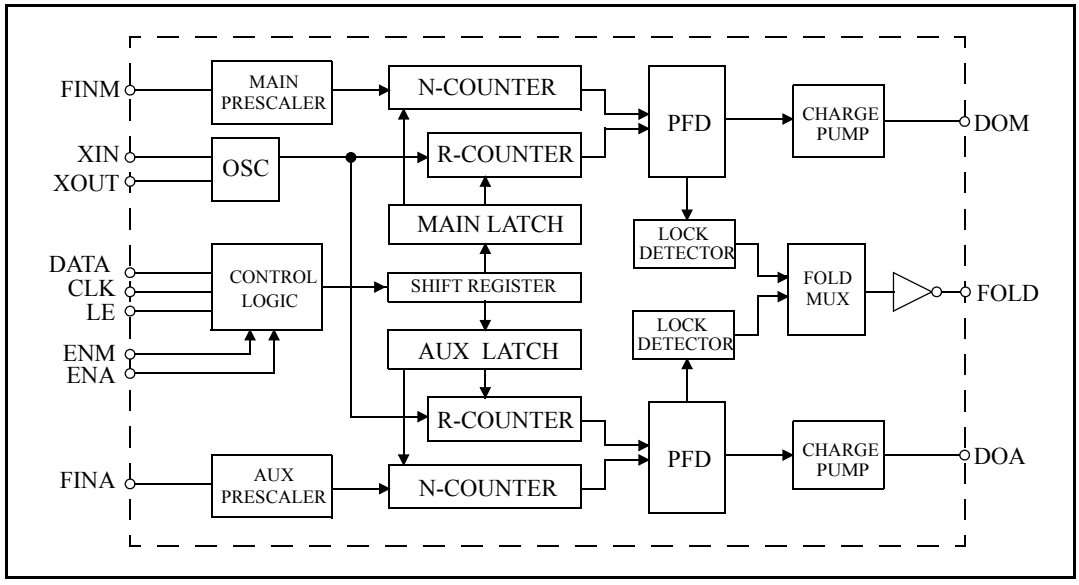




Pin Descriptions

Number	Name	I/O	Description
1	FOLD	O	Multiplexed CMOS level output (see Programming Description section)
2	XIN	I	Reference crystal oscillator or external clock input with internally biased amplifier
3	XOUT	O	Reference crystal oscillator output used with external resonator
4	VSSA	—	Ground (aux PLL)
5	FINA	I	VCO frequency input with internally biased input amplifier (aux PLL)
6	VDDA	—	Nominal 3.0 V supply voltage (aux PLL)
7	DOA	O	Single-ended charge pump output (aux PLL)
8	ENA	I	Enable control input; normal operation when high, power-down mode when low (aux PLL)
9	ENM	I	Enable control input; normal operation when high, power-down mode when low (main PLL)
10	DOM	O	Single-ended charge pump output (main PLL)
11	VDDM	—	Nominal 3.0 V supply voltage (main PLL)
12	FINM	I	VCO frequency input with internally biased input amplifier (main PLL)
13	VSSM	—	Ground (main PLL)
14	LE	I	Latch enable input
15	DATA	I	Serial data input
16	CLK	I	Shift register clock input

Functional Block Diagram



Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{DD,main}$	V_{SS} – 0.3 to V_{SS} + 6.5	V
	$V_{DD,aux}$	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage range	$V_{FIN,main}$	V_{SS} – 0.3 to $V_{DD,main}$ + 0.3	V
	$V_{FIN,aux}$	V_{SS} – 0.3 to $V_{DD,aux}$ + 0.3	V
Operating temperature range	T_{OPR}	–40 to 85	°C
Storage temperature range	T_{STG}	–40 to 125	°C
Soldering temperature range	T_{SLD}	255	°C
Soldering time range	t_{SLD}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	$V_{DD,main}$	2.7		3.6	V
	$V_{DD,aux}$	$V_{DD,main}$		$V_{DD,main}$	V
Operating temperature	T_A	–40	25	85	°C

Electrical Characteristics

($V_{DD,main}$ = $V_{DD,aux}$ = V_{DD} = 3.0 V, T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
GENERAL						
Current consumption	$I_{DD,total}$	1.1 GHz + 1.1 GHz		5.0		mA
		1.1 GHz only		2.5		mA
Standby current consumption	$I_{DD,standby}$	ENM = ENA = low		1		µA
FIN operating frequency range	f_{FIN}	Main	100		1100	MHz
		Auxiliary	100		1100	MHz
XIN operating frequency range	f_{XIN}	Logic mode	1		40	MHz
		Crystal mode	1		20	MHz
FIN input sensitivity	P_{FIN}	Main	–15		0	dBm
		Auxiliary	–15		0	dBm
XIN input sensitivity	V_{XIN}		0.5		$V_{DD,aux}$	V_{pk-pk}
DIGITAL INTERFACE						
Logic LOW input voltage	V_{IL}				0.2 × V_{DD}	V
Logic HIGH input voltage	V_{IH}		0.8 × V_{DD}			V
Logic LOW input current	I_{IL}	V_{IL} = 0 V, V_{DD} = 3.6 V	–1		1	µA
Logic HIGH input current	I_{IH}	V_{IH} = V_{DD} = 3.6 V	–1		1	µA
XIN logic LOW input current	$I_{IL,XIN}$	V_{IL} = 0 V, V_{DD} = 3.6 V	–100			µA
XIN logic HIGH input current	$I_{IH,XIN}$	V_{IH} = V_{DD} = 3.6 V			100	µA
XOUT output current magnitude	I_{XOUT}	Logic mode, V_{XOUT} = V_{DD}/2, V_{DD} = 3.6 V			|200|	µA
		Crystal mode, V_{XOUT} = V_{DD}/2, V_{DD} = 2.7 V	|300|			µA
Logic LOW output voltage	V_{OL}	I_{OL} = 500 µA			0.4	V
Logic HIGH output voltage	V_{OH}	I_{OH} = –500 µA	V_{DD} – 0.4			V
SERIAL PROGRAMMING TIMING						
DATA to CLK setup time	t_{SU1}		50			nS
DATA to CLK hold time	t_{H1}		10			nS

Electrical Characteristics (continued)

($V_{DD,main}$ = $V_{DD,aux}$ = V_{DD} = 3.0 V, T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
CLK to LE setup time	t_{SU2}		50			nS
CLK pulse width logic HIGH	t_{PWH}		50			nS
CLK pulse width logic LOW	t_{PWL}		50			nS
LE pulse width	t_{PW}		50			nS
CHARGE PUMP						
Charge pump output current	$I_{DO,source}$	High gain mode, V_{DOM},V_{DOA} = V_{DD}/2		–1600		µA
		Low gain mode, V_{DOM},V_{DOA} = V_{DD}/2		–160		µA
	$I_{DO,sink}$	High gain mode, V_{DOM},V_{DOA} = V_{DD}/2		+1600		µA
		Low gain mode, V_{DOM},V_{DOA} = V_{DD}/2		+160		µA
Charge pump high-Z state current	$I_{DO,high-Z}$	0.5 V ≤ V_{DOM}, V_{DOA} ≤ V_{DD} – 0.5 V		1		nA

Functional Description

The FS8160 dual phase-locked loop (PLL) IC contains two identical PLLs (main and auxiliary). Both the main and auxiliary PLLs share the crystal oscillator, serial data input logic, and multi-function lock detector output circuits. Each PLL has its own programmable input and reference frequency dividers, phase/frequency detectors, programmable charge pumps, and digital-filtered lock detectors.

Programmable Input Frequency Divider

The VCO input to the FIN pin is divided by the programmable divider and then internally output to the phase/frequency detector (PFD) as f_V. The programmable input frequency divider consists of a ÷ 16/17 (P/P+1) dual-modulus prescaler and a 16-bit (N) counter, which is further comprised of a 4-bit swallow (A) counter, and a 12-bit main (B) counter. The total divide ratio, M, is related to values for P, A, and B through the relation

$$M = (P+1) \times A + P \times (B-A) = P \times B + A,$$

with $B \geq A$. The minimum programmable divisor for continuous counting is given by $P \times (P-1) = 16 \times 15 = 240$, and the valid total divide ratio range for the input divider is $M = 240$ to 65535.

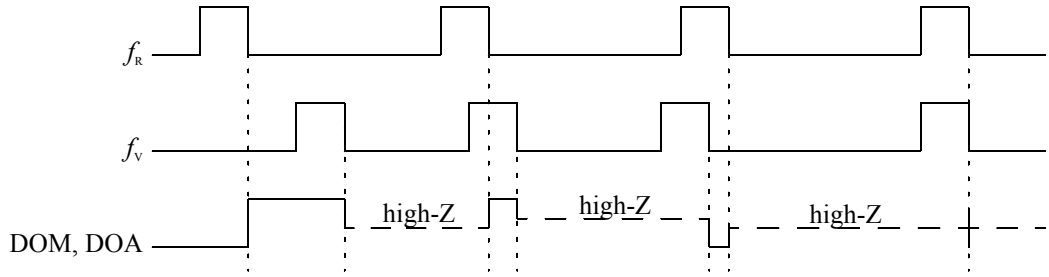
Programmable Reference Frequency Divider

The crystal oscillator output is divided by the programmable divider and then internally output to the PFD as f_R. The programmable reference frequency divider consists of a 13-bit reference (R) counter. Because of its design, the valid total divide ratio range for the reference divider is $R = 2$ to 4095.

Phase/Frequency Detector (PFD)

The PFD compares an internal input frequency divider output signal, f_V, with an internal reference frequency divider output signal, f_R, and generates an error signal which is proportional to the phase error between f_V and f_R. The polarity of the PFD is user-selectable using serial input data control bits (see Table 5 on page 9). The input/output waveforms for a positive polarity PFD (VCO frequency increases with increasing tuning voltage) are shown in Fig. 1.

Fig. 1 – Positive polarity PFD input/output waveforms



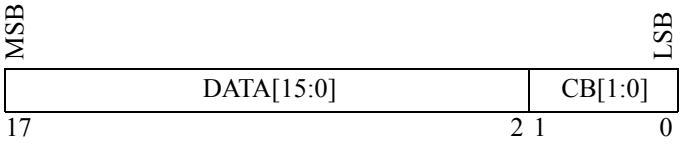
Charge Pump

The charge pump output sources/sinks current to/from an external loop filter, which converts the charge into a voltage used to control the external VCO's frequency. When the PLL is locked, the charge pump output is primarily in a high impedance (high-Z) state. The magnitude of the charge pump output current is user-selectable using serial input data control bits (see Table 5 on page 9).

Serial Input Data Format

The divide ratios for the input (*N*) and reference (*R*) dividers are input using an 18-bit serial interface consisting of separate clock (CLK), data (DATA), and latch enable (LE) lines. The format of the serial data is shown in Fig. 2.

Fig. 2 – Serial input data format



The data on the DATA line is written to the shift register on the rising edge of the CLK signal and is input with MSB first. The data on the DATA line should be changed on the falling edge of CLK, and LE should be held low while data is being written to the shift register. Data is transferred from the shift register to one of the four (4) frequency divider latches when LE is set high depending upon the state of the control bits (CB[1:0]) as indi-

cated below.

Table 1: Latch enable control bits

CB[1]	CB[0]	Latch Location
0	0	Aux. R
0	1	Aux. N
1	0	Main R
1	1	Main N

The definition of the contents of the shift register relating to each particular latch location is listed in the table below.

Table 2: Serial data input format

	First bit	Shift Register Bit Location															Last bit
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Aux. R	FOLD[3:0]				AUXR[11:0])												0	0
Aux. N	AUXB[11:0]												AUXA[3:0]				0	1
Main R	CP_CNTRL[3:0]				MAINR[11:0]												1	0
Main N	MAINB[11:0]												MAINA[3:0]				1	1

The 12-bit main and auxiliary reference (*R*) divider ratios are specified by the MAINR[11:0] and AUXR[11:0] bits, respectively, and are defined in the table below.

Table 3: Reference divider ratios

Divide Ratio	MAINR[11:0] and AUXR[11:0]											
	11	10	9	8	7	6	5	4	3	2	1	0
2	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Similarly, the 16-bit main and auxiliary input (*N*) divider ratios are specified by the MAINA[3:0] + MAINB[11:0] and AUXA[3:0] + AUXB[11:0] bits, respectively, and are defined in the table below.

Table 4: Input divider ratios

Divide Ratio	MAINB[11:0] and AUXB[11:0]												Divide Ratio	MAINA[3:0] and AUXA[3:0]			
	11	10	9	8	7	6	5	4	3	2	1	0		3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1	15	1	1	1	1

The charge pump control bits CP_CNTRL[3:0] set (1) the phase detector polarity and (2) the magnitude of the charge pump source/sink current, and are defined below.

Table 5: Charge pump and PFD control bits

Bit	Latch Location	Function	"0"	"1"
CP_CNTRL[3]	Main R, bit 17	Aux. charge pump current	Low, 160 µA	High, 1600 µA
CP_CNTRL[2]	Main R, bit 16	Main charge pump current	Low, 160 µA	High, 1600 µA
CP_CNTRL[1]	Main R, bit 15	Aux. phase/frequency detector polarity[a]	Negative	Positive
CP_CNTRL[0]	Main R, bit 14	Main phase/frequency detector polarity	Negative	Positive

a. When the VCO frequency *increases* with increasing control voltage, set the phase/frequency detector polarity to *positive*. When the VCO frequency *decreases* with increasing control voltage, set the phase/frequency detector polarity to *negative*.

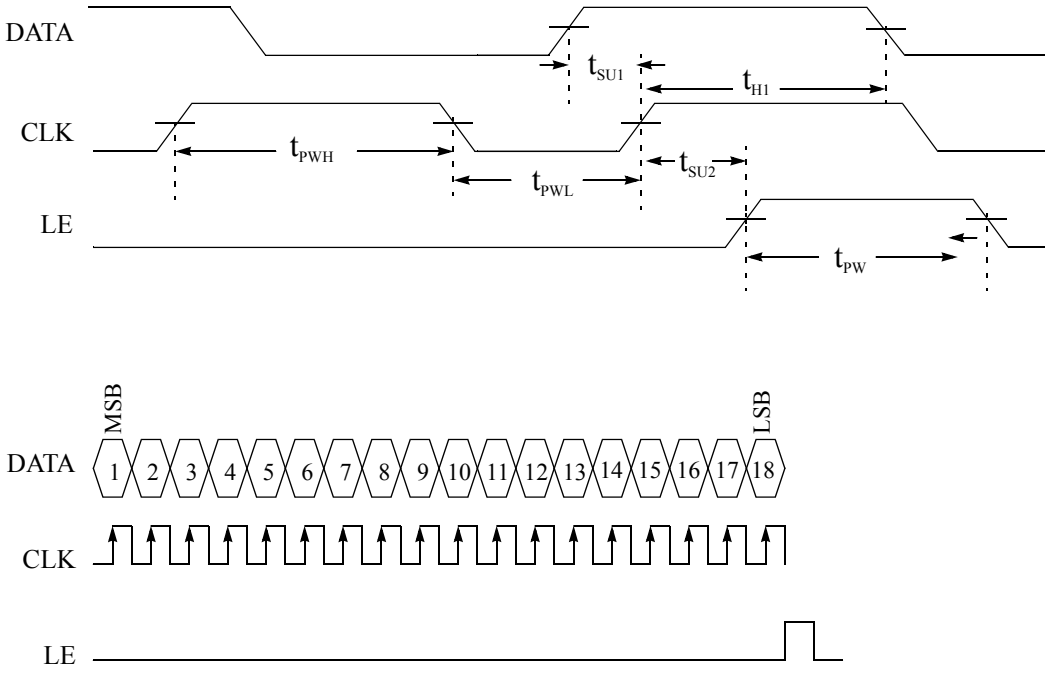
The outputs selected by the FOLD[3:0] control bits for the multiplexed FOLD output pin are defined in the table below.

Table 6: Multiplexed FOLD output control bits

FOLD[3]	FOLD[2]	FOLD[1]	FOLD[0]	FOLD Output State
Aux. R, bit 17	Aux. R, bit 16	Aux. R, bit 15	Aux. R, bit 14	
0	0	0	0	"0"
0	0	0	1	"1"
0	0	1	×	Main lock detector output
0	1	0	×	Aux. lock detector output
0	1	1	×	Main AND Aux. lock detector output
1	0	0	×	Main *R*-divider output
1	0	1	×	Aux. *R*-divider output
1	1	0	×	Main *N*-divider output
1	1	1	×	Aux. *N*-divider output

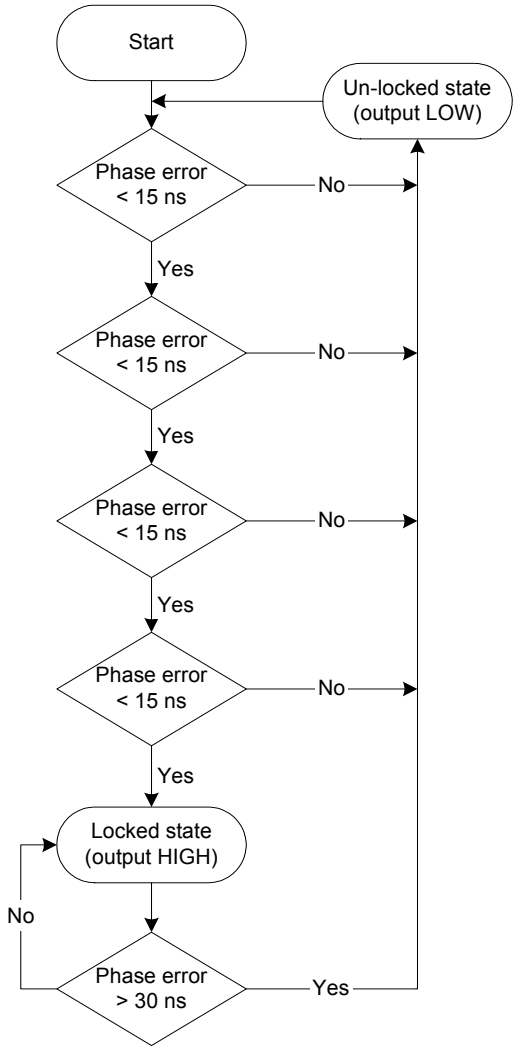
Serial input data timing waveforms are shown in Fig. 3.

Fig. 3 – Serial input data timing waveforms



Lock Detector

The lock detector incorporates a filter which compares the phase error between the inputs to the PFD to an R-C generated delay of 15 ns. To enter the locked state (output is high), the phase error must be less than 15 ns for four (4) consecutive cycles. Once in the locked state, the generated R-C delay is changed to 30 ns. To exit the locked state (i.e. lock detector output goes low), the phase error must become greater than the 30 ns delay. When the PLL is in stand-by mode, the lock detector output is forced low. A flow chart representing the operation of the lock detector is given below.



Crystal Oscillator

The internal crystal oscillator circuitry may be used in either of two modes: crystal mode — with an external crystal resonator (crystal mode) or logic mode — with an external reference frequency source such as a TCXO (logic mode). The FOLD[3:0] control bits select

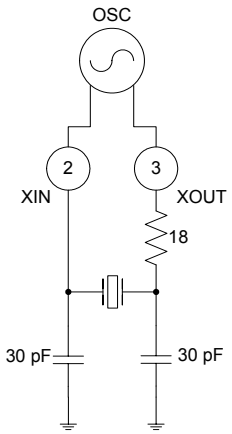
the operation mode of the crystal oscillator according to the table below.

Table 7: Crystal oscillator mode control bits

FOLD[3]	FOLD[2]	FOLD[1]	FOLD[0]	Crystal Oscillator Mode
Aux. R, bit 17	Aux. R, bit 16	Aux. R, bit 15	Aux. R, bit 14	
0	0	0	0	Crystal mode
0	0	0	1	Crystal mode
All other states				Logic mode
				Crystal mode

A typical crystal oscillator circuit implementing a 10 MHz oscillator in crystal mode is given in the figure below.

Fig. 4 – 10 MHz crystal oscillator circuit



Application Circuit