

February 2001 Revised August 2001

FSTU162450

Configurable 4-Bit to 20-Bit Bus Switch with -2V Undershoot Protection and 25 Ω Series Resistors in Outputs (Preliminary)

General Description

The Fairchild Universal Bus Switch FSTU162450 provides 4-bit, 5-bit, 8-bit, 10-bit, 16-bit, 20-bit of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The FSTU162450 is designed to allow "customer" configuration control of the enable connections. The device can be organized as either a five 4-bit, four 5-bit, two 10-bit or one 20-bit enable bus switch. Also achieveable are 8-bit and 16-bit enabled configurations (see Functional Description). The device's bit configuration is controlled through select pin logic. (see Truth Table). When $\overline{\text{OE}}_x$ is LOW, Port A_x is connected to Port B_x . When $\overline{\text{OE}}_x$ is HIGH, the switch is OPEN.

The A and B Ports are protected against undershoot to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHCTM) senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning the switch on.

Features

- Undershoot protected to -2V (A and B Ports)
- \blacksquare 25 Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Notes AN-5008 and AN-5021 for UHC details
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Applications Note

Select pins S_0 , S_1 , S_2 are intended to be used as static user configurable control pins. The AC performance of these pins has not been characterized or tested. Switching of these select pins during system operation may temporarily disrupt output logic states and/or enable pin controls.

Ordering Code:

Order Number	Package Number	Package Description
FSTU162450GX (Note 1)		54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]
FSTU162450MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

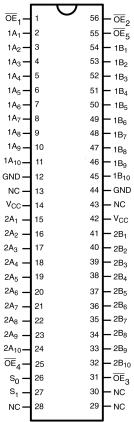
Note 1: BGA package available in Tape and Reel only.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code

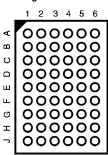
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Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



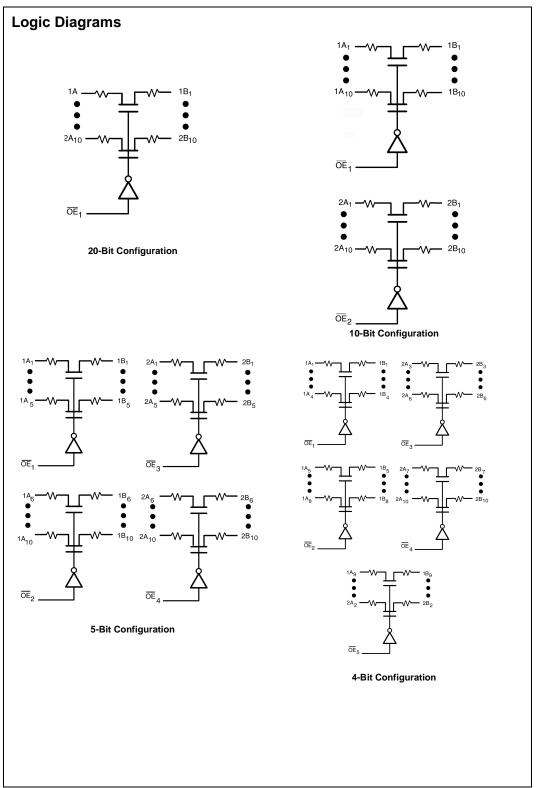
(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
S ₀ , S ₁	Bit Configuration Enables
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
Α	1A ₃	1A ₂	OE ₁	OE ₂	1B ₂	1B ₃
В	1A ₅	1A ₄	1A ₁	1B ₁	1B ₄	1B ₅
С	1A ₇	1A ₆	GND	OE ₅	1B ₆	1B ₇
D	1A ₉	1A ₈	GND	V_{CC}	1B ₈	1B ₉
E	2A ₁	1A ₁₀	S ₀	V _{CC}	1B ₁₀	2B ₁
F	2A ₃	2A ₂	S ₁	GND	2B ₂	2B ₃
G	2A ₅	2A ₄	V _{CC}	GND	2B ₄	2B ₅
Н	2A ₇	2A ₆	2A ₁₀	2B ₁₀	2B ₆	2B ₇
J	2A ₉	2A ₈	OE4	OE ₃	2B ₈	2B ₉



Functional Description

The device can also be configured as an 8 and 16-bit device by grounding the unused pins in the 10-bit and 20-bit configurations respectively. The 8-bit configuration may also be achieved by connecting two of the 4-bit enables from the 4-bit configuration together and connecting the remaining enable pin (\overline{OE}) HIGH.

Truth Tables

(see Functional Description)

20-Bit Configuration ($S_0 = S_1 = L$)

		Inputs			In mosts (Outtouts			
OE ₁	OE ₂	OE ₃	OE ₄	OE ₅	Inputs/Outputs			
L	Х	Х	Х	Х	$1A_{1-10} = 1B_{1-10}, 2A_{1-10} = 2B_{1-10}$			
Н	X	Х	Х	X	Z			

10-Bit Configuration ($S_0 = L, S_1 = H$)

		Inputs		Inputs/Outputs		
OE ₁	OE ₂	OE ₃	OE ₄	OE ₅	$1A_{1-10} = 1B_{1-10}$	$2A_{1-10} = 2B_{1-10}$
L	Х	Х	L	Х	$1A_X = 1B_X$	$2A_X = 2B_X$
L	Х	Х	Н	Х	$1A_X = 1B_X$	Z
Н	Х	Х	L	Х	Z	$2A_X = 2B_X$
Н	Х	Х	Н	Х	Z	Z

5-Bit Configuration ($S_0 = H, S_1 = L$)

	J	- 1-0	, - i ,					
		Inputs				Inputs/0	Outputs	
OE ₁	OE ₂	OE ₃	OE ₄	OE ₅	1A ₁₋₅ , 1B ₁₋₅	1A ₆₋₁₀ , 1B ₆₋₁₀	2A ₁₋₅ , 2B ₁₋₅	2A ₅₋₁₀ , 2B ₅₋₁₀
L	L	L	L	Х	$1A_X = 1B_X$	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$
L	L	L	Н	Х	$1A_X = 1B_X$	$1A_y = 1B_y$	$2A_X = 2B_X$	Z
L	L	Н	L	X	$1A_X = 1B_X$	$1A_y = 1B_y$	Z	$2A_y = 2B_y$
L	L	Н	Н	Х	$1A_X = 1B_X$	$1A_y = 1B_y$	Z	Z
L	Н	L	L	Х	$1A_X = 1B_X$	Z	$2A_X = 2B_X$	$2A_y = 2B_y$
L	Н	L	Н	Х	$1A_X = 1B_X$	Z	$2A_X = 2B_X$	Z
L	Н	Н	L	Х	$1A_X = 1B_X$	Z	Z	$2A_y = 2B_y$
L	Н	Н	Н	Х	$1A_X = 1B_X$	Z	Z	Z
Н	L	L	L	Х	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$
Н	L	L	Н	Х	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	Z
Н	L	Н	L	Х	Z	$1A_y = 1B_y$	Z	$2A_y = 2B_y$
Н	L	Н	Н	Х	Z	$1A_y = 1B_y$	Z	Z
Н	Н	L	L	Х	Z	Z	$2A_X = 2B_X$	$2A_y = 2B_y$
Н	Н	L	Н	Х	Z	Z	$2A_X = 2B_X$	Z
Н	Н	Н	L	Х	Z	Z	Z	$2A_y = 2B_y$
Н	Н	Н	Н	Х	Z	Z	Z	Z

Truth Tables (Continued)

4-Bit Configuration ($S_0 = S_1 = H$)

		Inputs	- 01 - 1	<u>* </u>			Inputs/Outputs	i	
OE ₁	OE ₂	OE ₃	OE ₄	OE ₅	1A ₁₋₄ , 1B ₁₋₄	1A ₅₋₈ , 1B ₅₋₈	2A ₃₋₆ , 2B ₃₋₆	2A ₇₋₁₀ , 2B ₇₋₁₀	1A ₉₋₁₀ , 2B ₉₋₁₀ 2A ₁₋₂ , 2B ₁₋₂
L	L	L	L	L	$1A_x = 1B_x$	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
L	L	L	L	Н	$1A_X = 1B_X$	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$	Z
L	L	L	Н	L	$1A_X = 1B_X$	$1A_y = 1B_y$	$2A_X = 2B_X$	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
L	L	L	Н	Н	$1A_X = 1B_X$	$1A_y = 1B_y$	$2A_X = 2B_X$	Z	Z
L	L	I	L	L	$1A_x = 1B_x$	$1A_y = 1B_y$	Z	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
L	L	Н	L	Н	$1A_X = 1B_X$	$1A_y = 1B_y$	Z	$2A_y = 2B_y$	Z
L	L	Η	Н	L	$1A_x = 1B_x$	$1A_y = 1B_y$	Z	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
L	L	Н	Н	Н	$1A_X = 1B_X$	$1A_y = 1B_y$	Z	Z	Z
L	Н	L	L	L	$1A_x = 1B_x$	Z	$2A_X = 2B_X$	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
L	Н	L	L	Н	$1A_X = 1B_X$	Z	$2A_X = 2B_X$	$2A_y = 2B_y$	Z
L	Н	L	Н	L	$1A_x = 1B_x$	Z	$2A_x = 2B_x$	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
L	Н	L	Н	Н	$1A_X = 1B_X$	Z	$2A_X = 2B_X$	Z	Z
L	Н	Ι	L	L	$1A_X = 1B_X$	Z	Z	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
L	Н	Η	L	Н	$1A_X = 1B_X$	Z	Z	$2A_y = 2B_y$	Z
L	Н	Ħ	Н	L	$1A_X = 1B_X$	Z	Z	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
L	Н	Η	Н	Н	$1A_X = 1B_X$	Z	Z	Z	Z
Н	L	L	L	L	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	L	L	L	Н	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	$2A_y = 2B_y$	Z
Н	L	L	Н	L	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	L	L	Н	Н	Z	$1A_y = 1B_y$	$2A_X = 2B_X$	Z	Z
Н	L	Н	L	L	Z	$1A_y = 1B_y$	Z	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	L	Н	L	Н	Z	$1A_y = 1B_y$	Z	$2A_y = 2B_y$	Z
Н	L	Н	Н	L	Z	$1A_y = 1B_y$	Z	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	L	Н	Н	Н	Z	$1A_y = 1B_y$	Z	Z	Z
Н	Н	L	L	L	Z	Z	$2A_X = 2B_X$	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	Н	L	L	Н	Z	Z	$2A_X = 2B_X$	$2A_y = 2B_y$	Z
Н	Н	L	Н	L	Z	Z	$2A_X = 2B_X$	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	H	L	Н	Н	Z	Z	$2A_X = 2B_X$	Z	Z
Н	Н	Н	L	L	Z	Z	Z	$2A_y = 2B_y$	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	Н	Н	L	Н	Z	Z	Z	$2A_y = 2B_y$	Z
Н	Н	Н	Н	L	Z	Z	Z	Z	$1A_z = 1B_z$ $2A_z = 2B_z$
Н	Н	Н	Н	Н	Z	Z	Z	Z	Z

Absolute Maximum Ratings(Note 3)

Recommended Operating Conditions (Note 6)

 $\begin{array}{ll} \mbox{Power Supply Operating (V_{CC})} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Rise and Fall Time (t_r, t_f)} \end{array}$

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

DC V_{CC} /GND Current (I_{CC} / I_{GND})

Storage Temperature Range (T_{STG})

		vcc	T _A = -40 °C to +85 °C					
Symbol	Parameter	(V)	Min	Typ (Note 7)	Max	Units	Conditions	
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	I _{IN} = -18 mA	
V _{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V		
V _{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V		
I _I	Input Leakage Current	5.5			±1.0	μΑ	$0 \le V_{IN} \le 5.5V$	
		0			±1.0	μΑ	$V_{IN} = 5.5V$	
l _{OZ}	OFF-STATE Leakage Current	5.5			±1.0	μΑ	0 ≤ A, B ≤ V _{CC}	
R _{ON}	Switch On Resistance	4.5	20	26	38	Ω	$V_{IN} = 0V$, $I_{IN} = 64$ mA	
	(Note 8)	4.5	20	27	40	Ω	$V_{IN} = 0V, I_{IN} = 30 \text{ mA}$	
		4.5	20	28	48	Ω	V _{IN} = 2.4V, I _{IN} = 15 mA	
		4.0	20	30	48	Ω	V _{IN} = 2.4V, I _{IN} = 15 mA	
I _{CC}	Quiescent Supply Current	5.5			3	μΑ	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	
ΔI _{CC}	Increase in I _{CC} per Input	5.5			2.5	mA	One Input at 3.4V	
							Other Inputs at V _{CC} or GND	
V _{IKU}	Voltage Undershoot	5.5			-2.0	V	$0.0 \text{ mA} \ge I_{\text{IN}} \ge -50 \text{ mA}$	
							$\overline{OE}_{x} = 5.5V$	

+/- 100 mA

-65°C to +150 °C

Note 7: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^{\circ}C$

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

			T _A = -40 °C	C to +85 °C	,		Conditions	
Symbol	Parameter	CL	= 50pF , RU	J = RD = 50	0 Ω	Units		Figure
Cymbol	l drameter	$V_{CC} = 4.5 - 5.5V$		V _{CC} = 4.0V		Omito	Containe	Number
		Min	Max	Min	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus-to-Bus (Note 9)		0.25		0.25	ns	V _I = OPEN	Figures 2, 3
t _{PZH} , t _{PZL}	Output Enable Time	1.5	5.5		6.0	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figures 2, 3
t _{PHZ} , t _{PLZ}	Output Disable Time	1.5	5.5		6.0	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figures 2, 3
t _{PZH} , t _{PZL}	Sel (S _{0, 1}) to Output Enable Time	1.5	6.0		6.5	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figures 2, 3
t _{PHZ} , t _{PLZ}	Sel (S _{0, 1}) to Output Disable Time	1.5	6.0		6.5	ns	$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figures 2, 3

Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	3		pF	$V_{CC} = 5.0V, V_{IN} = 0V$
C _{I/O}	Input/Output Capacitance "OFF State"	6		pF	V_{CC} , $\overline{OE} = 5.0V$, $V_{IN} = 0V$

Note 10: $T_A = +25^{\circ}C$, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 11)

Symbol	Parameter	Min	Тур	Max	Units	Conditions
V _{OUTU}	Output Voltage During Undershoot	2.5	V _{OH} – 0.3		V	Figure 1

Note 11: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage

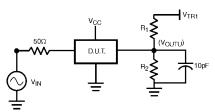
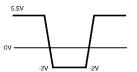


FIGURE 1.

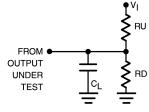
Device Test Conditions

Parameter	Value	Units
V _{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V _{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω Note: C_L includes load and stray capacitance

Note: Input Frequency = 1.0 MHz, $t_W = 500 \text{ ns}$

FIGURE 2. AC Test Circuit

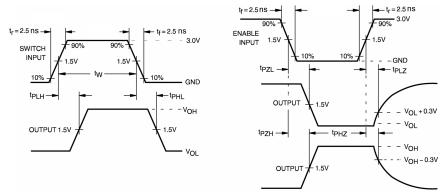
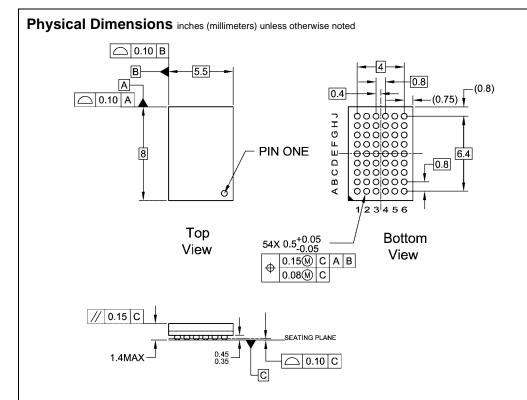


FIGURE 3. AC Waveforms

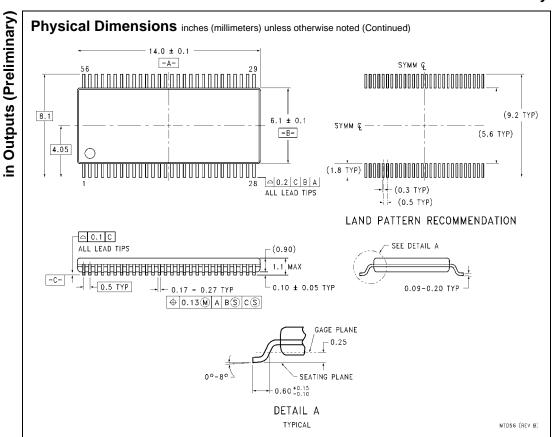


NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- **B. ALL DIMENSIONS IN MILLIMETERS**
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
 .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
 D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide Package Number BGA54A Preliminary



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

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